Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND
V+ .....-0.3V to +13V
IN_, COM_, NC_, NO_ (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current (any terminal).....±10mA
Peak Current, COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle max).....±20mA
ESD per Method 3015.7 .....> 2000V
Continuous Power Dissipation
SOT23-6 (derate 7.1mW/°C above +70°C).....571mW
SOT23-8 (derate 5.3mW/°C above +70°C).....421mW
TDFN (derate 24.4mW/°C above +70°C).....1951mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
Narrow SO (derate 5.88mW/°C above +70°C) 471mW
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX454_C_ _ .....0°C to +70°C
MAX454_E_ _.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on NC_, NO_, COM_, or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, GND = 0, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 4)			0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, $I_{COM\_}$ = 1.0mA, $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	T_A = +25°C			30	60	Ω
			T_A = T_{MIN} to T_{MAX}				75	
On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 5V, $I_{COM\_}$ = 1.0mA, $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	T_A = +25°C			0.8	2	Ω
			T_A = T_{MIN} to T_{MAX}				4	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 5V; $I_{COM\_}$ = 1.0mA; $V_{NO\_}$ or $V_{NC\_}$ = 1V, 2V, 3V	T_A = +25°C			2	6	Ω
			T_A = T_{MIN} to T_{MAX}				8	
NO_ or NC_ Off-Leakage Current (Note 7)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1V	T_A = +25°C		-0.1	±0.01	+0.1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-5		+5	
COM_ Off-Leakage Current (Note 7)	$I_{COM(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V; $V_{NO\_}$ or $V_{NC\_}$ = 1V, 4.5V	T_A = +25°C		-0.1		+0.1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-5		+5	
COM_ On-Leakage Current (Note 7)	$I_{COM(ON)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V or $V_{NO\_}$ or $V_{NC\_}$ = 1V, 4.5V, or floating	T_A = +25°C		-0.2		+0.2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		+10	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, GND = 0, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 3V, Figure 2	T_A = +25°C		35	100	ns
			T_A = T_{MIN} to T_{MAX}			240	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 3V, Figure 2	T_A = +25°C		25	75	ns
			T_A = T_{MIN} to T_{MAX}			150	
Break-Before-Make Time Delay (Note 4)	t_D	MAX4543/MAX4544 only, R_L = 300Ω, C_L = 35pF		2	10		ns
Charge Injection (Note 4)	Q	C_L = 1.0nF, V_{GEN} = 0, R_{GEN} = 0, T_A = +25°C, Figure 4			1	5	pC
Off-Isolation (Note 8)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, T_A = +25°C, Figure 5			-76		dB
Crosstalk (Note 9)		R_L = 50Ω, C_L = 5pF, f = 1MHz, T_A = +25°C, Figure 6			-90		dB
NC_ or NO_ Capacitance	C_{OFF}	f = 1MHz, T_A = +25°C, Figure 7			8		pF
COM_ Off-Capacitance	$C_{COM(OFF)}$	f = 1MHz, T_A = +25°C, Figure 7			8		pF
COM_ On-Capacitance	$C_{COM(ON)}$	f = 1MHz, T_A = +25°C, Figure 7	MAX4541/MAX4542/ MAX4543		13		pF
			MAX4544		20		
SUPPLY							
Power-Supply Range	V+			2.7		12	V
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0 or V+, all channels on or off		-1	±0.0001	+1	µA
LOGIC INPUT							
Input-Voltage Low	V_{INL}					0.8	V
Input-Voltage High	V_{INH}			2.4			V

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = +3.0V to +3.6V, GND = 0, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 2, 3)

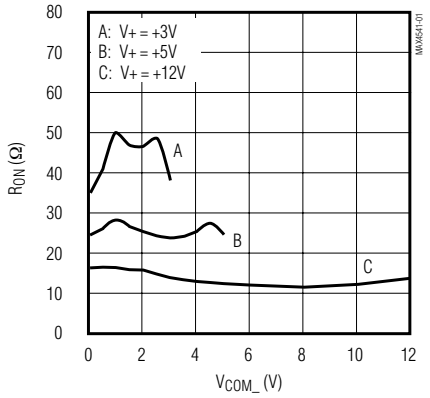
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)		0		V+	V
Channel On-Resistance	R_{ON}	V+ = 3V, $I_{COM\_}$ = 1.0mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		50	125	Ω
			T_A = T_{MIN} to T_{MAX}			275	
DYNAMIC							
Turn-On Time (Note 3)	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		80	400	ns
			T_A = T_{MIN} to T_{MAX}			500	
Turn-Off Time (Note 3)	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		50	125	ns
			T_A = T_{MIN} to T_{MAX}			175	
Break-Before-Make Time Delay (Note 3)	t_D	MAX4543/MAX4544 only, R_L = 300Ω, C_L = 35pF, T_A = +25°C		2	30		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0, R_{GEN} = 0, T_A = +25°C			1	5	pC
SUPPLY							
Positive Supply Current	I+	V+ = 3.6V, V_{IN} = 0 or V+, all channels on or off		-1		+1	µA

Note 2: QFN and SOT-packaged parts are 100% tested at +25°C only and guaranteed by correlation at the full hot rated temperature.
Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 4: Guaranteed by design.
Note 5: $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min.
Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 7: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
Note 8: Off-isolation = 20 x $\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 9: Between the two switches, MAX4541/MAX4542/MAX4543 only.

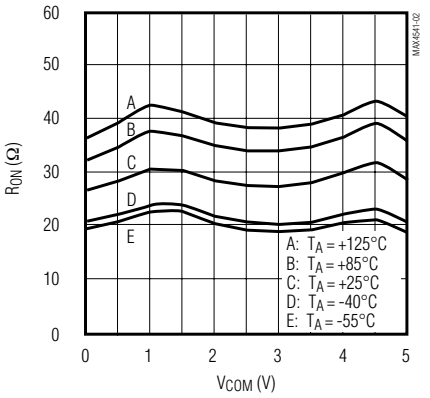
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

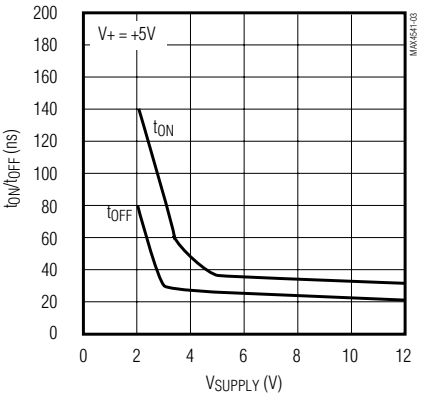
ON-RESISTANCE vs. COM_ VOLTAGE



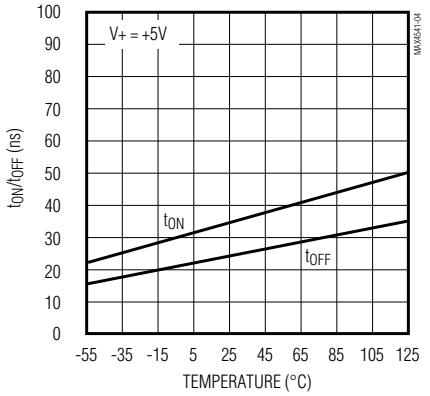
ON-RESISTANCE vs. COM VOLTAGE OVER TEMPERATURE



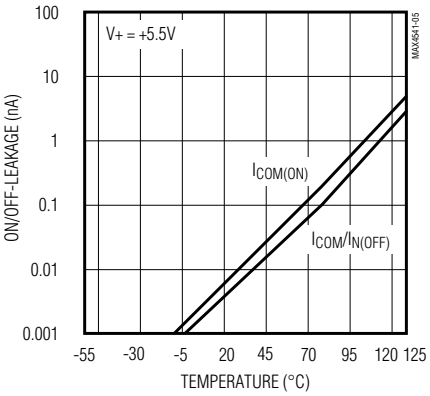
TURN-ON/OFF TIMES vs. SUPPLY VOLTAGE



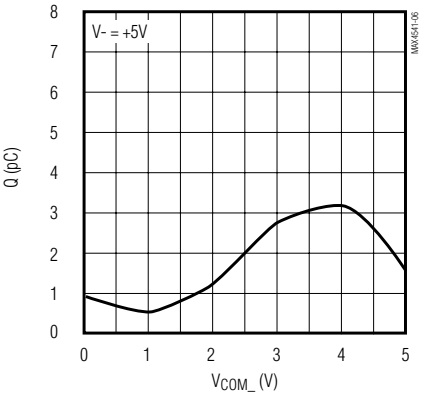
TURN-ON/OFF TIMES vs. TEMPERATURE



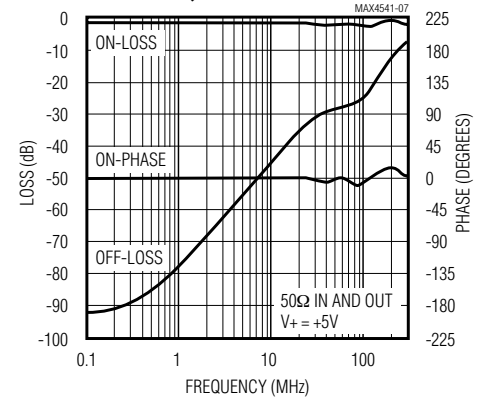
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



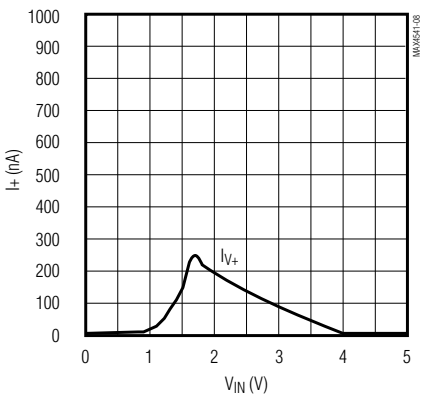
CHARGE INJECTION vs. COM_ VOLTAGE



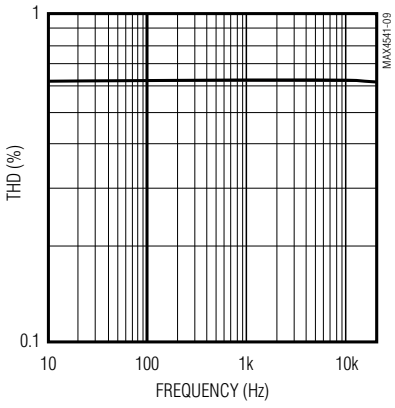
FREQUENCY RESPONSE



INPUT VOLTAGE vs. SUPPLY CURRENT



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Pin Description

PIN								NAME	FUNCTION
MAX4541		MAX4542		MAX4543		MAX4544			
DIP/SO/ µMAX/ TDFN	SOT23-8	DIP/SO/ µMAX/ TDFN	SOT23-8	DIP/SO/ µMAX/ TDFN	SOT23-8	DIP/SO/ µMAX/ TDFN	SOT23-6		
1	1	—	—	1	1	—	—	NO1	Analog Switch 1—Normally Open
2	8	2	8	2	8	—	—	COM1	Analog Switch 1—Common
3	3	3	3	3	3	—	—	IN2	Digital Control Input 2
4	6	4	6	4	6	4	3	GND	Ground—Negative Supply Input
5	5	—	—	—	—	—	—	NO2	Analog Switch 2—Normally Open
6	4	6	4	6	4	—	—	COM2	Analog Switch 2—Common
7	7	7	7	7	7	—	—	IN1	Digital Control Input 1
8	2	8	2	8	2	8	2	V+	Positive Supply Voltage Input
—	—	1	1	—	—	—	—	NC1	Analog Switch 1—Normally Closed
—	—	5	5	5	5	—	—	NC2	Analog Switch 2—Normally Closed
—	—	—	—	—	—	1	6	NO	Analog Switch—Normally Open
—	—	—	—	—	—	2	5	COM	Analog Switch—Common
—	—	—	—	—	—	3	4	NC	Analog Switch—Normally Closed
—	—	—	—	—	—	5, 6	—	N.C.	Not Connected (Open Circuit)
—	—	—	—	—	—	7	1	IN	Digital Control Input
EP	—	EP	—	EP	—	EP	—	EP	Exposed Pad. Connect EP to V+.

Applications Information

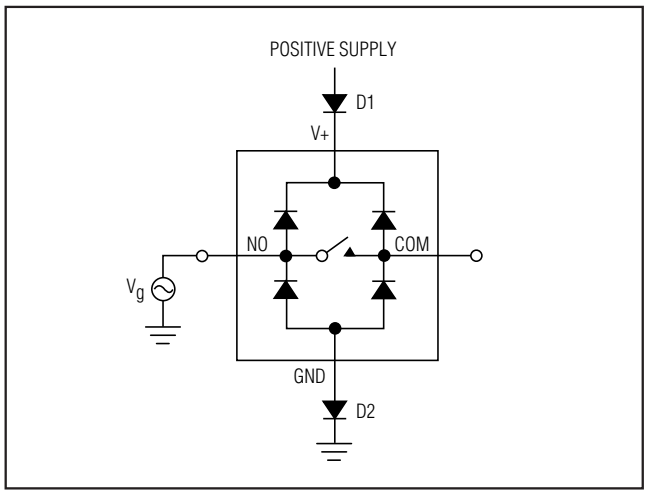


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

Logic Levels

The MAX4541–MAX4544 are TTL compatible when powered from a single +5V supply. When powered from other supply voltages, TTL compatibility is guaranteed and the logic inputs can be driven rail-to-rail. For example, with a +12V supply, IN1 and IN2 can be driven low to 0 and high to 12V. With a +3.3V supply, IN1 and IN2 should be driven low to 0 and high to 3.3V.

Driving IN1 and IN2 rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be switched with very little change in on-resistance over the entire voltage range (see the *Typical Operating Characteristics*). All the switches are bidirectional, so the NO_, NC_, and COM_ pins can be used as either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals or logic inputs, especially if the analog or logic signals are not current limited. If this sequencing is not possible, and if the analog or logic inputs are not current limited to <10mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V+) must not exceed 13V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. This can be significant when low supply voltages (+5V or less) are used. With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Test Circuits/Timing Diagrams

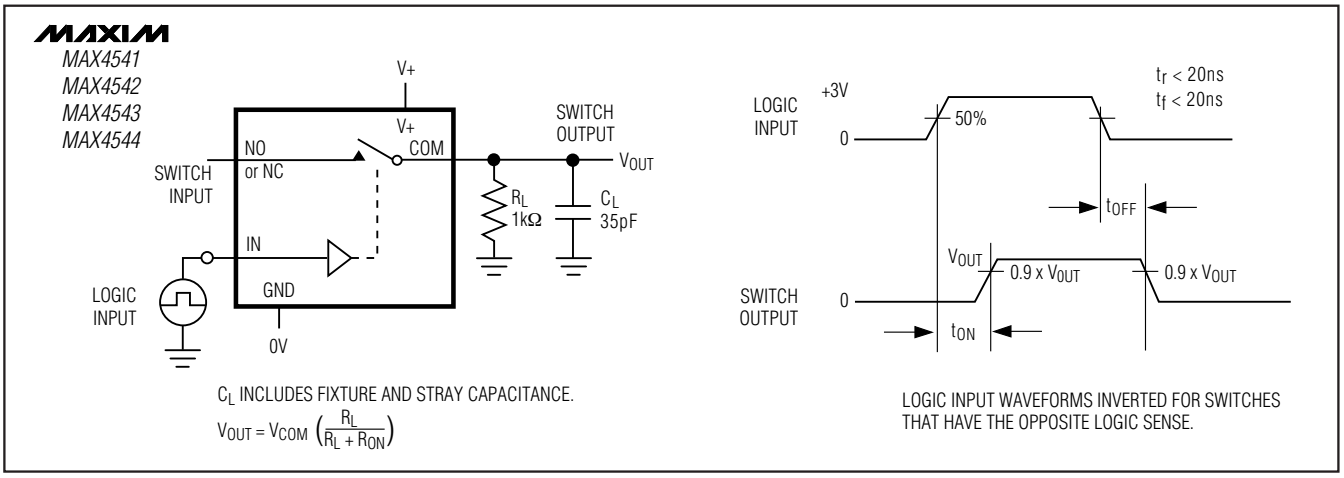


Figure 2. Switching Time

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Test Circuits/Timing Diagrams (continued)

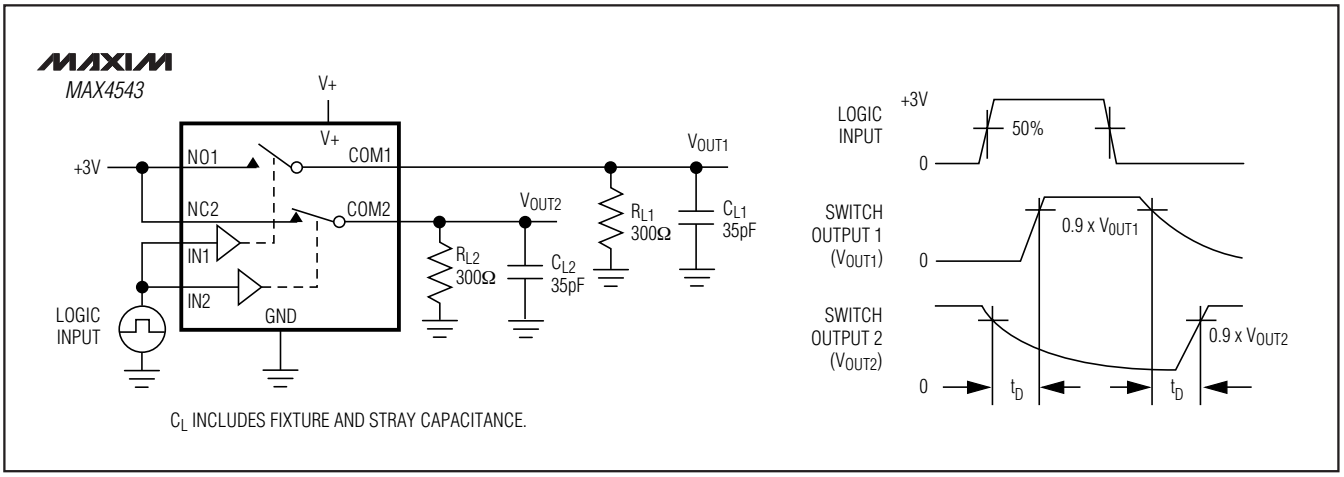


Figure 3a. Break-Before-Make Interval (MAX4543 Only)

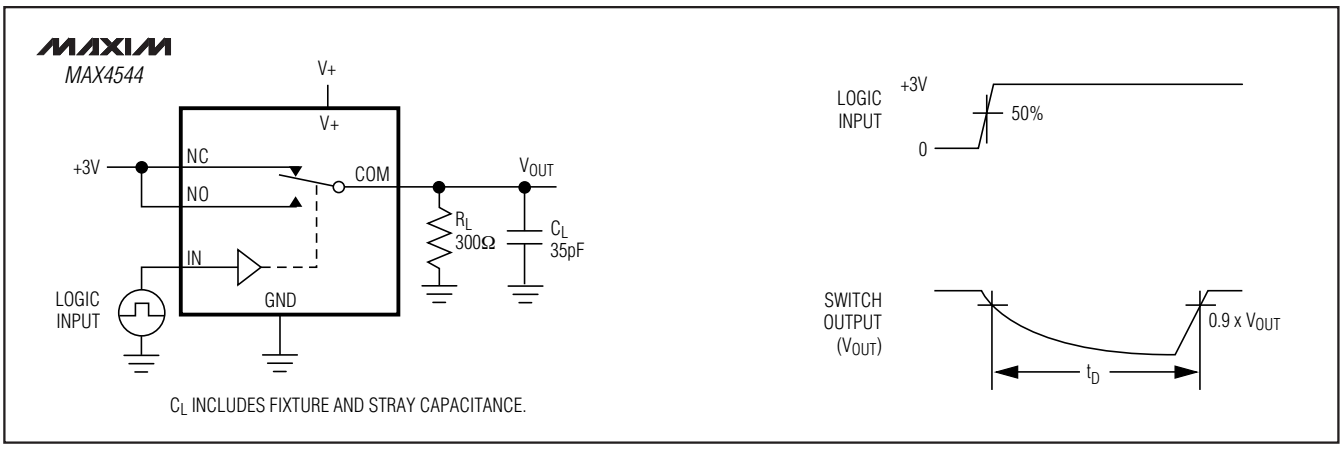


Figure 3b. Break-Before-Make Interval (MAX4544 Only)

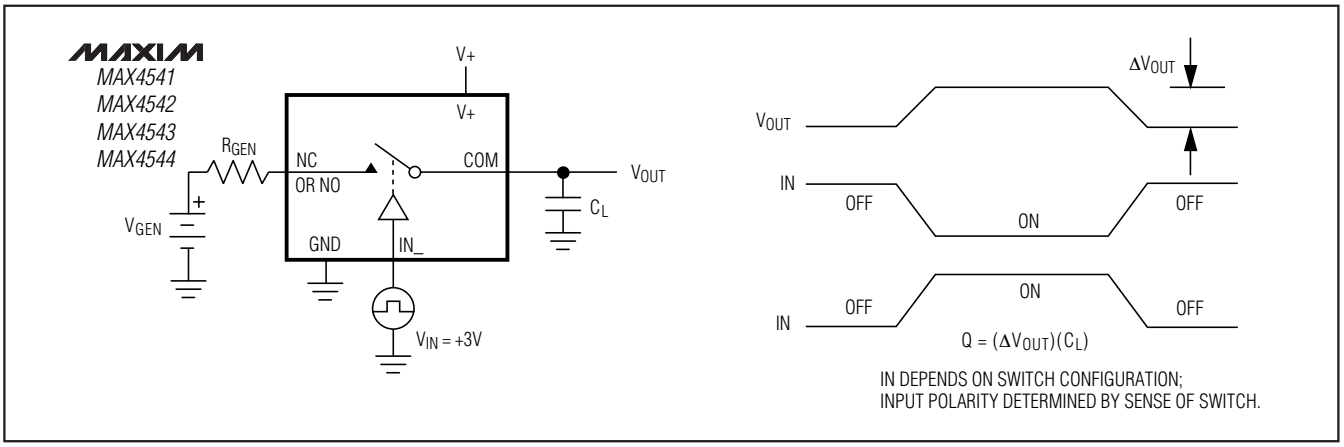


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

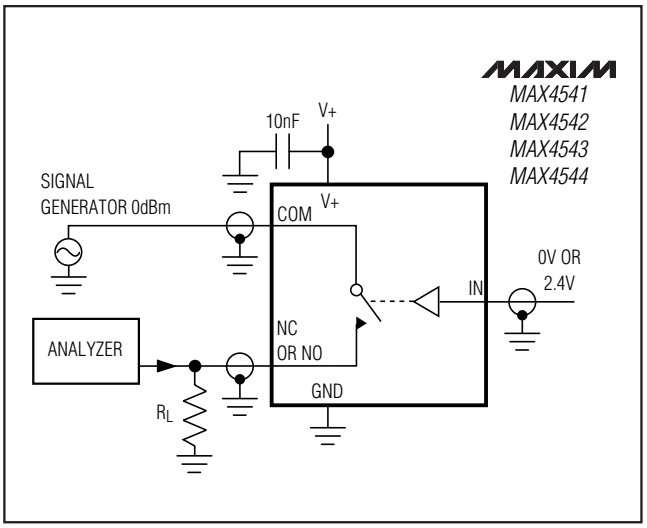


Figure 5. Off-Isolation

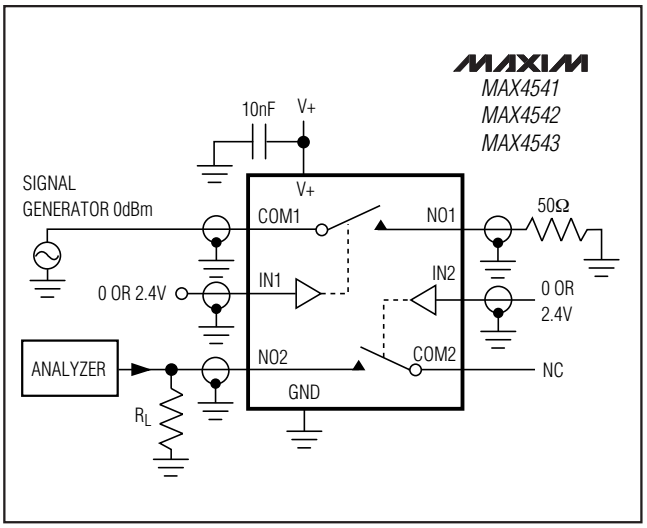


Figure 6. Crosstalk

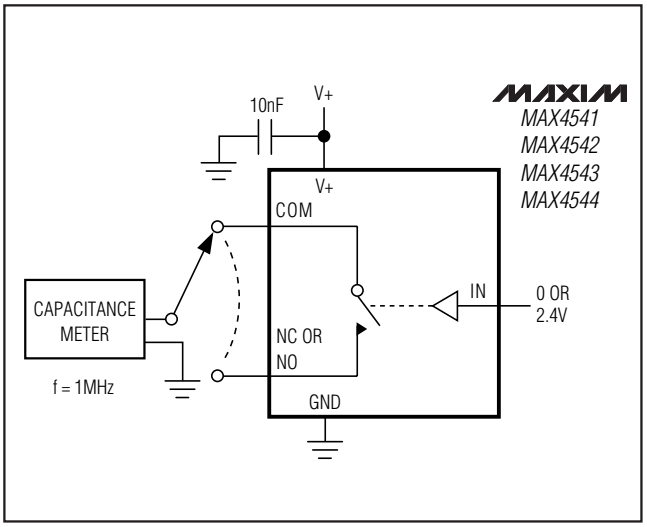


Figure 7. Channel Off/On-Capacitance

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

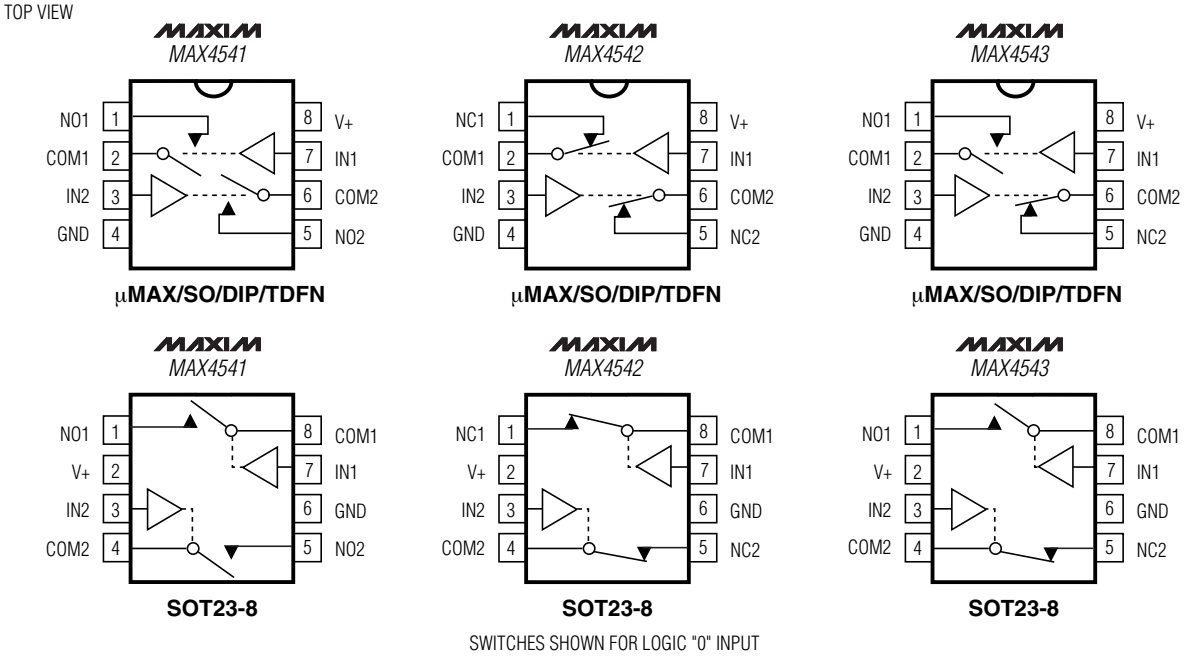
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4541EPA	-40°C to +85°C	8 Plastic DIP	—
MAX4542CUA	0°C to +70°C	8 µMAX	—
MAX4542CSA	0°C to +70°C	8 SO	—
MAX4542CPA	0°C to +70°C	8 Plastic DIP	—
MAX4542C/D	0°C to +70°C	Dice*	—
MAX4542EKA-T	-40°C to +85°C	8 SOT23-8	AAAF
MAX4542ETA	-40°C to +85°C	8 TDFN-EP**	—
MAX4542EUA	-40°C to +85°C	8 µMAX	—
MAX4542ESA	-40°C to +85°C	8 SO	—
MAX4542EPA	-40°C to +85°C	8 Plastic DIP	—
MAX4543CUA	0°C to +70°C	8 µMAX	—
MAX4543CSA	0°C to +70°C	8 SO	—
MAX4543CPA	0°C to +70°C	8 Plastic DIP	—
MAX4543C/D	0°C to +70°C	Dice*	—
MAX4543EKA-T	-40°C to +85°C	8 SOT23-8	AAAG
MAX4543ETA	-40°C to +85°C	8 TDFN-EP**	—
MAX4543EUA	-40°C to +85°C	8 µMAX	—
MAX4543ESA	-40°C to +85°C	8 SO	—
MAX4543EPA	-40°C to +85°C	8 Plastic DIP	—
MAX4544CUA	0°C to +70°C	8 µMAX	—
MAX4544CSA	0°C to +70°C	8 SO	—
MAX4544CPA	0°C to +70°C	8 Plastic DIP	—
MAX4544C/D	0°C to +70°C	Dice*	—
MAX4544EUT-T	-40°C to +85°C	6 SOT23-6	AAAM
MAX4544ETA	-40°C to +85°C	8 TDFN-EP**	—
MAX4544EUA	-40°C to +85°C	8 µMAX	—
MAX4544ESA	-40°C to +85°C	8 SO	—
MAX4544EPA	-40°C to +85°C	8 Plastic DIP	—

**Dice are specified at T_A = +25°C.*
***EP = Exposed pad.*

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW

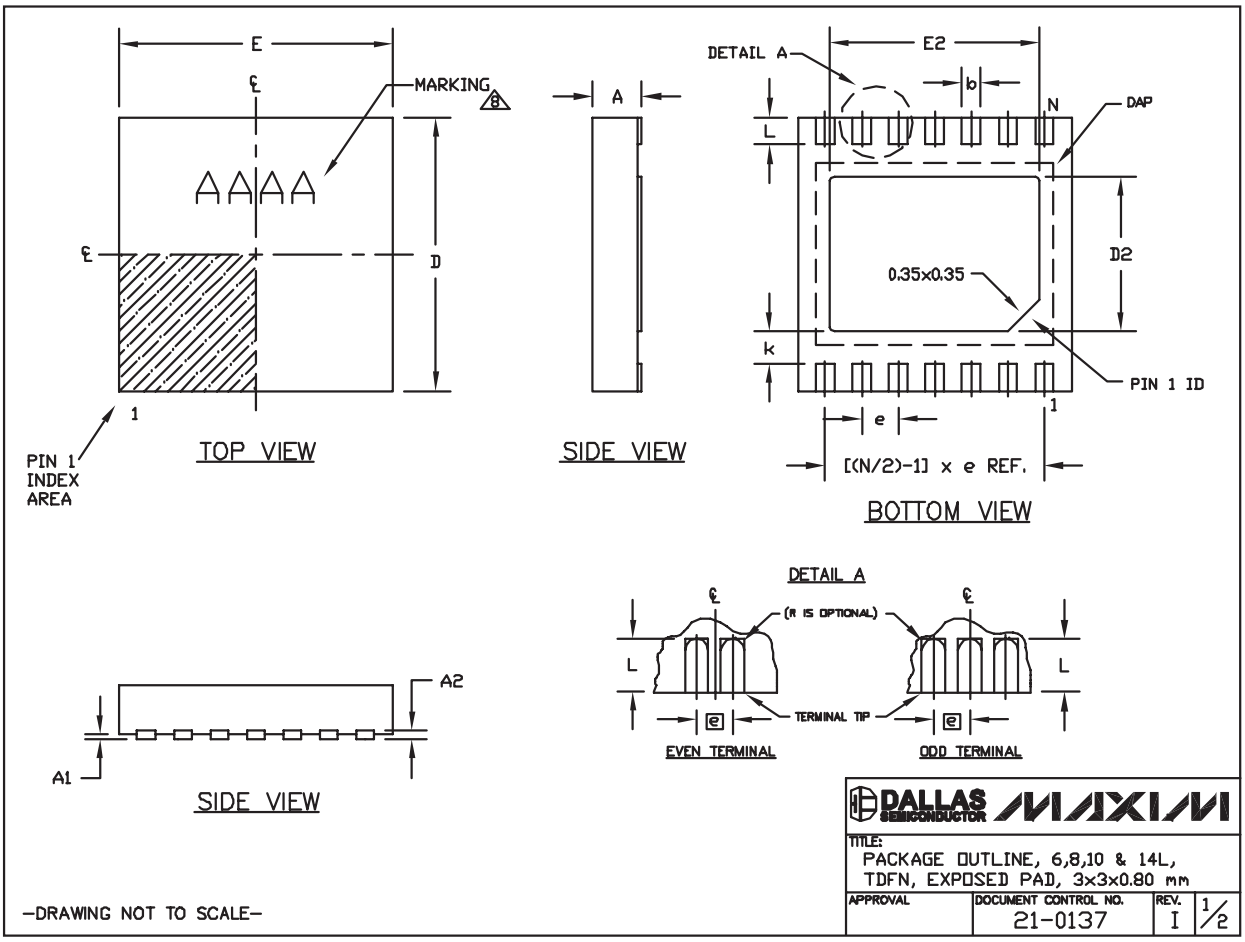


SWITCHES SHOWN FOR LOGIC "0" INPUT

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

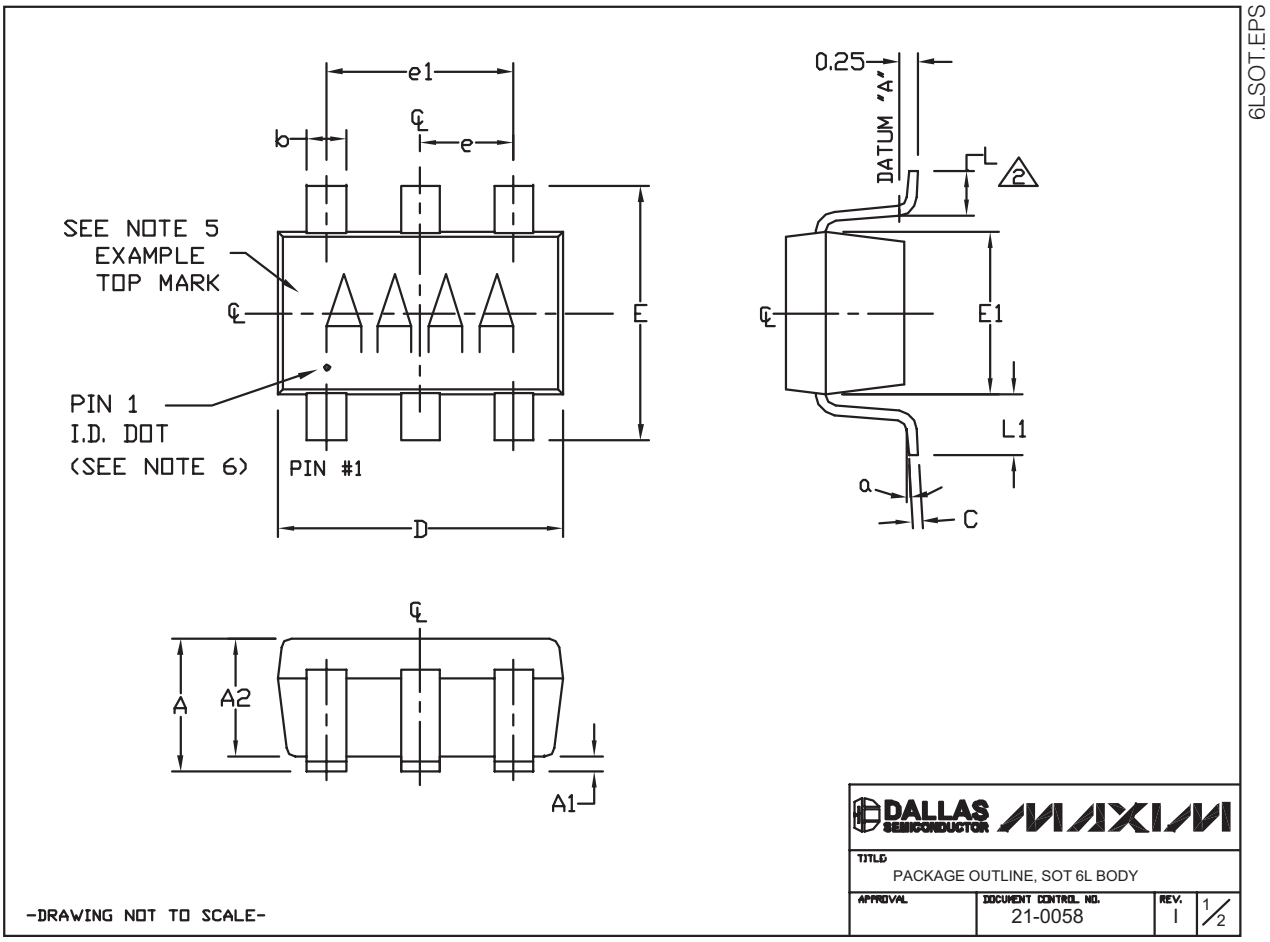
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3mm ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF.		
e1	1.90 BSC.		
e	0.95 BSC.		
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-2, U6-4, U6C-8, U6SN-1, U6CN-2, U6S-3, U6F-5, U6F-6, U6FH-5, U6FH-6

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

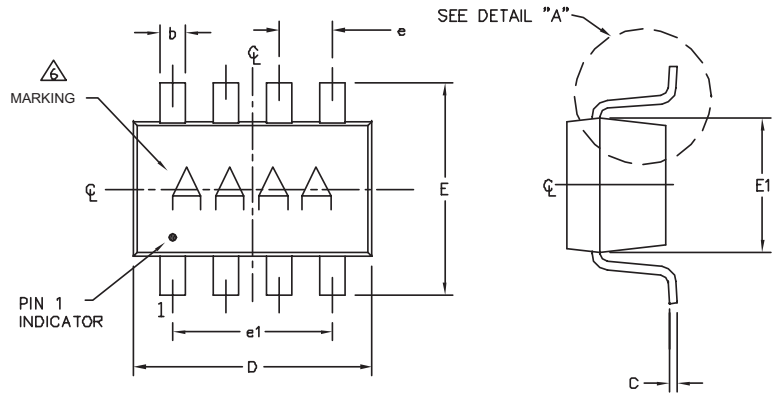
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	I	2/2

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Package Information (continued)

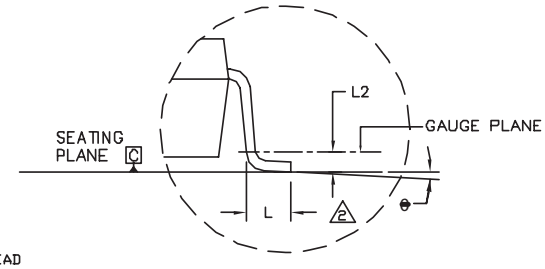
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°

PKG CODES: K8–1, K8–2, K8S–3, K8F–4, K8FH–4, K8–5, K8C–6; K8SN–1; K8CN–1



DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	G	1/1

Revision History

Pages changed at Rev 4: 1–16

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