

LT1352/LT1353

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 36V
 Differential Input Voltage (Transient Only, Note 2) $\pm 10V$
 Input Voltage $\pm V_S$
 Output Short-Circuit Duration (Note 3) Indefinite
 Operating Temperature Range -40°C to 85°C

Specified Temperature Range (Note 7) .. -40°C to 85°C
 Maximum Junction Temperature (See Below)
 Plastic Package 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$ (N8) $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 190^\circ\text{C/W}$ (S8)	ORDER PART NUMBER LT1352CN8 LT1352CS8 LT1352IN8 LT1352IS8 S8 PART MARKING 1352 1352I	TOP VIEW S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 150^\circ\text{C/W}$	ORDER PART NUMBER LT1353CS
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Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0V$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15V$		0.2	0.6	mV
			$\pm 5V$		0.2	0.6	mV
			$\pm 2.5V$		0.3	0.8	mV
I_{OS}	Input Offset Current		$\pm 2.5V$ to $\pm 15V$		5	15	nA
I_B	Input Bias Current		$\pm 2.5V$ to $\pm 15V$		20	50	nA
e_n	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		14		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		0.5		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$ Differential	$\pm 15V$	300	600		$M\Omega$
			$\pm 15V$		20		$M\Omega$
C_{IN}	Input Capacitance		$\pm 15V$		3		pF
			$\pm 15V$	12.0	13.5		V
			$\pm 5V$	2.5	3.5		V
	Positive Input Voltage Range		$\pm 2.5V$	0.5	1.0		V
			$\pm 15V$		-13.5	-12.0	V
			$\pm 5V$		-3.5	-2.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$ $V_{CM} = \pm 2.5V$ $V_{CM} = \pm 0.5V$	$\pm 15V$	80	94		dB
			$\pm 5V$	78	86		dB
			$\pm 2.5V$	68	77		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 15V$		90	106		dB

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ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 5\text{k}$	$\pm 15\text{V}$	40	80		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	30	60		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	20	40		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 5\text{k}$	$\pm 5\text{V}$	30	60		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	25	50		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	15	30		V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 5\text{k}$	$\pm 2.5\text{V}$	20	40		V/mV
V_{OUT}	Output Swing	$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.5	14.0		$\pm\text{V}$
		$R_L = 2\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.4	13.8		$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.0	13.4		$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.5	4.0		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.4	3.8		$\pm\text{V}$
		$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.3	1.7		$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 13\text{V}$	$\pm 15\text{V}$	13.0	13.4		mA
		$V_{OUT} = \pm 3.4\text{V}$	$\pm 5\text{V}$	6.8	7.6		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	30	45		mA
SR	Slew Rate	$A_V = -1$, $R_L = 5\text{k}$ (Note 4)	$\pm 15\text{V}$	120	200		V/ μs
			$\pm 5\text{V}$	30	50		V/ μs
	Full-Power Bandwidth	10V Peak (Note 5) 3V Peak (Note 5)	$\pm 15\text{V}$		3.2		MHz
			$\pm 5\text{V}$		2.6		MHz
GBW	Gain Bandwidth	$f = 200\text{kHz}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	2.0	3.0		MHz
			$\pm 5\text{V}$	1.8	2.7		MHz
			$\pm 2.5\text{V}$		2.5		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V	$\pm 15\text{V}$		46		ns
			$\pm 5\text{V}$		53		ns
	Overshoot	$A_V = 1$, 0.1V	$\pm 15\text{V}$		13		%
			$\pm 5\text{V}$		16		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT} , 0.1V	$\pm 15\text{V}$		41		ns
			$\pm 5\text{V}$		52		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		700		ns
		10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		1250		ns
		5V Step, 0.1%, $A_V = -1$	$\pm 5\text{V}$		950		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$		1400		ns
R_O	Output Resistance	$A_V = 1$, $f = 20\text{kHz}$	$\pm 15\text{V}$		1.5		Ω
	Channel Separation	$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	101	120		dB
I_S	Supply Current	Each Amplifier	$\pm 15\text{V}$		250	320	μA
		Each Amplifier	$\pm 5\text{V}$		230	300	μA

 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15\text{V}$			0.8	mV
			$\pm 5\text{V}$			0.8	mV
			$\pm 2.5\text{V}$			1.0	mV
	Input V_{OS} Drift	(Note 6)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$		3	8	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			20	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			75	nA

ELECTRICAL CHARACTERISTICS

$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	78			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	77			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		89			dB
A _{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 5\text{k}$	$\pm 15\text{V}$	25			V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	20			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 5\text{k}$	$\pm 5\text{V}$	20			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	10			V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 5\text{k}$	$\pm 2.5\text{V}$	15			V/mV
V _{OUT}	Output Swing	$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.4			$\pm \text{V}$
		$R_L = 2\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.3			$\pm \text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	12.0			$\pm \text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.4			$\pm \text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.3			$\pm \text{V}$
		$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.2			$\pm \text{V}$
I _{OUT}	Output Current	$V_{OUT} = \pm 12\text{V}$	$\pm 15\text{V}$	12.0			mA
		$V_{OUT} = \pm 3.3\text{V}$	$\pm 5\text{V}$	6.6			mA
I _{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	24			mA
SR	Slew Rate	$A_V = -1$, $R_L = 5\text{k}$ (Note 4)	$\pm 15\text{V}$	100			V/ μs
			$\pm 5\text{V}$	21			V/ μs
GBW	Gain Bandwidth	$f = 200\text{kHz}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	1.8			MHz
			$\pm 5\text{V}$	1.6			MHz
	Channel Separation	$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	100			dB
I _S	Supply Current	Each Amplifier	$\pm 15\text{V}$			350	μA
		Each Amplifier	$\pm 5\text{V}$			330	μA

$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted (Note 7)

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage		$\pm 15\text{V}$			1.0	mV
			$\pm 5\text{V}$			1.0	mV
			$\pm 2.5\text{V}$			1.2	mV
	Input V _{OS} Drift	(Note 6)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$		3	8	$\mu\text{V}/^{\circ}\text{C}$
I _{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			50	nA
I _B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			100	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	76			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	76			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		87			dB
A _{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 5\text{k}$	$\pm 15\text{V}$	20			V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 5\text{k}$	$\pm 5\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	10			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	8			V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 5\text{k}$	$\pm 2.5\text{V}$	10			V/mV

ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted (Note 7)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.3			$\pm\text{V}$
		$R_L = 2\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.2			$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	10.0			$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.3			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.2			$\pm\text{V}$
		$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.1			$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 10\text{V}$	$\pm 15\text{V}$	10.0			mA
		$V_{OUT} = \pm 3.2\text{V}$	$\pm 5\text{V}$	6.4			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	20			mA
SR	Slew Rate	$A_V = -1$, $R_L = 5\text{k}$ (Note 4)	$\pm 15\text{V}$	50			$\text{V}/\mu\text{s}$
			$\pm 5\text{V}$	15			$\text{V}/\mu\text{s}$
GBW	Gain Bandwidth	$f = 200\text{kHz}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	1.6			MHz
			$\pm 5\text{V}$	1.4			MHz
	Channel Separation	$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	99			dB
I_S	Supply Current	Each Amplifier	$\pm 15\text{V}$			380	μA
		Each Amplifier	$\pm 5\text{V}$			350	μA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of $\pm 10\text{V}$ are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Slew rate is measured between $\pm 8\text{V}$ on the output with $\pm 12\text{V}$

input for $\pm 15\text{V}$ supplies and $\pm 2\text{V}$ on the output with $\pm 3\text{V}$ input for $\pm 5\text{V}$ supplies.

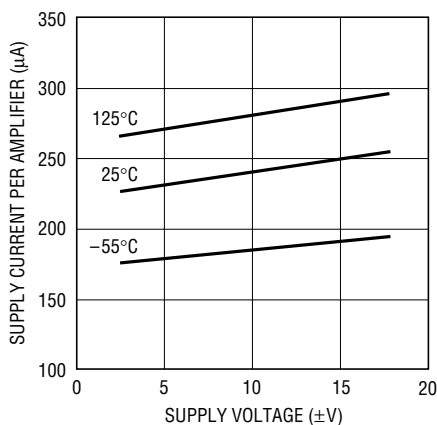
Note 5: Full-power bandwidth is calculated from the slew rate measurement: $\text{FPBW} = (\text{Slew Rate})/2\pi V_P$.

Note 6: This parameter is not 100% tested.

Note 7: The LT1352C/LT1353C are guaranteed to meet specified performance from 0°C to 70°C . The LT1352C/LT1353C are designed, characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1352I/LT1353I are guaranteed to meet specified performance from -40°C to 85°C .

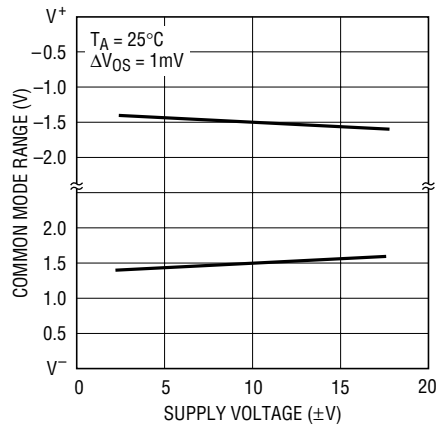
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



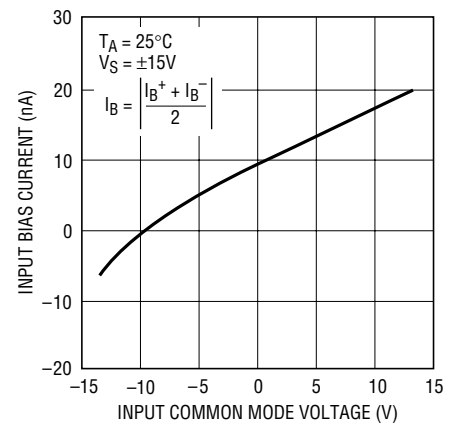
1352/53 G01

Input Common Mode Range vs Supply Voltage



1352/53 G02

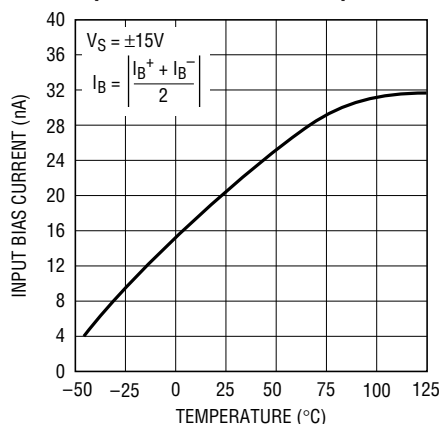
Input Bias Current vs Input Common Mode Voltage



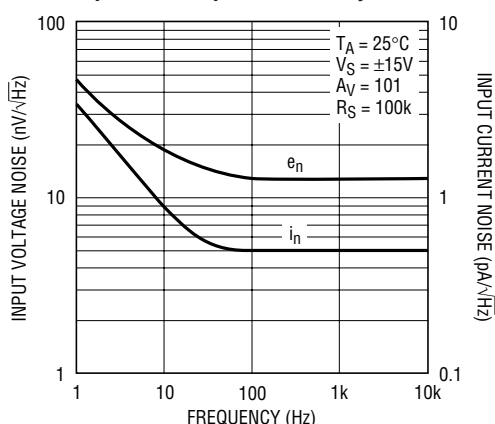
1352/53 G03

TYPICAL PERFORMANCE CHARACTERISTICS

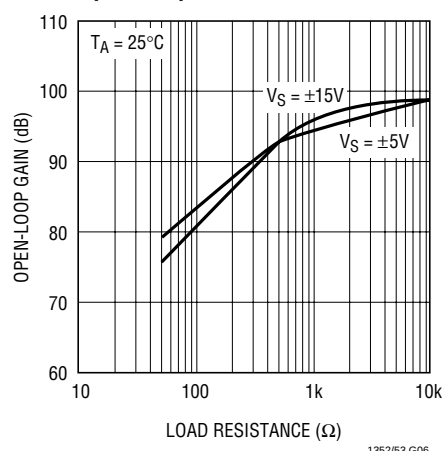
Input Bias Current vs Temperature



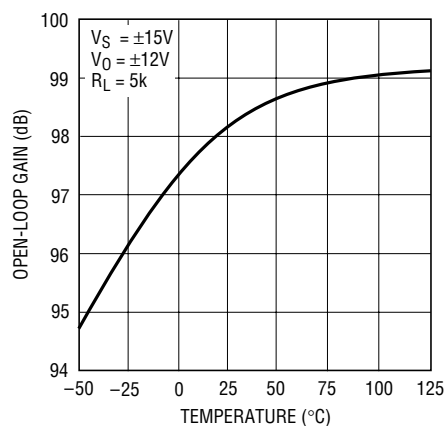
Input Noise Spectral Density



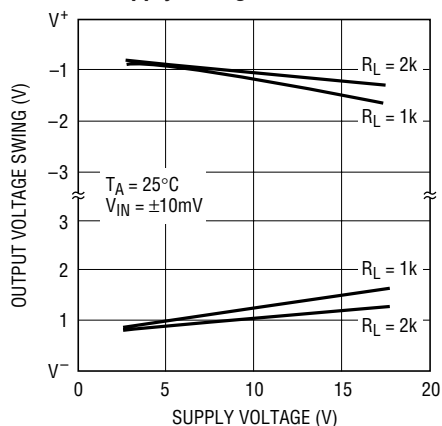
Open-Loop Gain vs Resistive Load



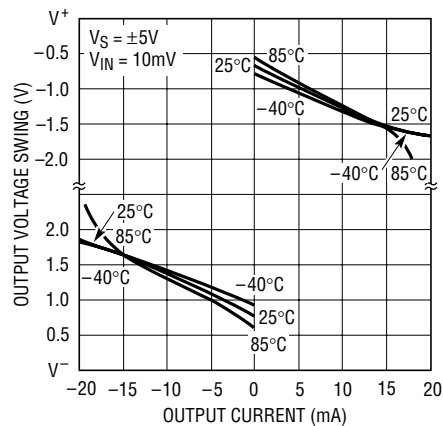
Open-Loop Gain vs Temperature



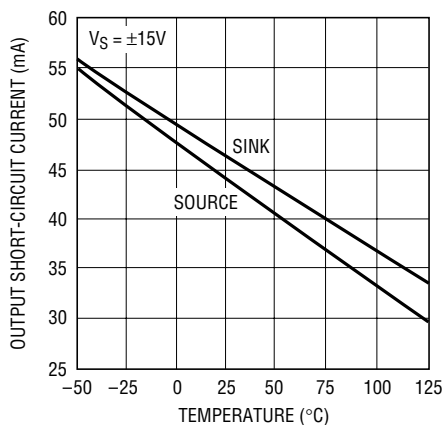
Output Voltage Swing vs Supply Voltage



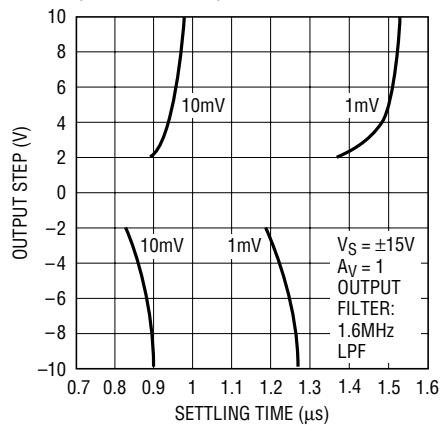
Output Voltage Swing vs Load Current



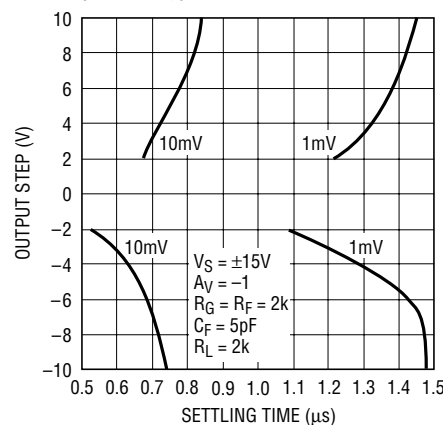
Output Short-Circuit Current vs Temperature



Settling Time vs Output Step (Noninverting)

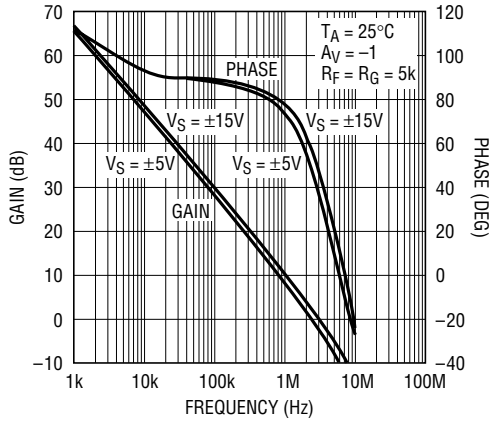


Settling Time vs Output Step (Inverting)



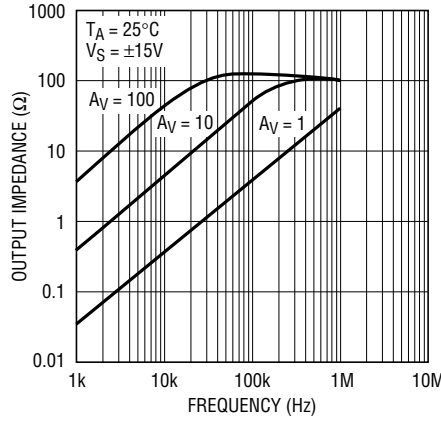
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase vs Frequency



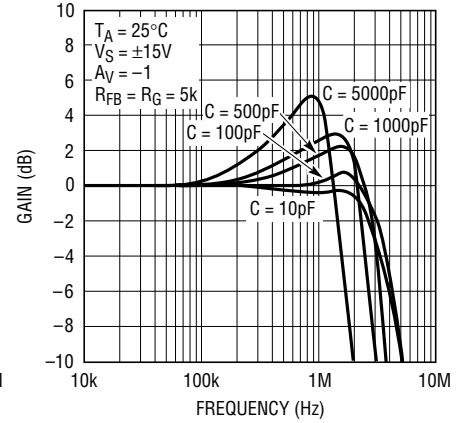
1352/53 G13

Output Impedance vs Frequency



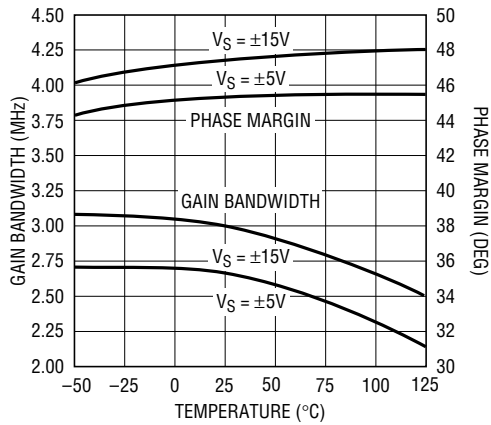
1352/53 G14

Frequency Response vs Capacitive Load



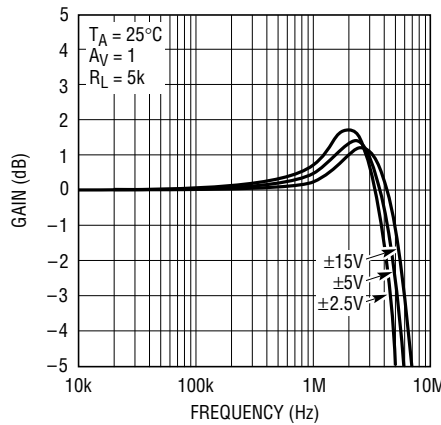
1352/53 G15

Gain Bandwidth and Phase Margin vs Temperature



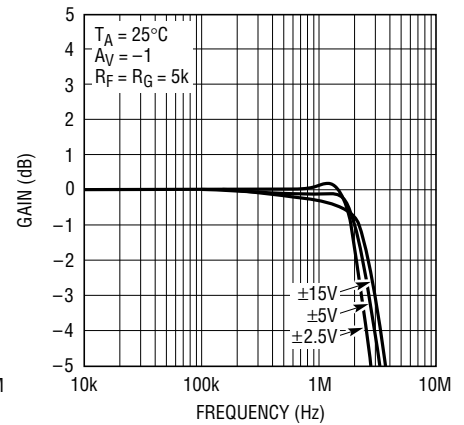
1352/53 G16

Frequency Response vs Supply Voltage (AV = 1)



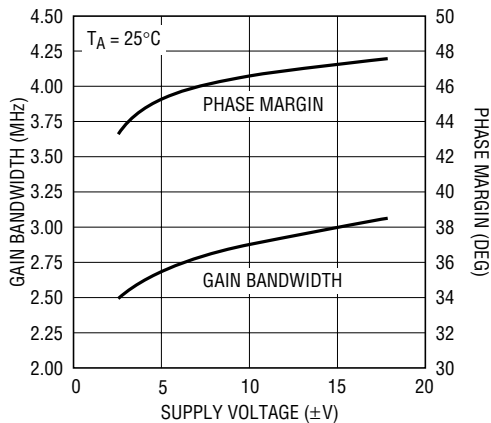
1352/53 G17

Frequency Response vs Supply Voltage (AV = -1)



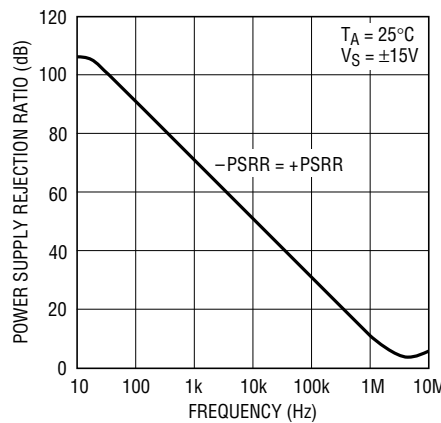
1352/53 G18

Gain Bandwidth and Phase Margin vs Supply Voltage



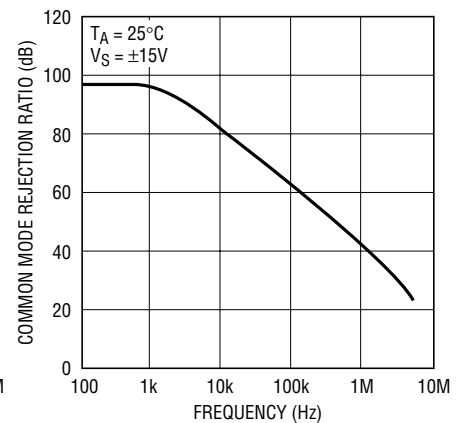
1352/53 G19

Power Supply Rejection Ratio vs Frequency



1352/53 G20

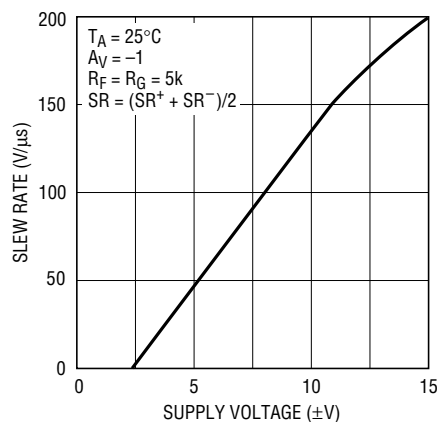
Common Mode Rejection Ratio vs Frequency



1352/53 G21

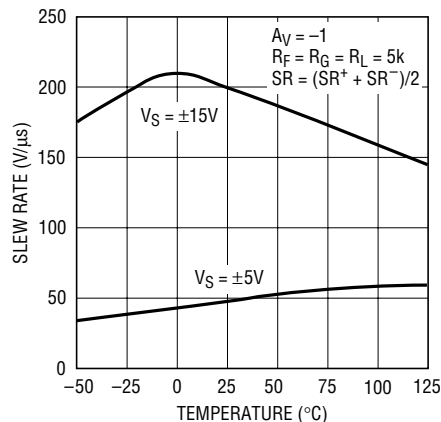
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Supply Voltage



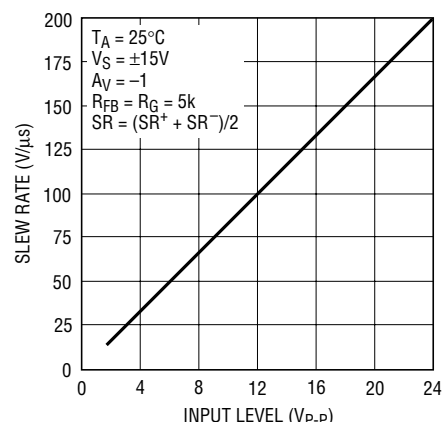
1352/53 G22

Slew Rate vs Temperature



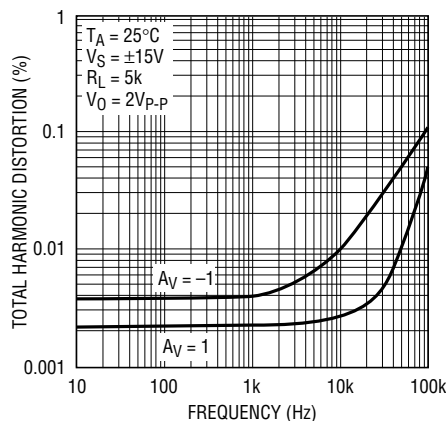
1352/53 G23

Slew Rate vs Input Level



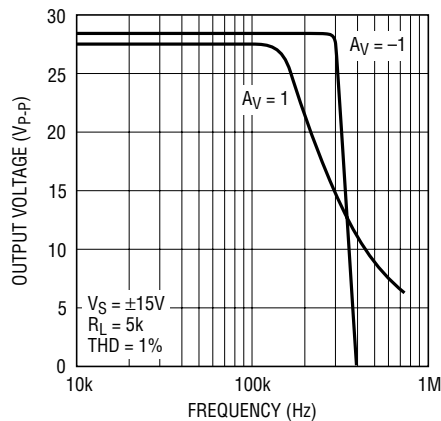
1352/53 G24

Total Harmonic Distortion vs Frequency



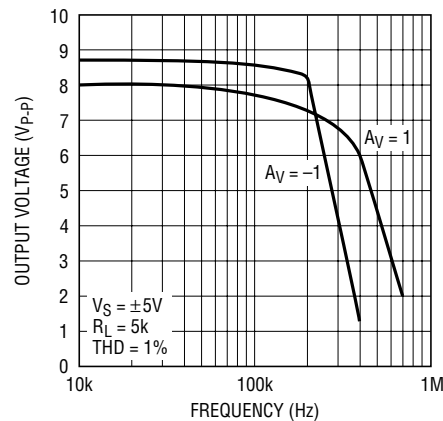
1352/53 G25

Undistorted Output Swing vs Frequency (±15V)



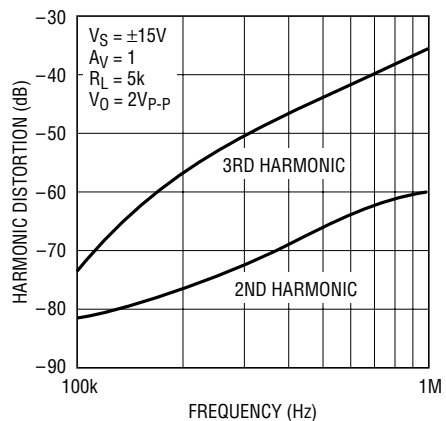
1352/53 G26

Undistorted Output Swing vs Frequency (±5V)



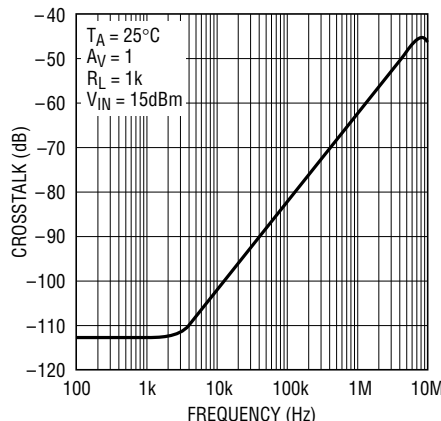
1352/53 G27

2nd and 3rd Harmonic Distortion vs Frequency



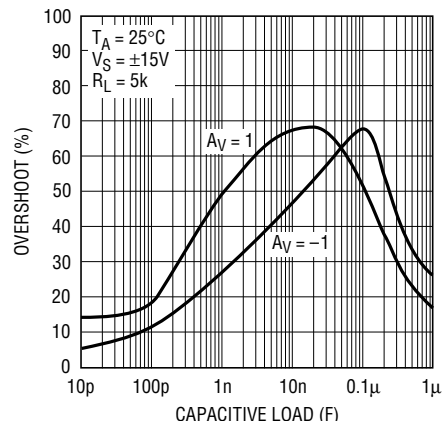
1352/53 G28

Crosstalk vs Frequency



1352/53 G29

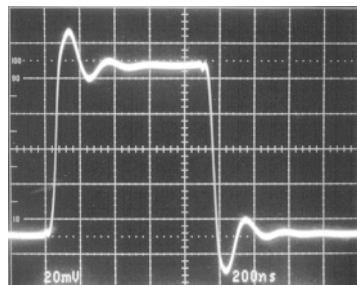
Capacitive Load Handling



1352/53 G30

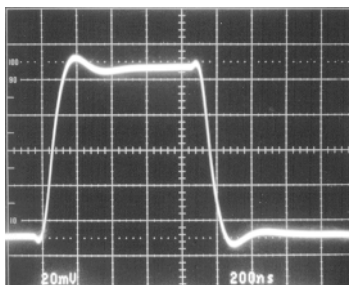
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient
($A_V = 1$)



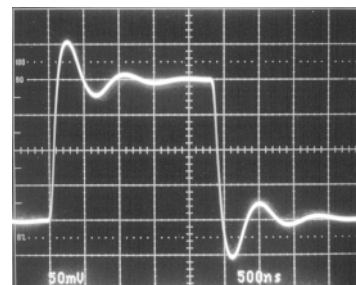
1352/53 G31

Small-Signal Transient
($A_V = -1$)



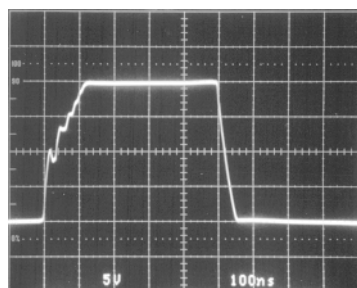
1352/53 G32

Small-Signal Transient
($A_V = -1$, $C_L = 1000\text{pF}$)



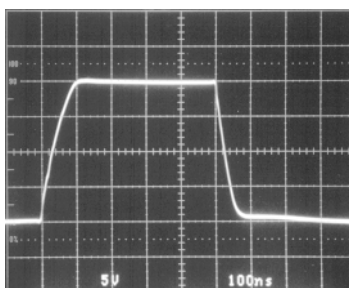
1352/53 G33

Large-Signal Transient
($A_V = 1$)



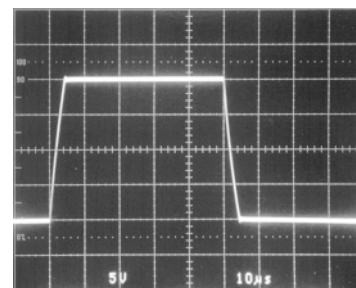
1352/53 G34

Large-Signal Transient
($A_V = -1$)



1352/53 G35

Large-Signal Transient
($A_V = 1$, $C_L = 10,000\text{pF}$)



1352/53 G36

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1352/LT1353 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01 μF to 0.1 μF). For high drive current applications use low ESR bypass capacitors (1 μF to 10 μF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. If feedback resistors greater than 10k are used, a parallel capacitor of value, $C_F > (R_G)(C_{IN}/R_F)$, should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one and a large feedback resistor is used, C_F should be greater than or equal to C_{IN} . An example would be an I-to-V converter as shown in the Typical Applications section.

Capacitive Loading

The LT1352/LT1353 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Graphs of Frequency Response vs Capacitive Load, Capacitive Load Handling and the transient response photos clearly show these effects.

Input Considerations

Each of the LT1352/LT1353 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for

13523fa

APPLICATIONS INFORMATION

applications where DC accuracy must be maximized. The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. **The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs.** Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Circuit Operation

The LT1352/LT1353 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic.

The inputs are buffered by complementary NPN and PNP emitter followers which drive R1, a 1k resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node and compensation capacitor C_T . Complementary followers form an output stage which buffers the gain node from the load. The output devices Q19 and Q22 are connected to form a composite PNP and a composite NPN.

The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the high impedance node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step whereas the same output step in unity gain has a 10 times greater

input step. The graph Slew Rate vs Input Level illustrates this relationship. In higher gain configurations the large-signal performance and the small-signal performance both look like a single pole response.

Capacitive load compensation is provided by the R_C , C_C network which is bootstrapped across the output stage. When the amplifier is driving a light load the network has no effect. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier and a zero is created by the RC combination, both of which improve the phase margin. The design ensures that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1352/LT1353 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature of 150°C under certain conditions. Maximum junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

$$\text{LT1352CN8: } T_J = T_A + (P_D)(130^\circ\text{C/W})$$

$$\text{LT1352CS8: } T_J = T_A + (P_D)(190^\circ\text{C/W})$$

$$\text{LT1353CS: } T_J = T_A + (P_D)(150^\circ\text{C/W})$$

Worst-case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier $P_{D(\text{MAX})}$ is:

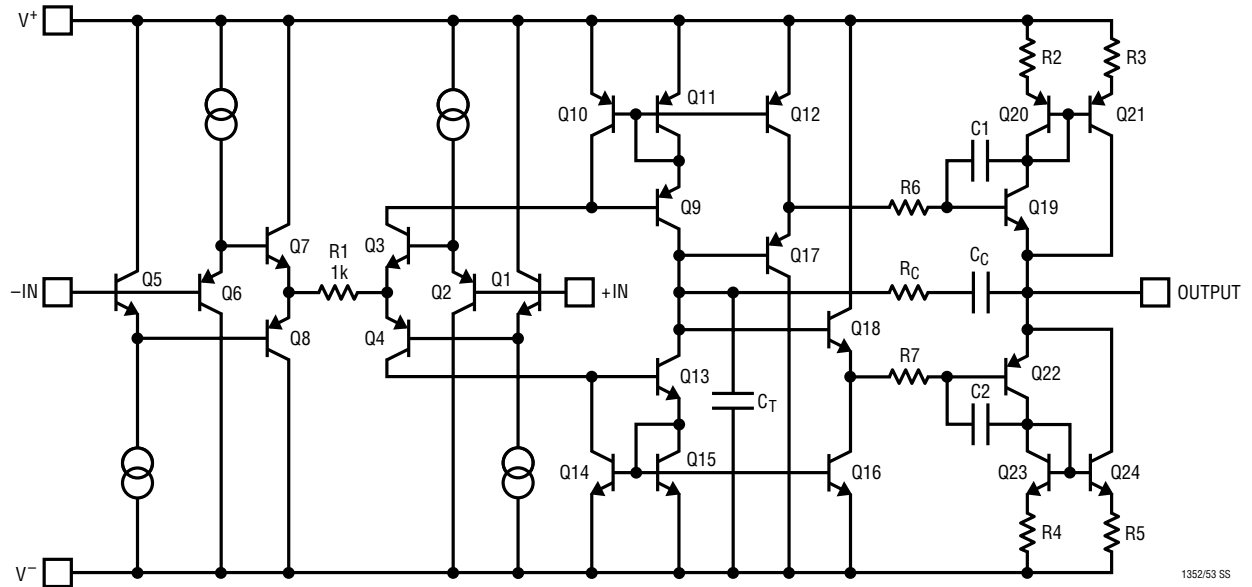
$$P_{D(\text{MAX})} = (V^+ - V^-)(I_{S(\text{MAX})}) + (V^+/2)^2/R_L \text{ or } (V^+ - V^-)(I_{S(\text{MAX})}) + (V^+ - V_{\text{MAX}})(I_{\text{MAX}})$$

Example: LT1353 in S14 at 85°C, $V_S = \pm 15\text{V}$, $R_L = 500\Omega$, $V_{\text{OUT}} = \pm 5\text{V}$ ($\pm 10\text{mA}$)

$$P_{D(\text{MAX})} = (30\text{V})(380\mu\text{A}) + (15\text{V} - 5\text{V})(10\text{mA}) = 111\text{mW}$$

$$T_J = 85^\circ\text{C} + (4)(111\text{mW})(150^\circ\text{C/W}) = 152^\circ\text{C}$$

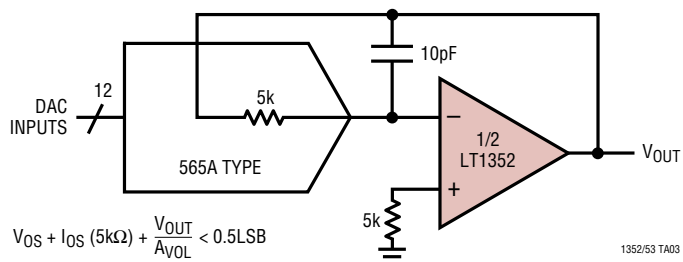
SIMPLIFIED SCHEMATIC



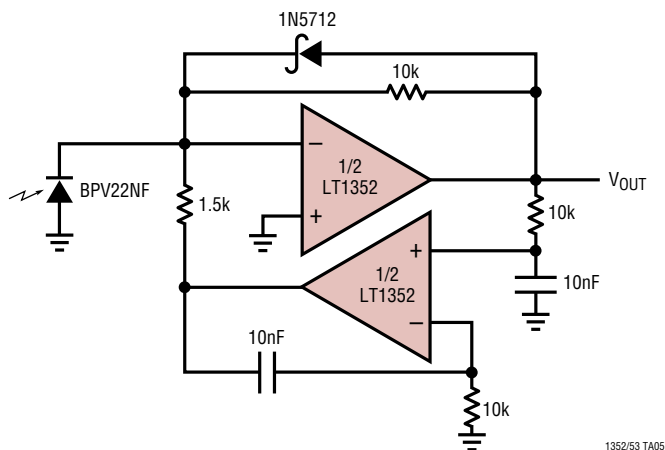
1352/53 SS

TYPICAL APPLICATIONS

DAC I-to-V Converter

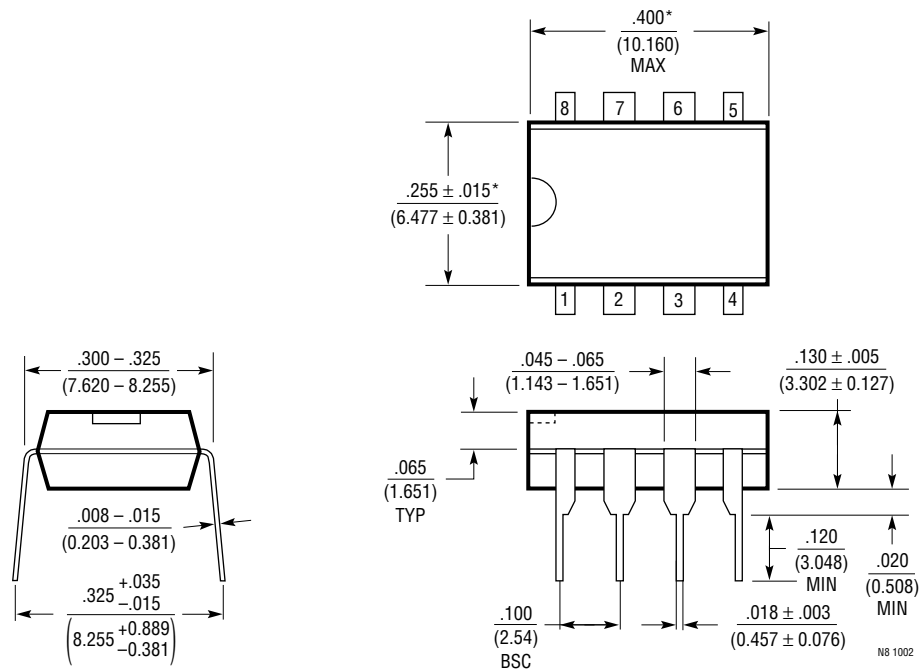


400kHz Photodiode Preamp with 10kHz Highpass Loop



PACKAGE DESCRIPTION

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)

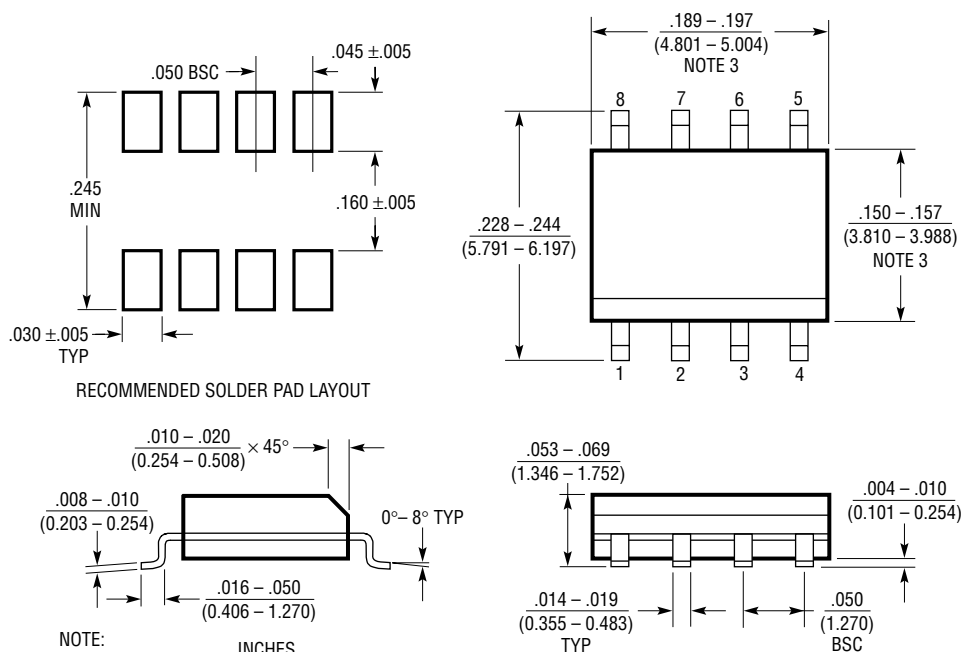


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

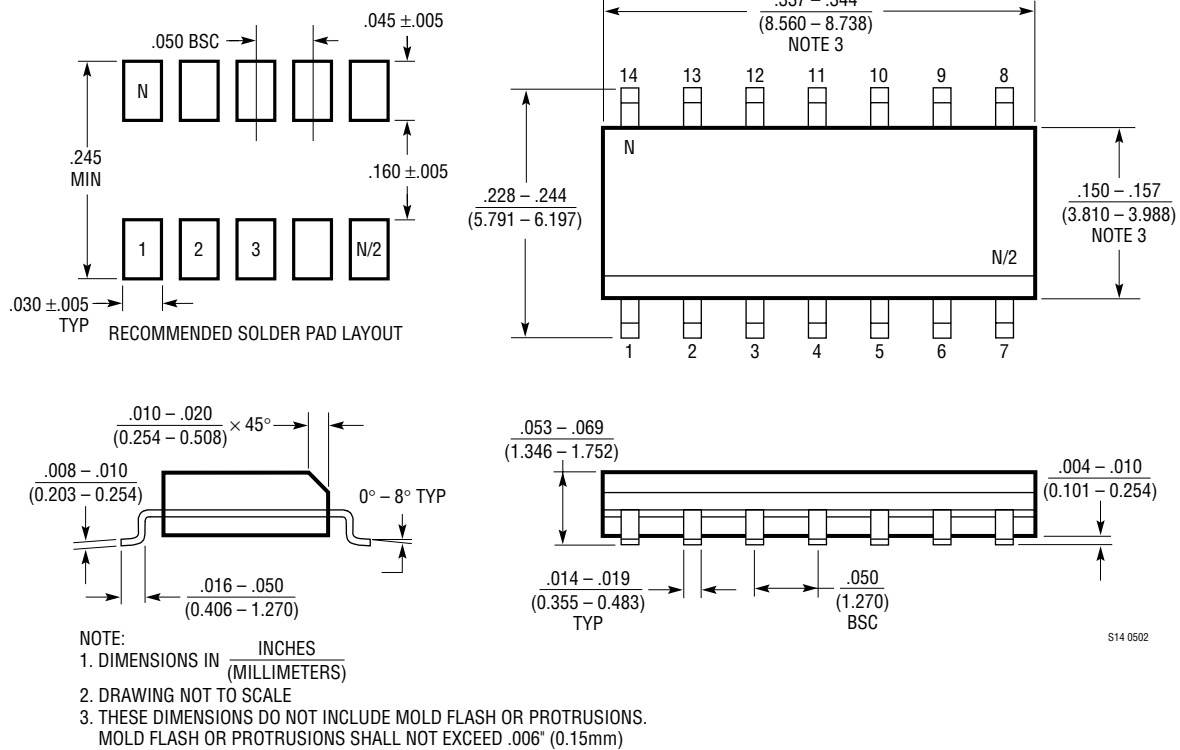


- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)

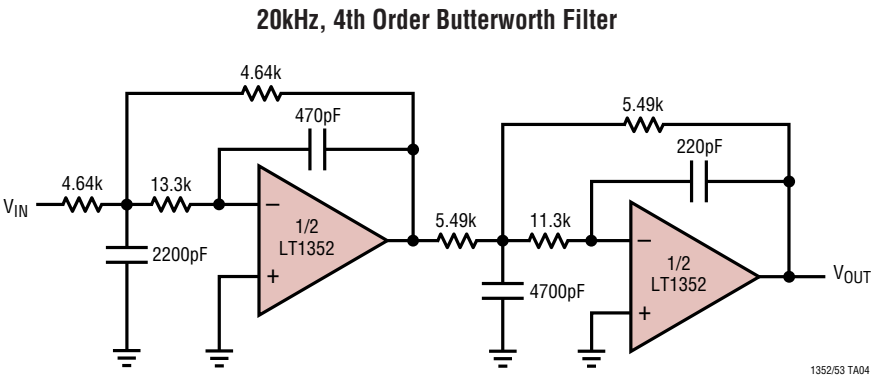
S08 0303

PACKAGE DESCRIPTION

S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



TYPICAL APPLICATIONS



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1351	250μA, 3MHz, 200V/μs Op Amp	Good DC Precision, C-Load Stable, Power Saving Shutdown
LT1354/55/56	Single/Dual/Quad 1mA, 12MHz, 400V/μs Op Amp	Good DC Precision, Stable with All Capacitive Loads