Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = V_{SS} P0= V_{SS}P2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Ratings min	Ratings typ	Ratings max	Unit
Maximum supply voltage	V_{DD} max	V_{DD}, V_{DD}P0, V_{DD}P1, V_{DD}P2	V_{DD}=V_{DD}P0= V_{DD}P1=V_{DD}P2		-0.3		+7.0	V
Input voltage	V_I	$\overline{RES}$, $\overline{CS}$, DIN, $\overline{CLK}$			-0.3		V_{DD}+0.3	
Output voltage	V_O	DOUT			-0.3		V_{DD}+0.3	
Input/output voltage	V_{IO}(1)	Port 0			-0.3		V_{DD}P0 +0.3	
	V_{IO}(2)	Port 1			-0.3		V_{DD}P1 +0.3	
	V_{IO}(3)	Port 2			-0.3		V_{DD}P2 +0.3	
High level output current								
Peak output current	IOPH(1)	Ports 0 to 2	CMOS output selected Per 1 applicable pin		-7			mA
	IOPH(2)	DOUT			-13			
Mean output current (Note 1)	IOMH(1)	Ports 0 to 2	CMOS output selected Per 1 applicable pin		-3			
	IOMH(2)	DOUT			-6			
Total output current	∑IOP0H	Port 0	Total of all applicable pins		-32			
	∑IOP1H	Port 1	Total of all applicable pins		-32			
	∑IOP2H	Port 2	Total of all applicable pins		-32			
	∑IOAH	DOUT, ports 0 to 1	Total of all applicable pins		-105			
Low level output current								
Peak output current	IOPL(1)	Ports 0 to 2	Per 1 applicable pin				16	mA
	IOPL(2)	DOUT					13	
Mean output current (Note 1)	IOML(1)	ports 0 to 2	Per 1 applicable pin				7	
	IOML(2)	DOUT					6	
Total output current	∑IOP0L	Port 0	Total of all applicable pins				32	
	∑IOP1L	Port 1	Total of all applicable pins				32	
	∑IOP2L	Port 2	Total of all applicable pins				32	
	∑IOAL	DOUT, ports 0 to 2	Total of all applicable pins				105	
Power dissipation	Pd max	MFP36SDJ	Ta=-30 to +70°C				330	mW
			Ta=-40 to +85°C				250	
Operating temperature	Topr				-40		85	°C
Storage temperature	Tstg				-55		125	

Note 1: The mean output current is a mean value measured over 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = -40 to +85°C, V_{SS} = V_{SS} P0= V_{SS}P2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification (Note 3)			Unit
				V_{DD}[V]	min	typ	max	
Operating supply voltage	V_{DD}(1)	V_{DD}			2.0		6.0	V
	V_{DD}(2)	V_{DD}P0	Supply voltage must be within V_{DD} (1)'s specification.		V_{DD}-3.0		V_{DD}	
	V_{DD}(3)	V_{DD}P1, V_{DD}P2	Supply voltage must be within V_{DD} (1)'s specification.		V_{DD}		V_{DD}+3.0	
High level input voltage	V_{IH}(1)	DIN, ports 0 to 2		4.5 to 6.0	0.3V_{DD}+0.7		V_{DD}Px	
	V_{IH}(2)	DIN, ports 0 to 2		2.0 to 6.0	0.3V_{DD}+0.7		V_{DD}Px	
	V_{IH}(3)	$\overline{RES}$, $\overline{CS}$, $\overline{CLK}$		4.5 to 6.0	0.4V_{DD}+0.7		V_{DD}	
	V_{IH}(4)	$\overline{RES}$, $\overline{CS}$, $\overline{CLK}$		2.0 to 6.0	0.4V_{DD}+0.7		V_{DD}	
Low level input voltage	V_{IL}(1)	DIN, ports 0 to 2		4.5 to 6.0	V_{SS}		0.2V_{DD}+0.1	
	V_{IL}(2)	DIN, ports 0 to 2		2.0 to 6.0	V_{SS}		0.2V_{DD}+0.1	
	V_{IL}(3)	$\overline{RES}$, $\overline{CS}$, $\overline{CLK}$		4.5 to 6.0	V_{SS}		0.1V_{DD}+0.2	
	V_{IL}(4)	$\overline{RES}$, $\overline{CS}$, $\overline{CLK}$		2.0 to 6.0	V_{SS}		0.1V_{DD}+0.2	

Note 3: V_{DD}Px denote the power supply pin (V_{DD}P0,V_{DD}P1,V_{DD}P2) for port pins.

Electrical Characteristics at Ta = -40 to +85°C, V_{SS} = V_{SS} P0= V_{SS}P2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	(Note 3)		Specification			Unit
				V_{DD}[V]	V_{DD}Px[V]	min	typ	max	
High level input current	I_{IH}	$\overline{RES}$, $\overline{CS}$, $\overline{CLK}$, Ports 0 to 2	V_{IN}=V_{DD} (including output Tr. off leakage current)	2.0 to 6.0				10	µA
Lower level input current	I_{IL}	$\overline{RES}$, $\overline{CS}$, $\overline{CLK}$, Ports 0 to 2	V_{IN}=V_{SS} (including output Tr. off leakage current)	2.0 to 6.0		-10			
High level output voltage	V_{OH}(1)	Ports 0	I_{OH}=-2mA	2.0 to 6.0	4.5 to 6.0	V_{DD}Px-0.5			V
	V_{OH}(2)		I_{OH}=-5mA	2.0 to 6.0	4.5 to 6.0	V_{DD}Px-1.0			
	V_{OH}(3)		I_{OH}=-1mA	2.0 to 6.0	2.0 to 6.0	V_{DD}Px-0.5			
	V_{OH}(4)	Ports 1	I_{OH}=-2mA	2.0 to 6.0	4.5 to 6.0	V_{DD}Px-0.5			
	V_{OH}(5)		I_{OH}=-5mA	2.0 to 6.0	4.5 to 6.0	V_{DD}Px-1.0			
	V_{OH}(6)		I_{OH}=-1mA	2.0 to 6.0	2.0 to 6.0	V_{DD}Px-0.5			
	V_{OH}(7)	DOUT	I_{OH}=-5mA	4.5 to 6.0		V_{DD}Px-0.5			
	V_{OH}(8)		I_{OH}=-10mA	4.5 to 6.0		V_{DD}Px-1.0			
	V_{OH}(9)		I_{OH}=-2mA	2.0 to 6.0		V_{DD}Px-0.5			
Lower level output voltage	V_{OL}(1)	Ports 0	I_{OL}=5mA	4.5 to 6.0	2.0 to 6.0			0.4	
	V_{OL}(2)		I_{OL}=12mA	4.5 to 6.0	2.0 to 6.0			1	
	V_{OL}(3)		I_{OL}=2mA	2.0 to 6.0	2.0 to 6.0			0.4	
	V_{OL}(4)	Ports 1,2	I_{OL}=5mA	4.5 to 6.0	4.5 to 6.0			0.4	
	V_{OL}(5)		I_{OL}=12mA	4.5 to 6.0	4.5 to 6.0			1	
	V_{OL}(6)		I_{OL}=2mA	2.0 to 6.0	2.0 to 6.0			0.4	
	V_{OL}(7)	DOUT	I_{OL}=5mA	4.5 to 6.0				0.4	
	V_{OL}(8)		I_{OL}=10mA	4.5 to 6.0				1	
	V_{OL}(9)		I_{OL}=2mA	2.0 to 6.0				0.4	
Pull-up resistance	Rpu(1)	$\overline{CS}$	V_{OH}=V_{SS}	4.5 to 6.0		100	230	650	kΩ
Voltage hysteresis	VHIS	$\overline{RES}$, $\overline{CS}$, $\overline{CLK}$		2.0 to 6.0			0.1V_{DD}		V
Consumption current (operation stopped)	IDDSP	V_{DD}=V_{DD}P0= V_{DD}P1=V_{DD}P2	$\overline{RES}$=$\overline{CS}$=V_{DD} $\overline{CLK}$=DIN=V_{DD} or V_{SS} DOUT=open P0 to P2=open or V_{DD} or V_{SS} (Note 2)	2.0 to 6.0				20	µA
Pin capacity	CP	All pins	Other than test pin V_{IN}=V_{SS} f=1MHz Ta=25°C	2.0 to 6.0			10		pF

Note 2: The consumption current does not include the current flowing into the port's output transistor.
Note 3: V_{DD}Px denote the power supply pin (V_{DD}P0,V_{DD}P1,V_{DD}P2) for port pins.

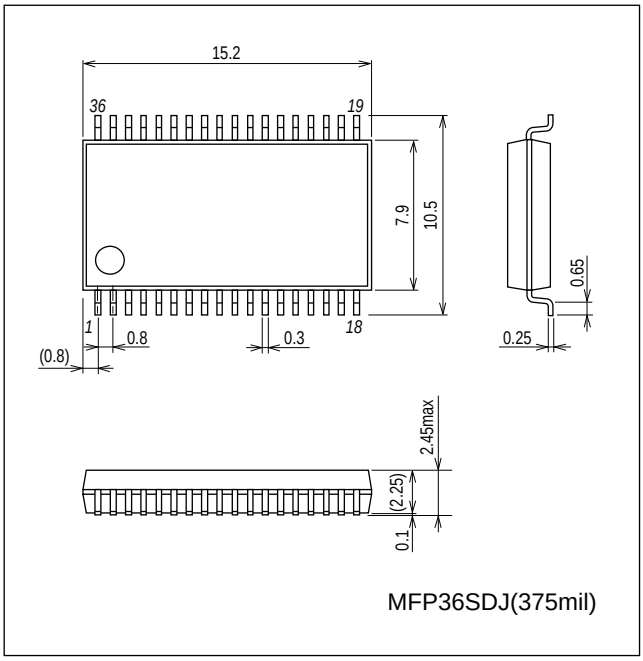
Switching I/O Characteristics at Ta=-40 to +85°C, $V_{DD}=V_{DD}P0=V_{DD}P1=V_{DD}P2$, $V_{SS}=V_{SS}P0=V_{SS}P1=V_{SS}P2$, $V_{SS}=0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			Unit
				V_{DD}[V]	min	typ	max	
Clock setup time	TsCLK	$\overline{CS}$, $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$. •See Fig. 9.	2.0 to 6.0	100			ns
Chip select low level setup time	TslCS	$\overline{CS}$, $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$. •See Fig. 9.	2.0 to 6.0	100			
Chip select low level hold time	ThlCS	$\overline{CS}$, $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$. •See Fig. 9.	2.0 to 6.0	100			
Clock hold time	ThCLK	$\overline{CS}$, $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$. •See Fig. 9.	2.0 to 6.0	200			
Clock low level pulse width	TwlCLK	$\overline{CLK}$	•See Fig. 9.	4.5 to 6.0	250			
				2.7 to 6.0	500			
				2.0 to 6.0	1000			
Clock high level pulse width	TwhCLK	$\overline{CLK}$	•See Fig. 9.	4.5 to 6.0	250			
				2.7 to 6.0	500			
				2.0 to 6.0	1000			
Chip select high level setup time	TshCS	$\overline{CS}$, $\overline{RES}$	•See Fig. 9.	2.0 to 6.0	200			
Chip select high level hold time	ThhCS	$\overline{CS}$, $\overline{RES}$	•See Fig. 9.	2.0 to 6.0	100			
Chip select low level pulse width	TwlCS	$\overline{CS}$, $\overline{RES}$	•See Fig. 9.	2.0 to 6.0	200			
Reset low level pulse width	TwlRES	$\overline{CS}$, $\overline{RES}$	•See Fig. 9.	2.0 to 6.0	150			
Data setup time	TsDIN	DIN	•Specified with respect to falling edge of $\overline{CLK}$. •See Fig. 9.	4.5 to 6.0	30			
				2.0 to 6.0	50			
Data hold time	ThDIN	DIN	•Specified with respect to falling edge of $\overline{CLK}$. •See Fig. 9.	4.5 to 6.0	50			
				2.7 to 6.0	150			
				2.0 to 6.0	300			
Serial data output delay time (Note 4)	TdD0UT	DOUT	•Specified with respect to falling edge of $\overline{CLK}$. •See Fig. 9.	4.5 to 6.0			200	
				2.7 to 6.0			400	
				2.0 to 6.0			800	
Port data output delay time	TdPOUT	Port 0 to 2	•Specified with respect to rising edge of $\overline{CS}$. •See Fig. 9.	4.5 to 6.0			200	
				2.7 to 6.0			400	
				2.0 to 6.0			800	
Port data input setup time	TsPIN	Port 0 to 2	•Specified with respect to rising edge of $\overline{CLK}$. •See Fig. 9.	4.5 to 6.0	30			
				2.0 to 6.0	50			
Port data input hold time	ThPIN	Port 0 to 2	•Specified with respect to rising edge of $\overline{CLK}$. •See Fig. 9.	4.5 to 6.0	50			
				2.7 to 6.0	150			
				2.0 to 6.0	300			

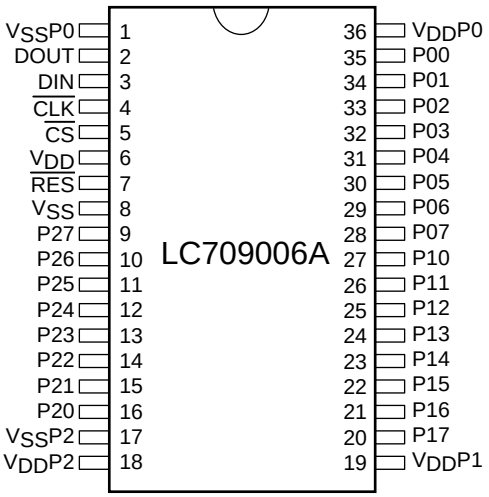
Note 4: The input data of P00 will be out from DOUT terminal at the first negative edge of $\overline{CLK}$ signal. Because of this, Serial data output delay time of the first clock will be the time measured from the negative edge of the $\overline{CLK}$ or the time at the input data (P00) is settled.

Package Dimensions

unit : mm (typ)
3263

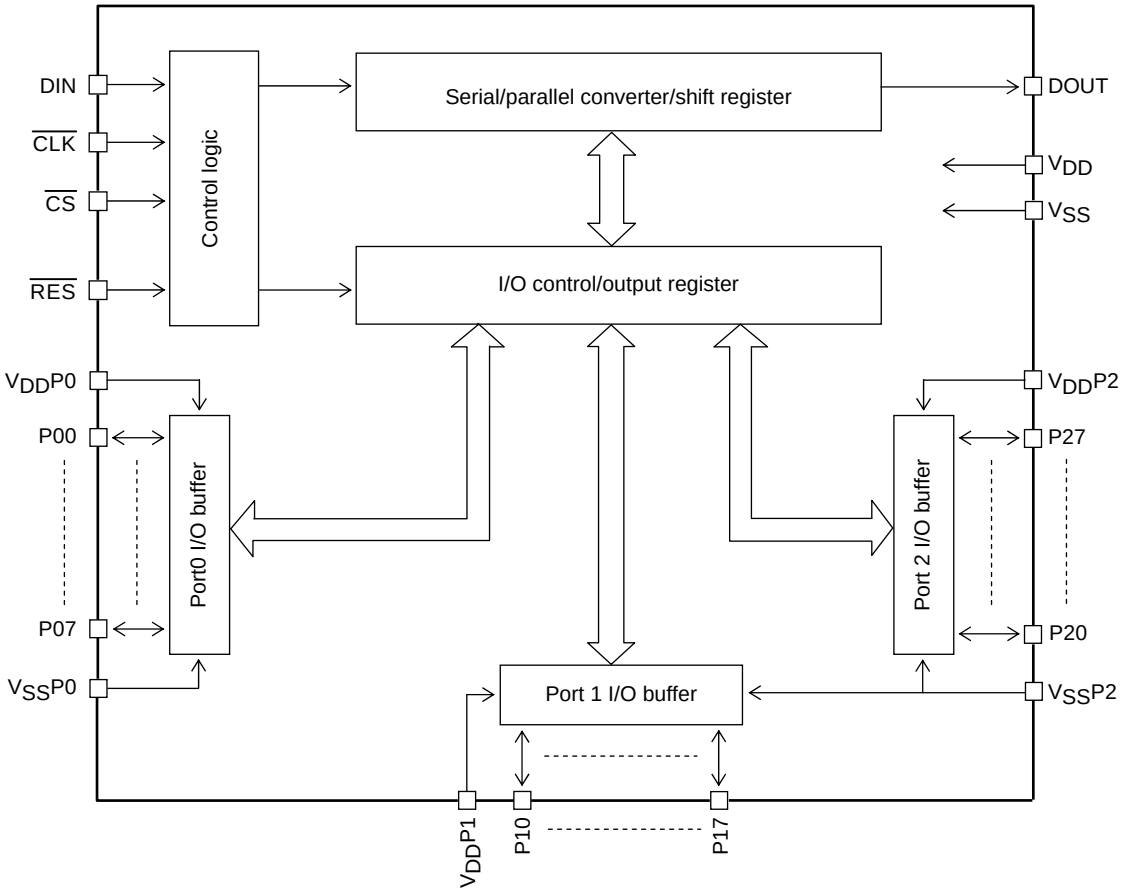


Pin Assignment



Top view

Block Diagram



Pin Description

Pin Name	I/O	Description	I/O Type	Reset Time
V_{SS} $V_{SS}P0$ $V_{SS}P2$	-	• - power supply pin • V_{SS} is the power supply pin for blocks other than I/O ports (P00 to P27). • $V_{SS}P0$ is the power supply pin for port pins P00 to P07. • $V_{SS}P2$ is the power supply pin for port pins P10 to P17 and P20 to P27.		
V_{DD} $V_{DD}P0$ $V_{DD}P1$ $V_{DD}P2$	-	• + power supply pin • V_{DD} is the power supply pin for blocks other than I/O ports (P00 to P27). • $V_{DD}P0$ is the power supply pin for port pins P00 to P07. • $V_{DD}P1$ is the power supply pin for port pins P10 to P17. • $V_{DD}P2$ is the power supply pin for port pins P20 to P27. (Notes) • $V_{DD}P0$ must not be set higher than V_{DD} l ($V_{DD}P0 \leq V_{DD}$). • $V_{DD}P1$ must not be set lower than V_{DD} ($V_{DD}P1 \geq V_{DD}$). • $V_{DD}P2$ must not be set lower than V_{DD} ($V_{DD}P2 \geq V_{DD}$).		
Port 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 1 bit units. • CMOS/Nch-open drain specifiable in 1 bit units. • Output voltage variable in 1 port units according to $V_{DD}P0$ voltage.	Output: CMOS/Nch-OD Input: TTL	Hi-Z
Port 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1 bit units. • CMOS/Nch-open drain specifiable in 1 bit units. • Output voltage variable in 1 port units according to $V_{DD}P1$ voltage.	Output: CMOS/Nch-OD Input: TTL	Hi-Z
Port 2 P20 to P27	I/O	• 8-bit I/O port • I/O specifiable in 1 bit units. • CMOS/Nch-open drain specifiable in 1 bit units. • Output voltage variable in 1 port units according to $V_{DD}P2$ voltage.	Output: CMOS/Nch-OD Input: TTL	Hi-Z

Continued on next page.

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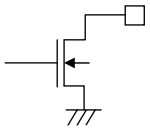
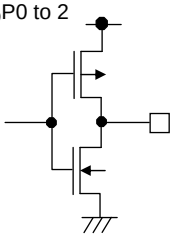
Pin Name	I/O	Description	I/O Type	Reset Time
DIN	I	• Serial data input pin	Input: TTL	
DOUT	O	• Serial data output pin	Output: CMOS	High
$\overline{CLK}$	I	• Serial clock input pin • Port data is placed on DOUT on the falling edge of this clock. • The data from DIN is latched on the negative-to-positive transition of this clock.	Input: TTL Schmidt	
$\overline{CS}$	I	• Chip select input pin • Setting this pin to the low level enables serial data to be input or output.	Input: TTL Schmidt	
$\overline{RES}$	I	• Device's system reset input pin • Setting this pin to the low level initializes the internal control circuit and registers and puts DOUT in the high level and all data port pins (P00 to P27) into the Hi-Z state.	Input: TTL Schmidt	

Port Output Types and I/O States

The output type and I/O states of the LC709006A's ports can be selected by configuring the data direction register (DDR) and data register (DTR). Port data can be taken into the LC709006A only when DDR is set to 0 (Nch-open drain) and DTR is set to 1 (Nch-Tr OFF). The ports are held high for the other settings of DDR and DTR.

Port Name	DDR	DTR	Port		
			Output Type	Input	Output
P00 to P07 P10 to P17 P20 to P27	0	1	Nch-open drain	Enabled	Hi-Z
	0	0	Nch-open drain	Disabled (High)	Low
	1	1	CMOS	Disabled (High)	High
	1	0	CMOS	Disabled (High)	Low

Port Output Circuit

Nch-open drain	CMOS
	V_{DD} P0 to 2 

Principles of Operation

The LC709006A accomplishes data transmission and reception to and from the MCU through synchronous serial communication and performs I/O operations on the extended ports in parallel mode. Its communication modes (MCU to LC709006A by serial to parallel conversion and LC709006A to MCU by parallel to serial conversion) include the initial communication modes (modes 0 and 1) in which the LC709006A initializes itself and the data communication mode in which the LC709006A sends and receives port data. The initial communication modes are used for various communication control purposes for the first time in system operation after a power-on or system reset. In these modes, the LC709006A sets up the I/O mode and output type of the ports. The data communication mode is used for communication control after the end of the initial communication modes. In this mode, the LC709006A carries out actual port I/O operations. The port I/O mode and output type settings are stored in the data direction register (DDR). The data output state settings ("High" output, "Hi-Z" output, or "Low" output) are stored in the data register (DTR). The LC709006A's operating modes are summarized below, followed by detailed mode descriptions.

Communication Mode		Description
Initial communication mode	Mode 0	Sets the output type of all ports to "N-ch-open drain."
	Mode 1	Sets the I/O direction of the ports and the their output type to CMOS or "Nch-open-drain" on a bit basis.
Data communication mode		Sends and receives port data.

(1) Initial communication modes

• Mode 0

1) Setting the $\overline{RES}$ pin to the low level initializes the system, sets the DOUT pin to the high level, and sets the DDR register of all ports to 0 and the DTR register to 1. The output type of the ports is set to Nch-open drain and their I/O state (Nch-Tr=OFF) to the "Hi-Z" (input mode) state.
2) When the $\overline{RES}$ pin is set high (reset) and the $\overline{CS}$ pin is set and held low for a certain period (TwlCS), the DDR is fixed at 0. Subsequently, the LC709006A is placed in the data communication mode.

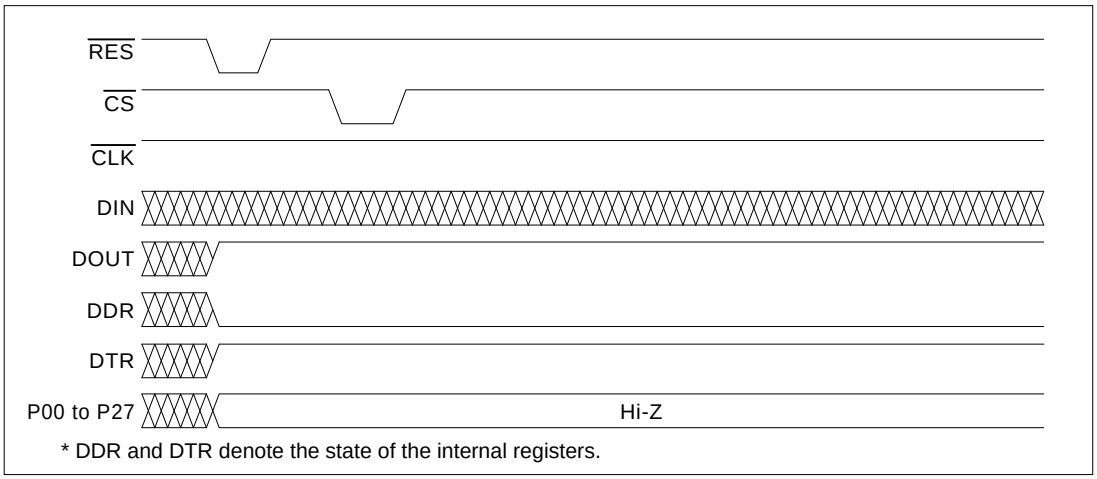


Fig. 1

• Mode 1

1) When the $\overline{RES}$ pin is set to the low level, the LC709006A initializes the system, sets the DOUT pin to the high level, and sets the DDR register of all ports to 0 and the DTR register to 1. The output type of the ports is set to Nch-open drain and their I/O state (Nch-Tr=OFF) to the "Hi-Z" (input mode) state.
2) When the $\overline{RES}$ pins is set high (reset) and the $\overline{CS}$ pin is set low, the LC709006A gets ready for serial communication.
3) The input data at P00 is sent directly to the DOUT pin on the first falling edge of the transmission clock signal $\overline{CLK}$. The data at pins P01 to P27 is loaded into the shift register on the rising edge of the next clock.
4) Subsequently, the ports' input data, which is loaded into the shift register on the falling edge of $\overline{CLK}$, is placed at the DOUT pin sequentially (P00→P07, P20→P27) in synchronization with the falling edges of $\overline{CLK}$, starting at port pin P00. In parallel with this operation, when data to be placed at the ports is supplied to the DIN pin sequentially starting at the port pin P00 (P00→P07, P10→P17, P20→P27), it is loaded into the internal shift register in synchronization with the rising edges of $\overline{CLK}$.
5) When the $\overline{CS}$ pin is set high after the rising edge of the 24th clock, the data loaded in the shift register is loaded into the DDR register which determines the I/O mode and output type of the data (serial data is loaded into the DDR register after a reset is effected). Subsequently, the LC709006A controls serial data transmission and reception in the data communication mode.

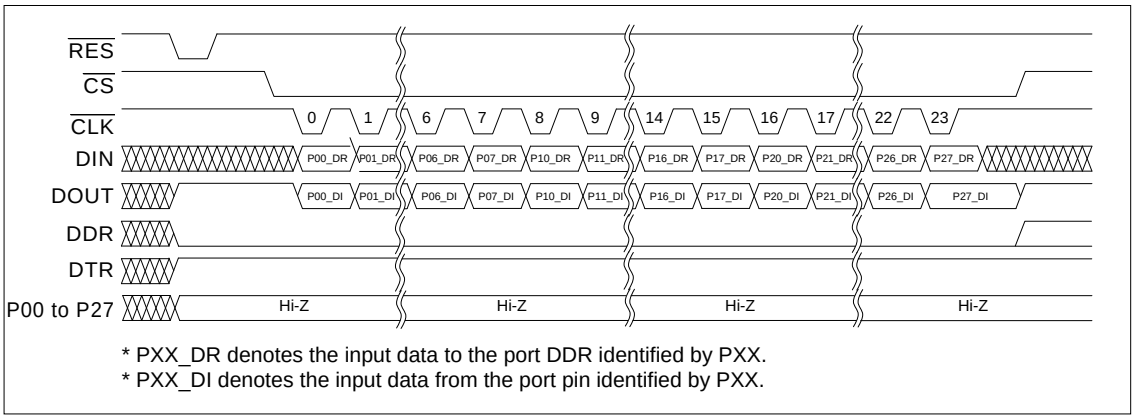


Fig. 2

(2) Data communication mode

1) When the $\overline{CS}$ pin is set low with the $\overline{RES}$ pin held high, the LC709006A gets ready for serial communication. (Subsequently, processing in steps 2) and 3) are identical to steps 2) and 3) in paragraph (1)-2).
2) The input data at P00 is sent directly to the DOUT pin on the first falling edge of the $\overline{CLK}$ signal. Data at pins P01 to P27 is loaded into the shift register on the next rising edge of the clock.
3) Subsequently, the ports' input data, which is loaded into the shift register on the falling edge of $\overline{CLK}$, is placed at the DOUT pin sequentially (P00→P07, P10→P17, P20→P27) in synchronization with the falling edges of $\overline{CLK}$, starting at port pin P00. In parallel with this operation, when data to be placed at the ports is supplied to the DIN pin sequentially starting at the port pin P00 (P00→P07, P10→P17, P20→P27), it is loaded into the internal shift register in synchronization with the rising edges of $\overline{CLK}$.
4) When the $\overline{CS}$ pin is set high after the rising edge of the 24th clock, the data loaded in the shift register is loaded into the DDR register which determines the output state of the ports and the states of all port pins (P00 to P27) are then changed (output) according to the conditions established in the DDR and DTR registers. Serial data that occurs following the initial communication mode processing is always loaded into the DTR register.

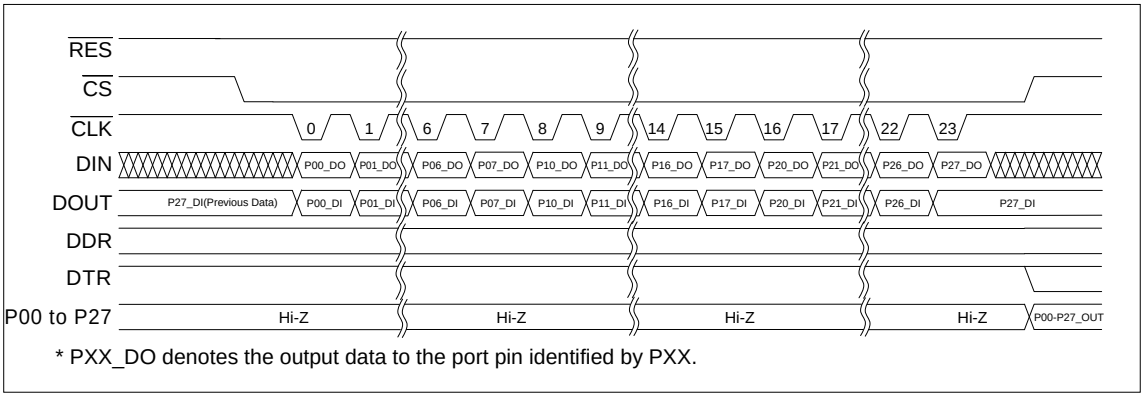


Fig. 3

5) Subsequently, the state of all port pins (P00 to P27) is updated each time the set of steps 1) to 4) described in paragraph (2) are performed.

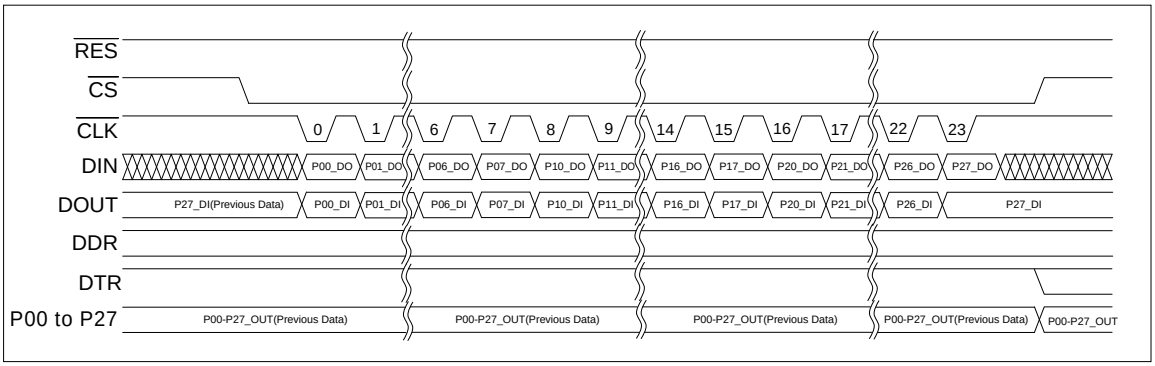


Fig. 4

Note: Connect a Pull-up resister (about 100kΩ) to $\overline{CS}$ using MCU V_{DD}.

Application Examples

(1) Example of a cascade configuration

Two or more LC709006A LSI chips can be cascaded to realize port expansion beyond 24 bits. Port expansion, however, need to be made in units of 24 bits × n (n denotes the number of LSI chips).

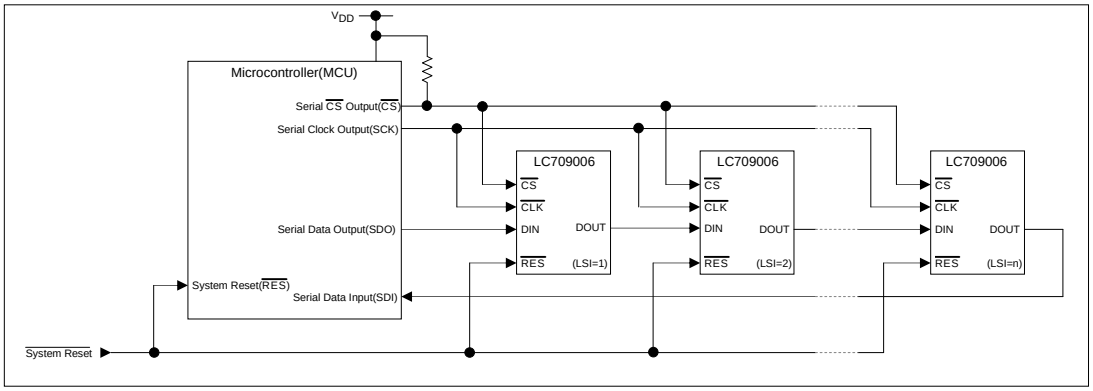


Fig. 5

(2) Variable port power level example

When controlling the level of I/O ports according to the power voltage level of the peripheral equipment, the user can connect the output from the power supply of the peripheral equipment directly to the power supply pins for the I/O ports. The LC709006A dispenses with the need to add an external level shifter circuit.

Note the following when configuring the LC709006A in this way:

Note 5:

- $V_{DD}P0$: The voltage level of $V_{DD}P0$ must not be higher than that of V_{DD} ($V_{DD}P0 \leq V_{DD}$).
- $V_{DD}P1$: The voltage level of $V_{DD}P1$ must not be lower than that of V_{DD} ($V_{DD}P1 \geq V_{DD}$).
- $V_{DD}P2$: The voltage level of $V_{DD}P2$ must not be lower than that of V_{DD} ($V_{DD}P2 \geq V_{DD}$).
- The input level of all ports (P00 to P27) is dependent on the V_{DD} power source; it depends on none of the power sources $V_{DD}P0$ to $V_{DD}P2$.

* Be sure to check the electrical characteristics of the LC709006A.

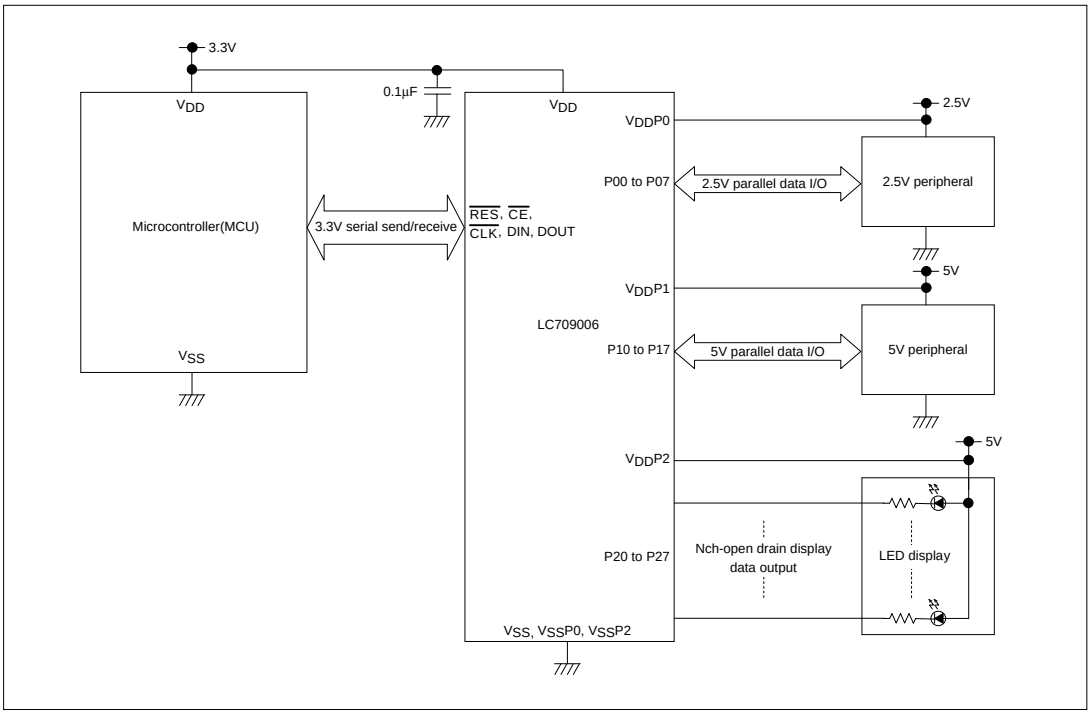


Fig. 6

Example of Placing Bypass Capacitors between V_{DD} and V_{SS} Terminals

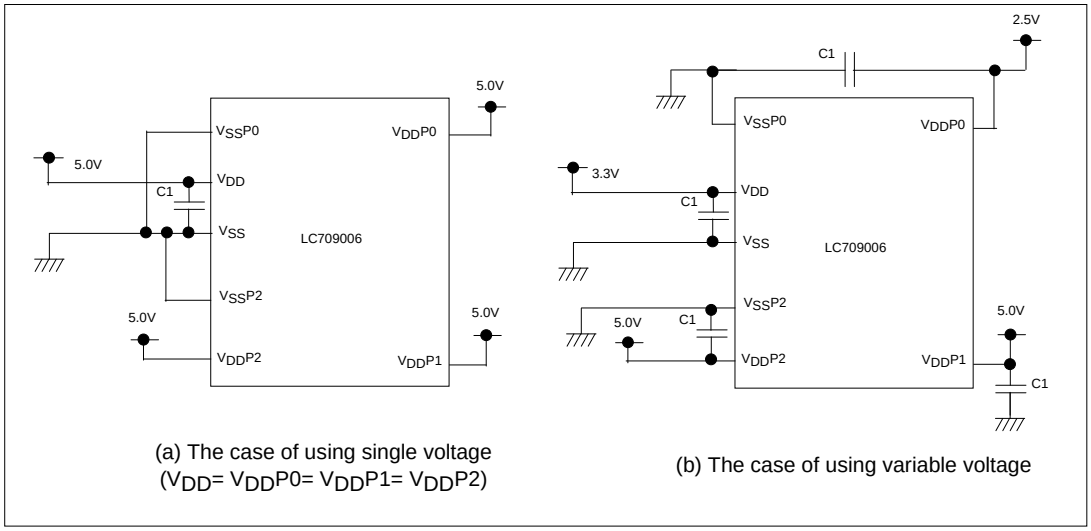
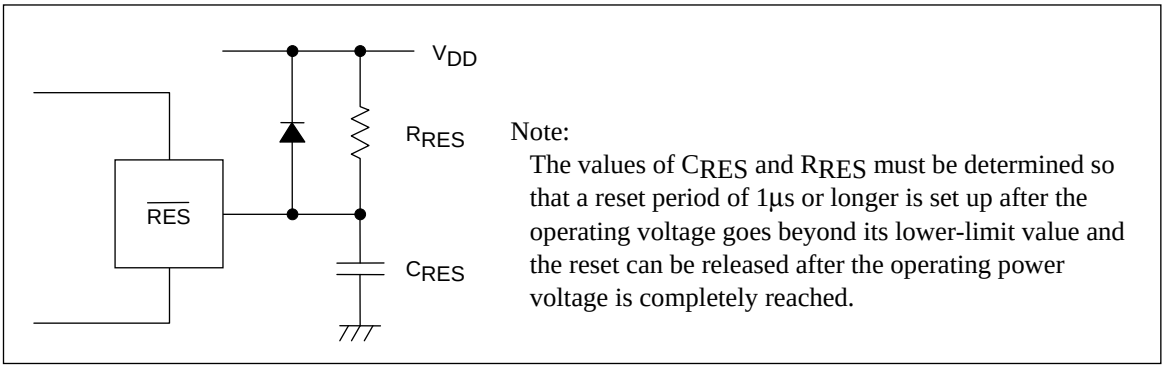


Fig. 7

In the case of using single voltage source as showing in the Fig.7 (a), you must connect a bypass capacitor (C1, about 0.1µF) between V_{DD} and V_{SS}. When connecting the capacitor (C1) and V_{DD}-V_{SS}, use a thick wire, and try to make its length as short as possible: moreover, try to make the impedance of V_{DD}-C1 and V_{SS}-C1 equal.
In addition, when using several voltage sources as showing in the Fig.7 (b), it is suggested to connect the bypass capacitor to each set of the voltage terminals.



Note:
The values of C_{RES} and R_{RES} must be determined so that a reset period of 1µs or longer is set up after the operating voltage goes beyond its lower-limit value and the reset can be released after the operating power voltage is completely reached.

Fig. 8: Reset Circuit

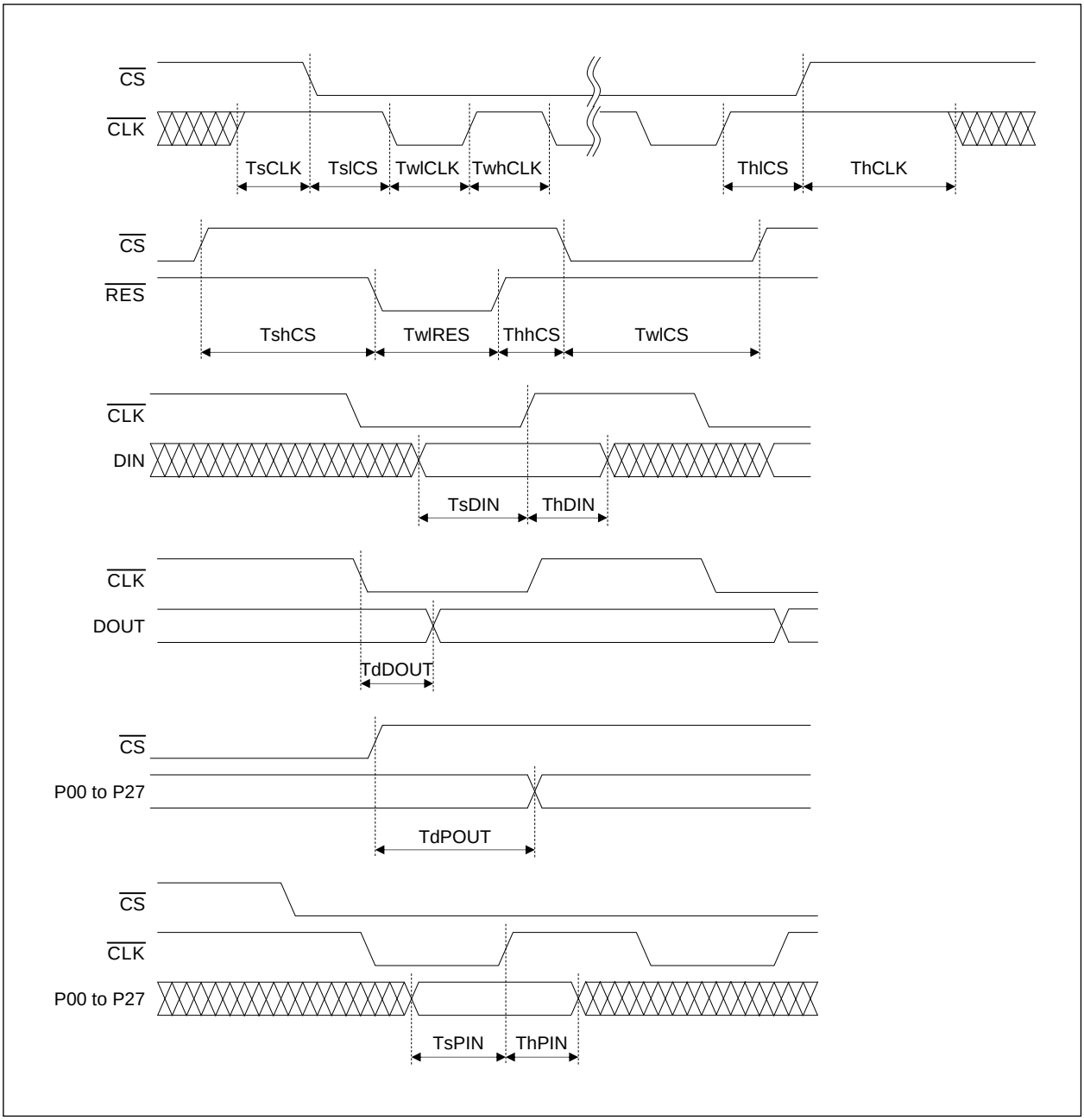


Fig. 9: Serial I/O and Parallel Data I/O Timing Diagram