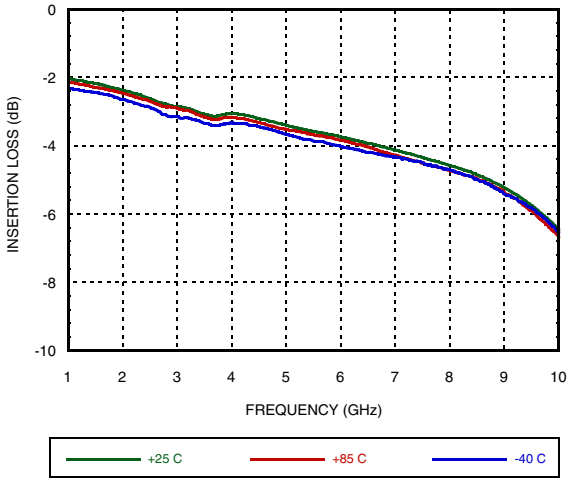
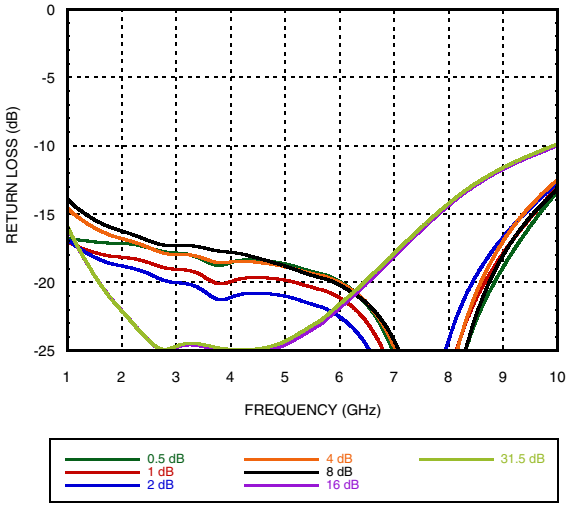
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 2.2 - 8.0 GHz

Insertion Loss



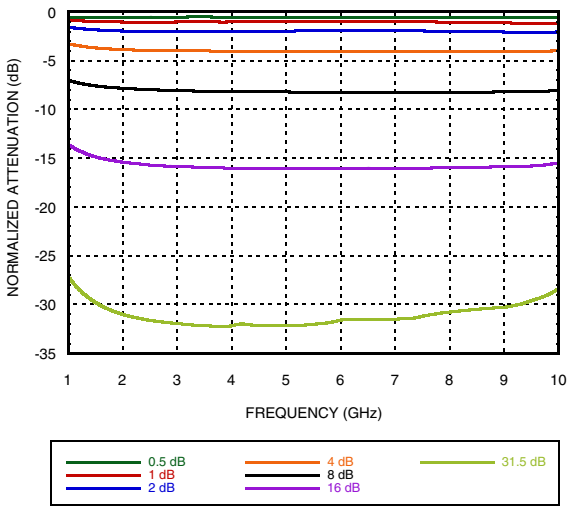
Return Loss RF1, RF2

(Only Major States are Shown)

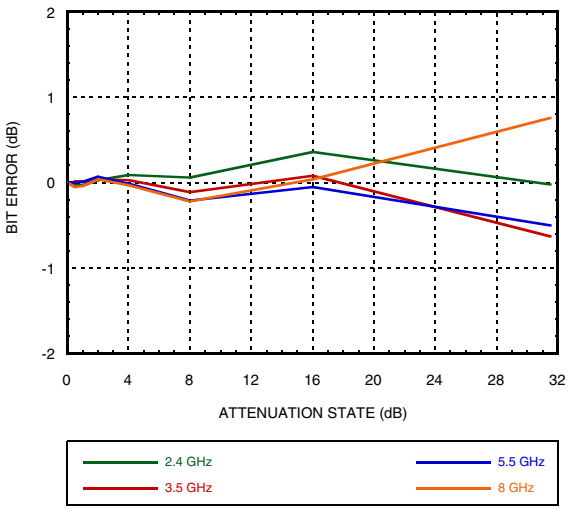


Normalized Attenuation

(Only Major States are Shown)

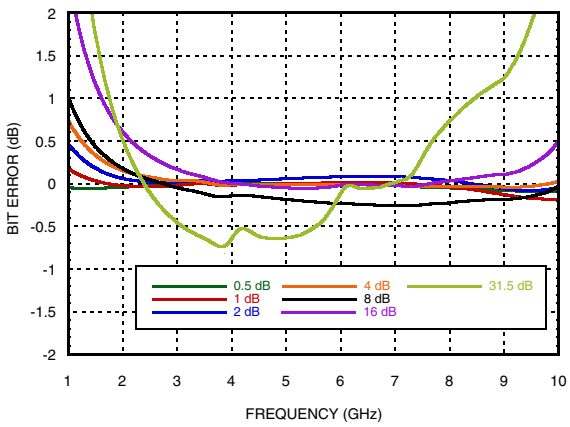


Bit Error vs. Attenuation State



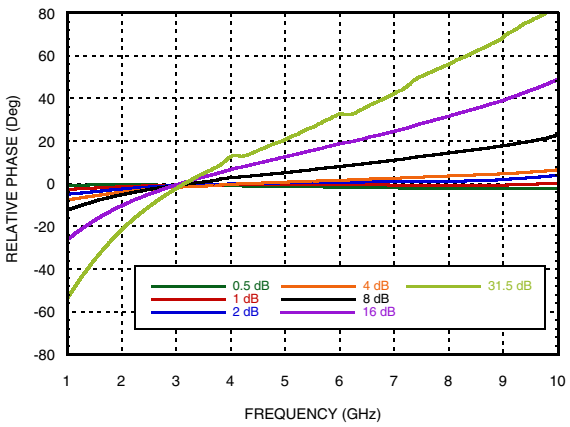
Bit Error vs. Frequency

(Only Major States are Shown)



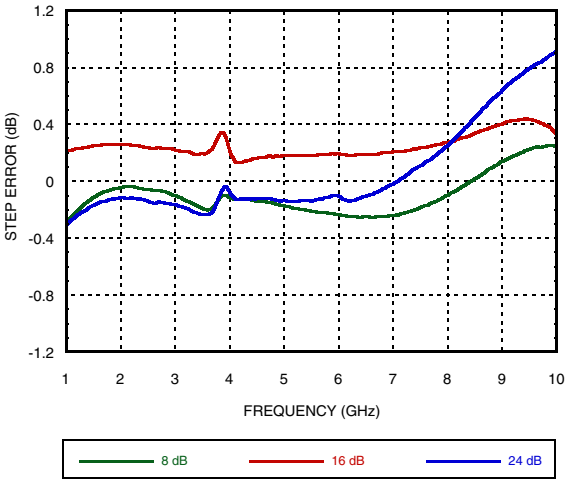
Relative Phase vs. Frequency

(Only Major States are Shown)

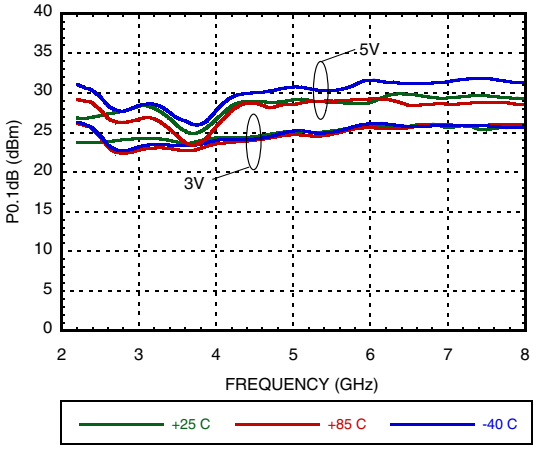


0.5 dB LSB GaAs MMIC 6-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 2.2 - 8.0 GHz

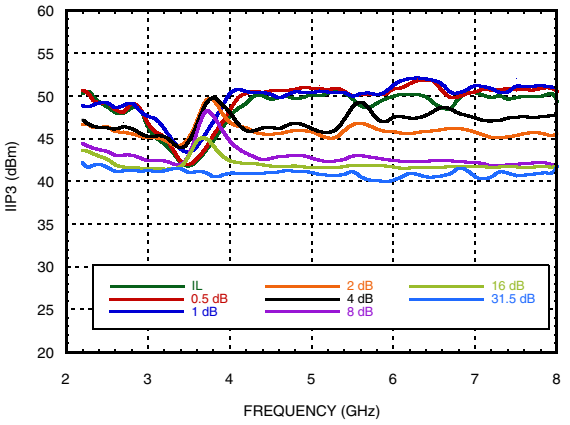
Worst Case Step Error Between Successive Attenuation States



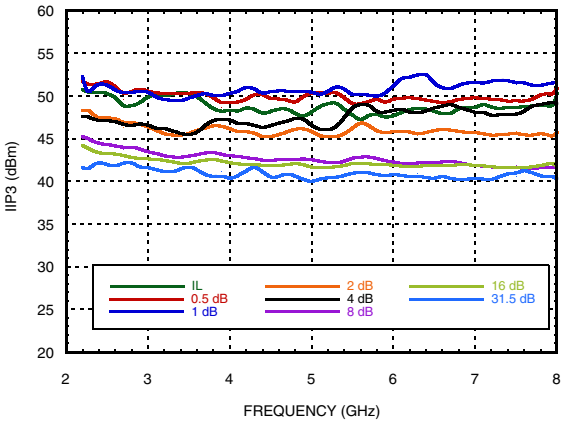
P0.1dB vs. Temprature, IL State



IIP3 vs. Frequency at VDD=3V



IIP3 vs. Frequency at VDD=5V



Truth Table

Control Voltage Input						Attenuation State RF1 - RF2
V1 16 dB	V2 8 dB	V3 4 dB	V4 2 dB	V5 1 dB	V6 0.5 dB	
High	High	High	High	High	High	Reference I.L.
High	High	High	High	High	Low	0.5 dB
High	High	High	High	Low	High	1 dB
High	High	High	Low	High	High	2 dB
High	High	Low	High	High	High	4 dB
High	Low	High	High	High	High	8 dB
Low	High	High	High	High	High	16 dB
Low	Low	Low	Low	Low	Low	31.5 dB

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

Bias Voltage & Current

VDD Range = +3.0 V to +5.0 V	
VDD (Vdc)	IDD (Typ.)
+3.0 V	10 µA
+5.0 V	30 µA

Control Voltage

State	Bias Condition
Low	0 to 0.2V at 10 µA Typ.
High	VDD ± 0.2V at 5 µA Typ.

Note: VDD = +3V to +5V

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 2.2 - 8.0 GHz

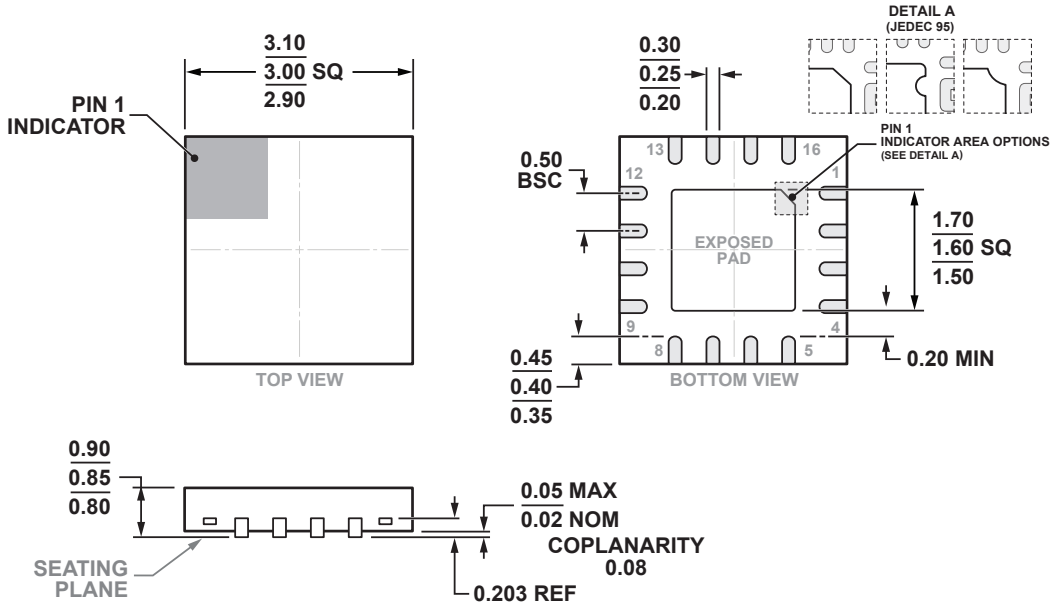
Absolute Maximum Ratings

Control Voltage (V1 to V6)	VDD +0.5 Vdc
Supply Voltage (VDD)	+7.0 Vdc
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
RF Input Power (2.2 - 8.0 GHz)	+27 dBm
ESD Sensitivity (HBM)	Class 1A
ESD Sensitivity (FICDM)	Class IV

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing

**16-Lead Lead Frame Chip Scale Package [LFCSP
3 x 3 mm Body and 0.85 mm Package Height
(CP-16-50)
Dimensions shown in millimeters**



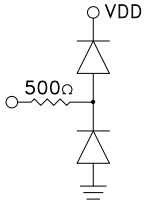
COMPLIANT TO JEDEC STANDARDS MO-220-VEED-4

Package Information

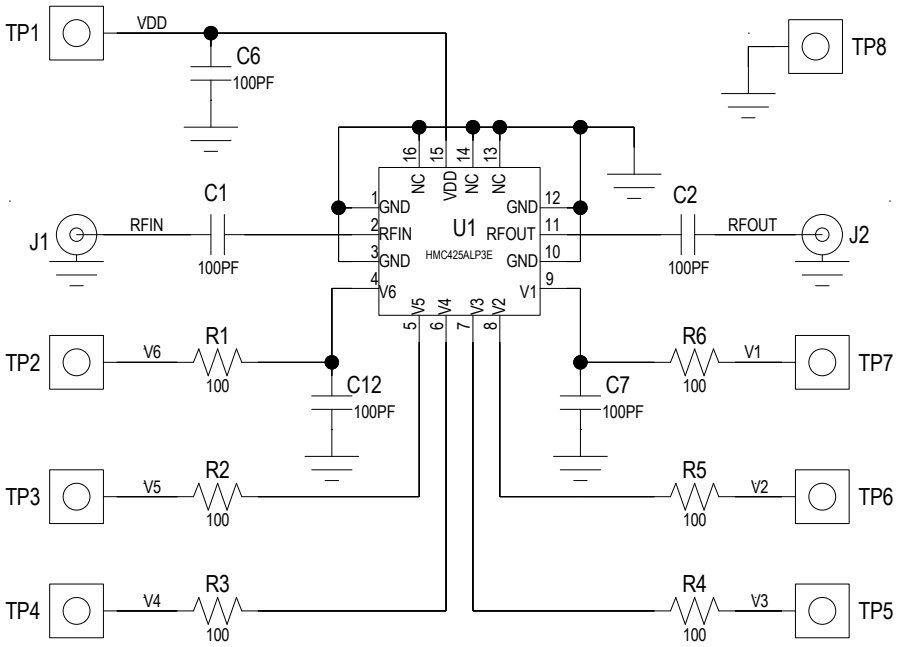
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC425ALP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% Matte Sn	MSL3 [1]	H425A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

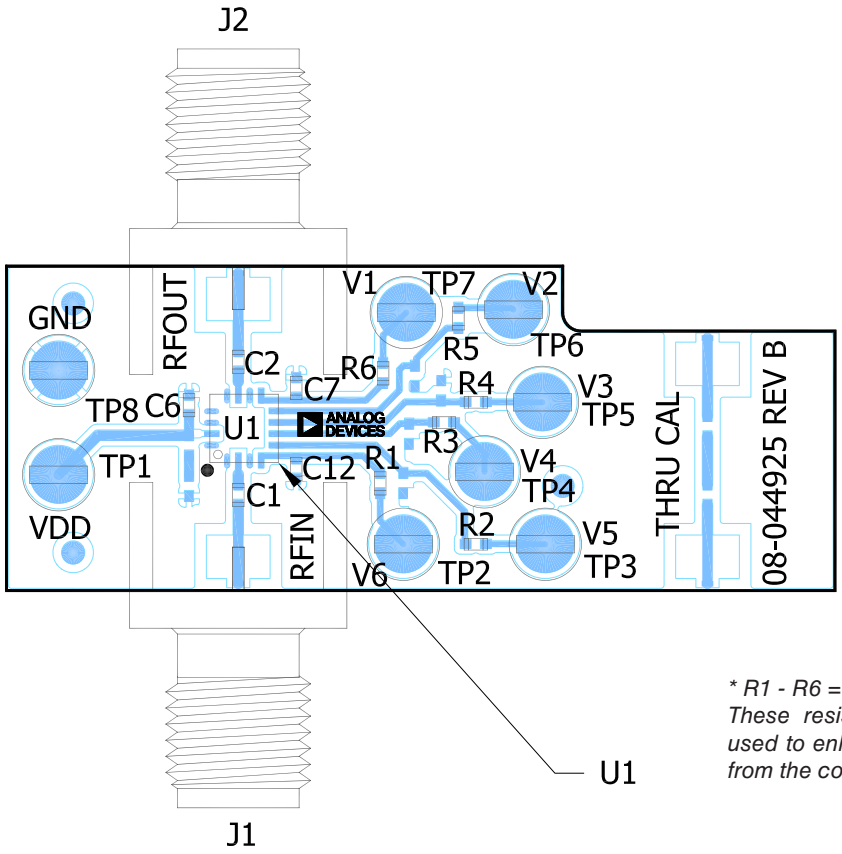
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 10, 12	GND	Package bottom has an exposed metal paddle that must also be connected to RF ground.	
2, 11	RFIN, RFOUT	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required.	
4, 5, 6, 7, 8, 9	V1 - V6	See truth table and control voltage table.	
13, 14, 16	NC	This pin should be connected to PCB RF ground to maximize performance.	
15	VDD	Supply Voltage	

Evaluation PCB Schematic



Evaluation PCB Layout



** R1 - R6 = 100 Ohm.*
These resistors are optional and may be used to enhance decoupling of the RF path from the control inputs.

List of Materials for Evaluation PCB EV1HMC425ALP3E [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
TP1-TP8	DC Test Point
C1-C2, C6, C7, C12	100 pF Capacitor, 0402 Pkg.
R1 - R6	100 Ohm Resistor, 0402 Pkg.
U1	HMC425ALP3E Digital Attenuator
PCB [2]	08-044925 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices upon request.