Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.3	7.0	V
Voltages on: ENABLE, V_{SENSE}, V_{S0}-V_{S2}		-0.3	V_{IN} + 0.3	V
Voltage on: V_{FB}		-0.3	2.7	V
Storage Temperature Range	T_{STG}	-65	150	℃
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Output Voltage Range	V_{OUT}	0.6	V_{IN}-0.45	V
Operating Ambient Temperature	T_A	-40	+85	℃
Operating Junction Temperature	T_J	-40	+125	℃

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM)	θ_{JA}	65	℃/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	15	℃/W
Thermal Shutdown	T_{J-TP}	+150	℃
Thermal Shutdown Hysteresis		15	℃

Electrical Characteristics

NOTE: T_A = 25℃ unless otherwise noted. Typical values are at VIN = 3.6V.
EP5352QI, EP5362QI: C_{IN} = 2.2µF, C_{OUT}=10uF.
EP5382QI: C_{IN} = 4.7µF, C_{OUT}=10uF.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Under Voltage Lockout	V_{UVLO}	VIN going low to high		2.2	2.3	V
UVLO Hysteresis				0.145		V
V_{OUT} Initial Accuracy	V_{OUT}	2.4V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 100mA; T_A = 25C	-2.0		+2.0	%
V_{OUT} Variation for all Causes	V_{OUT}	2.4V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 0 – 800mA, T_A = -40℃ to +85℃	-3.0		+3.0	%
Feedback Pin Voltage	V_{FB}	2.4V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 100mA VSO=VS1=VS2=1	0.591	0.603	0.615	V
Feedback Pin Input Current	I_{FB}			1		nA
Feedback Pin Voltage	V_{FB}	2.4V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 0-800mA, T_A = -40℃ to +85℃ VSO=VS1=VS2=1	0.585	0.603	0.621	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Voltage Slew Rate	V_{slew}			3		V/mS
Continuous Output Current EP5352QI	I_{OUT}	EP5352Q	500			mA
Continuous Output Current EP5362QI	I_{OUT}	EP5362Q	600			mA
Continuous Output Current EP5382QI	I_{OUT}	EP5382Q	800			mA
Shut-Down Current	I_{SD}	Enable = Low		0.75		µA
Quiescent Current		No switching		800		µA
PFET OCP Threshold	I_{LIM}	$2.4V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le V_{IN} - 0.6V$	1.4	2		A
VS0-VS1 Voltage Threshold		Pin = Low Pin = High	0.0 1.4		0.4 V_{IN}	V
VS0-VS2 Pin Input Current	I_{VSX}			1		nA
Enable Voltage Threshold		Logic Low Logic High	0.0 1.4		0.2 V_{IN}	V
Enable Pin Input Current	I_{EN}	V_{IN} = 3.6V		2		µA
Operating Frequency	F_{OSC}			4		MHz
PFET On Resistance	$R_{DS(ON)}$			340		mΩ
NFET On Resistance	$R_{DS(ON)}$			270		mΩ
Internal Inductor DCR				.110		Ω
Soft-Start Operation						
Soft-Start Slew Rate	VSS	VID programming mode	1.95	3	4.05	V/mS
VOUT Rise Time	TSS	VFB programming mode	1.56	2.4	3.24	mS

Pin Description

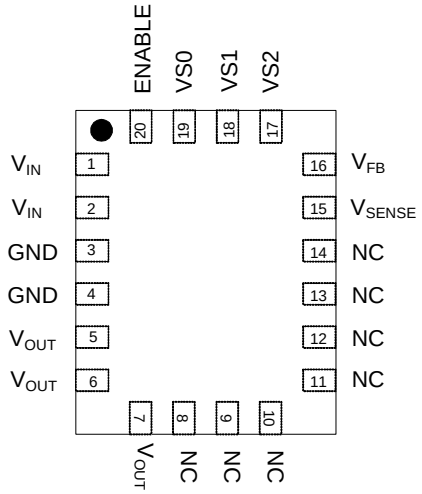


Figure 2. Pin description, top view.

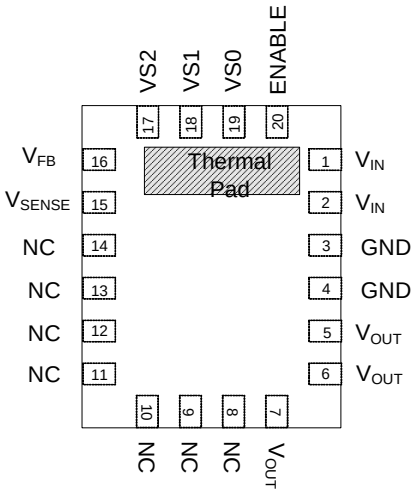


Figure 3. Pin description, bottom view.

V_{IN} (Pin 1,2): Input voltage pin. Supplies power to the IC. V_{IN} can range from 2.4V to 5.5V.

Input GND: (Pin 3): Input power ground. Connect this pin to the ground terminal of the input capacitor. Refer to Layout Recommendations for further details.

Output GND: (Pin 4): Power ground. The output filter capacitor should be connected to this pin. Refer to Layout recommendations for further detail.

V_{OUT} (Pin 5,6,7): Regulated output voltage.

NC (Pin 8,9,10,11,12,13,14): These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.

V_{SENSE} (Pin 15): Sense pin for output voltage regulation. Connect V_{SENSE} to the output voltage rail as close to the terminal of the output filter capacitor as possible.

V_{FB} (Pin 16): Feed back pin for external divider option. When using the external divider option (VS0=VS1=VS2= high) connect this pin to the center of the external divider. Set the divider such that V_{FB} = 0.603V.

VS0,VS1,VS2 (Pin 17,18,19): Output voltage select. VS0=pin19, VS1=pin18, VS2=pin17. Selects one of seven preset output voltages or choose external divider by connecting pins to logic high or low. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate. (refer to section on output voltage select for more detail).

ENABLE (Pin 20): Output enable. Enable = logic high, disable = logic low. Logic low is defined as $V_{LOW} \leq 0.2V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate.

Thermal Pad. Thermal pad to remove heat from package. Connect to surface ground pad and PCB internal ground plane.

Functional Block Diagram

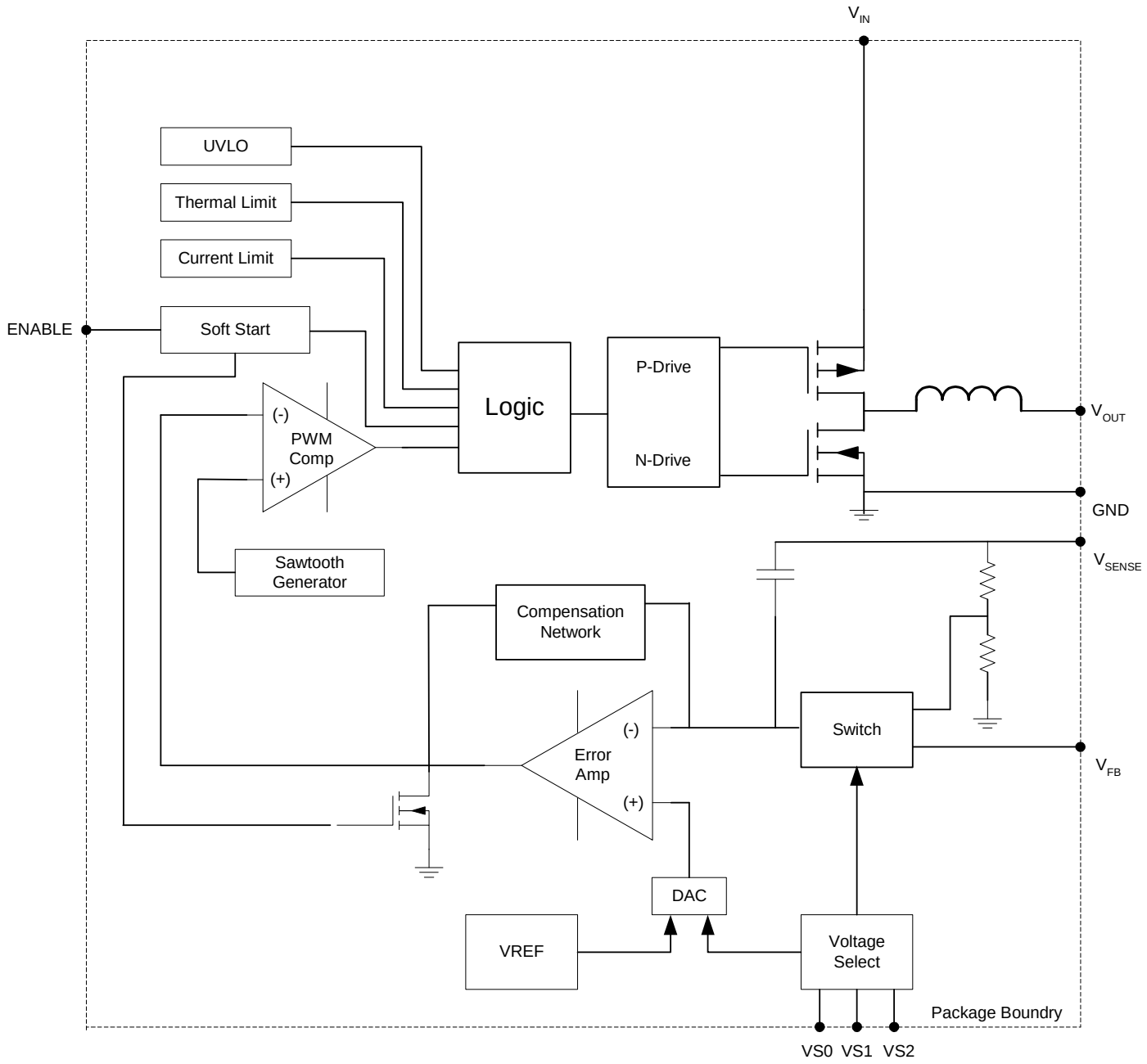
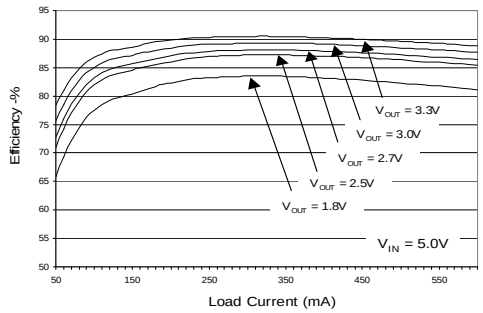


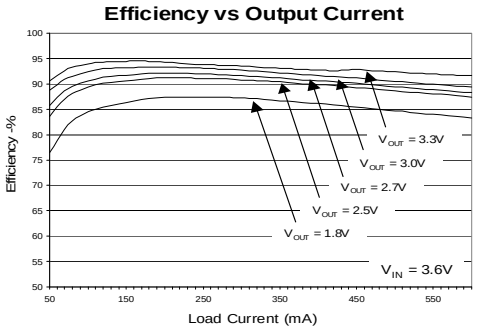
Figure 4. Functional block diagram.

Typical Performance Characteristics

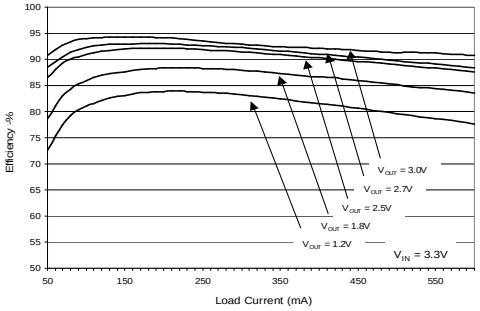
Efficiency vs Output Current



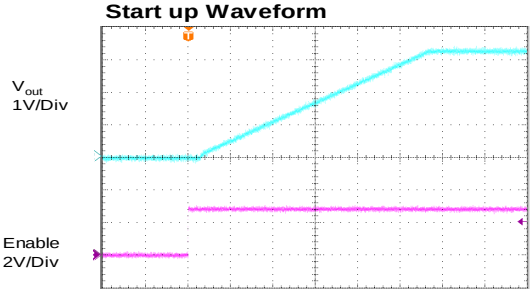
Efficiency vs Output Current



Efficiency vs Output Current

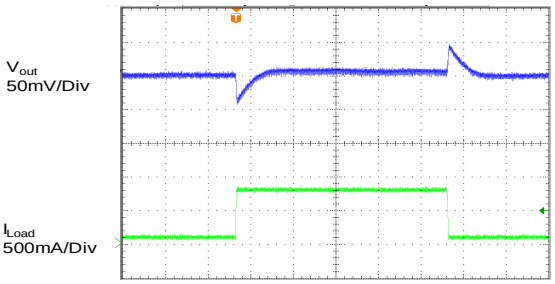


Start up Waveform



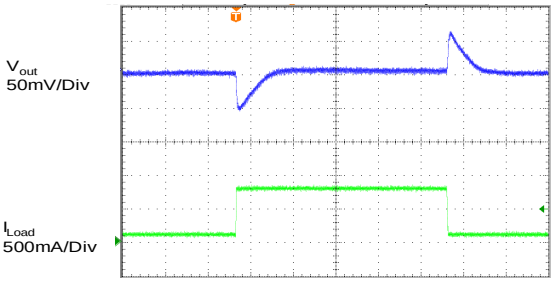
V_{IN} = 5.0V 200µs/Div
V_{OUT} = 3.3V

Transient Response



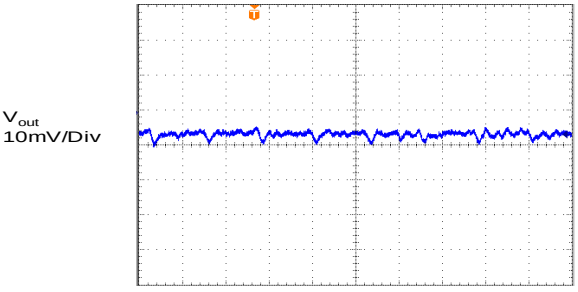
V_{IN} = 5.0V 20µs/Div
V_{OUT} = 3.3V
I_{load} = 100mA to 800mA

Transient Response



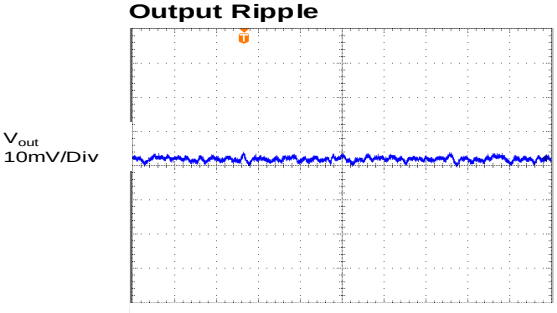
V_{IN} = 3.3V 20µs/Div
V_{OUT} = 1.8V
I_{load} = 100mA to 800mA

Output Ripple



V_{IN} = 3.6V 200ns/Div
V_{OUT} = 3.3V
Output Cap = 10 µF 0805

Output Ripple



V_{IN} = 3.6V 200ns/Div
V_{OUT} = 3.3V
Output Cap = 2 x 10 µF 0805

Detailed Description

Functional Overview

The EP53x2Q family is a complete DCDC converter solution requiring only two low cost MLCC capacitors. MOSFET switches, PWM controller, Gate-drive, compensation, and inductor are integrated into the tiny 5mm x 4mm x 1.1mm package to provide the smallest footprint possible while maintaining high efficiency and high performance. The converter uses voltage mode control to provide the simplest implementation and high noise immunity. The device operates at a 4 MHz switching frequency. The high switching frequency allows for a wide control loop bandwidth providing excellent transient performance. The 4 MHz switching frequency enables the use of very small components making possible this unprecedented level of integration.

Enpirion's proprietary power MOSFET technology provides very low switching loss at frequencies of 4 MHz and higher, allowing for the use of very small internal components, and very wide control loop bandwidth. Unique magnetic design allows for integration of the inductor into the very low profile 1.1mm package. Integration of the inductor virtually eliminates the design/layout issues normally associated with switch-mode DCDC converters. All of this enables much easier and faster integration into various applications to meet demanding EMI requirements.

Output voltage is chosen from seven preset values via a three pin VID voltage select scheme. An external divider option enables the selection of any voltage in the 0.6 to V_{IN} - $V_{dropout}$. This reduces the number of components that must be qualified and reduces inventory problems. The VID pins can be toggled on the fly to implement glitch free dynamic voltage scaling.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor

Enpirion has introduced the world's first product family featuring integrated inductors. The EP53x2Q family utilizes a low loss, planar construction inductor. The use of an internal inductor localizes the noises associated with the output loop currents. The inherent shielding and compact construction of the integrated inductor reduces the radiated noise that couples into the traces of the circuit board. Further, the package layout is optimized to reduce the electrical path length for the AC ripple currents that are a major source of radiated emissions from DCDC converters. The integrated inductor significantly reduces parasitic effects that can harm loop stability, and makes layout very simple.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EP53x2QI have two soft start operating modes. When VOUT is programmed using a preset voltage in VID mode, the device has a constant slew rate. When the EP53x2QI is configured in external resistor divider mode, the device has a constant VOUT ramp time. Output voltage slew rate and ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup.

When operating in VID mode, the maximum total capacitance on the output, including the output filter capacitor and bulk and decoupling capacitance, at the load, is given as:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 350uF$

When the EP53x2QI output voltage is programmed using and external resistor divider the maximum total capacitance on the output is given as:

$C_{OUT\_TOTAL\_MAX} = 6.253x10^{-4}/V_{OUT}$ Farads

The above number and formula assume a no load condition at startup.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for a period of 1mS and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat in a "hiccup" mode.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. In shutdown mode, the device quiescent current will be less than 1 uA. The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 15C°, the device will go through the normal startup process.

Application Information

Output Voltage Select

To provide the highest degree of flexibility in choosing output voltage, the EP53x2Q family uses a 3 pin VID, or Voltage ID, output voltage select arrangement. This allows the designer to choose one of seven preset voltages, or to use an external voltage divider. Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

Table 1 shows the various VS0-VS2 pin logic states and the associated output voltage levels. A logic "1" indicates a connection to V_{IN} or to a "high" logic voltage level. A logic "0" indicates a connection to ground or to a "low" logic voltage level. These pins can be either hardwired to V_{IN} or GND or alternatively can be driven by standard logic levels. These pins must not be left floating.

Table 1. Voltage select settings.

VS2	VS1	VS0	V_{OUT}
0	0	0	3.3
0	0	1	2.5
0	1	0	2.8
0	1	1	1.2
1	0	0	3.0
1	0	1	1.8
1	1	0	2.7
1	1	1	External

External Voltage Divider

As described above, the external voltage divider option is chosen by connecting the VS0, VS1, and VS2 pins to V_{IN} or logic "high". The EP53x2Q uses a separate feedback pin, V_{FB}, when using the external divider. VSENSE must be connected to V_{OUT} as indicated in Figure 5.

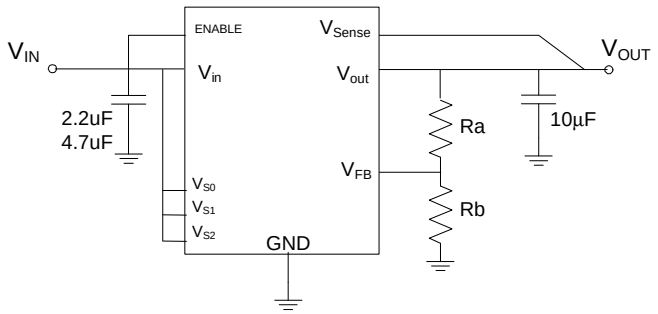


Figure 5. External Divider.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.603V\left(1+\frac{Ra}{Rb}\right)$$

R_a must be chosen as 200KΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{1.2x10^5}{V_{OUT} - 0.603}\Omega$$

Dynamically Adjustable Output

The EP53x2Q are designed to allow for dynamic switching between the predefined VID voltage levels The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is identical to the soft-start slew rate of 3V/mS.

Dynamic transitioning between internal VID settings and the external divider is not allowed.

Input and Output Capacitors

The **input** capacitance requirement is as follows:

EP5352Q, EP5362Q = 2.2uF

EP5382Q = 4.7uF

Enpirion recommends that a low ESR MLCC capacitor be used. The input capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input and output filter applications.

The **output** capacitance requirement is a minimum of 10uF. The control loop is designed to be stable with up to 60uF of total output capacitance without requiring modification of the control loop. Capacitance above the 10uF minimum should be added if the transient performance is not sufficient using the 10uF. Enpirion recommends a low ESR MLCC type capacitor be used. The output capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter input and output filter applications.

Cin

Manufacturer	Part #	Value	WVDC	Case Size
Murata	GRM219R61A475KE19D	4.7uF	10V	0805
	GRM319R61A475KA01D			1206
	GRM219R60J475KE01D		6.3V	0805
	GRM31MR60J475KA01L			1206
Panasonic	ECJ-2FB1A475K		10V	0805
	ECJ-3YB1A475K			1206
	ECJ-2FB0J475K		6.3V	0805
	ECJ-3YB0J475K			1206
Taiyo Yuden	LMK212BJ475KG-T		10V	0805
	LMK316BJ475KD-T			1206
	JMK212BJ475KD-T		6.3V	0805

Cin

Manufacturer	Part #	Value	WVDC	Case Size
Murata	GRM21BR71A225KA01L	2.2uF	10V	0805
	GRM31MR71A225KA01L			1206
	GRM21BR70J225KA01L		6.3V	0805
Panasonic	ECJ-2FB1A225K		10V	0805
	ECJ-3YB1A225K			1206
	ECJ-2YB0J225K		6.3V	0805
Taiyo Yuden	LMK107BJ225KA-T		10V	0603
	LMK212BJ225KG-T			0805

Cout

Manufacturer	Part #	Value	WVDC	Case Size
Murata	GRM219R60J106KE19D	10uF	6.3V	0805
	GRM319R60J106KE01D			1206
Panasonic	ECJ-2FB0J106K		6.3V	0805
	ECJ-3YB0J106K			1206
Taiyo Yuden	JMK212BJ106KD-T		6.3V	0805
	JMK316BJ106KF-T			1206

LAYOUT CONSIDERATIONS*

*Optimized PCB Layout file downloadable from the Enpirion Website to assure first pass design success

Recommendation 1: Input and output filter capacitors should be placed as close to the EP53x2QI package as possible to reduce EMI from input and output loop AC currents. This reduces the physical area of the Input and Output AC current loops.

Recommendation 2: DO NOT connect GND pins 3 and 4 together. Pin 3 should be used for the Input capacitor local ground and pin 4 should be used for the output capacitor ground. The ground pad for the input and output filter capacitors should be isolated ground islands and should be connected to system ground as indicated in recommendation 3 and recommendation 5.

Recommendation 3: Multiple small vias (0.25mm after copper plating) should be used to connect ground terminals of the Input capacitor and the output capacitor to the system ground plane. This provides a low inductance path for the high-frequency AC currents, thereby reducing ripple and suppressing EMI (see Fig. 5, Fig. 6, and Fig. 7).

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many thermal vias as possible. The vias should use 0.33mm drill size with minimum one ounce copper plating (0.035mm plating thickness). This provides the path for heat dissipation from the converter.

Recommendation 5: The system ground plane referred to in recommendations 3 and 4 should be the first layer immediately below the surface layer (PCB layer 2). This ground plane should be continuous and un-interrupted below the converter and the input and output capacitors that carry large AC currents. If it is not possible to make PCB layer 2 a continuous ground plane, an uninterrupted ground “island” should be created on PCB layer 2 immediately underneath the EP53x2QI and its input and output capacitors. The vias that connect the input and output capacitor

grounds, and the thermal pad to the ground island, should continue through to the PCB GND layer as well.

Recommendation 6: As with any switch-mode DC/DC converter, do not run sensitive signal or control lines underneath the converter package.

Figure 6 shows an example schematic for the EP53x2Q using the internal voltage select. In this example, the device is set to a V_{OUT} of 1.2V (VS2=0, VS1=1, VS0=1).

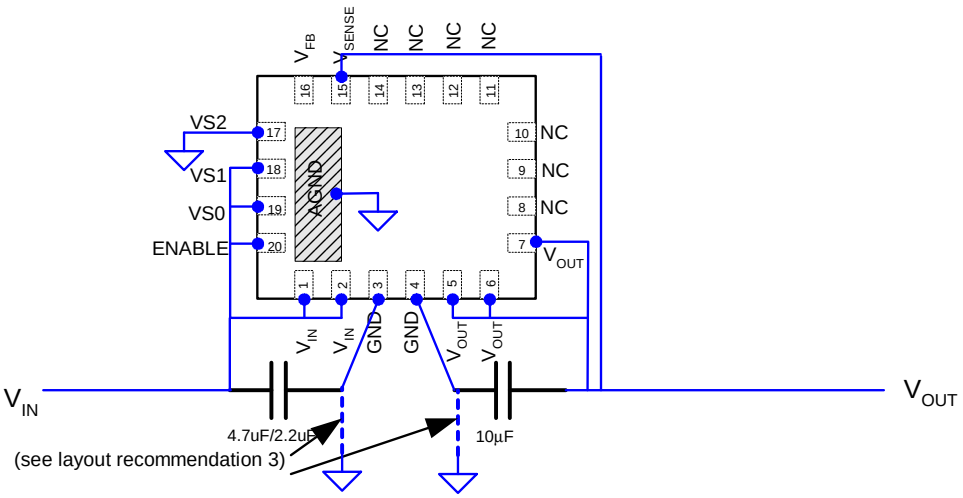


Figure 6. Example application, Vout=1.2V.

Figure 7 shows an example schematic using an external voltage divider. VS0=VS1=VS2= “1”. The resistor values are chosen to give an output voltage of 2.6V.

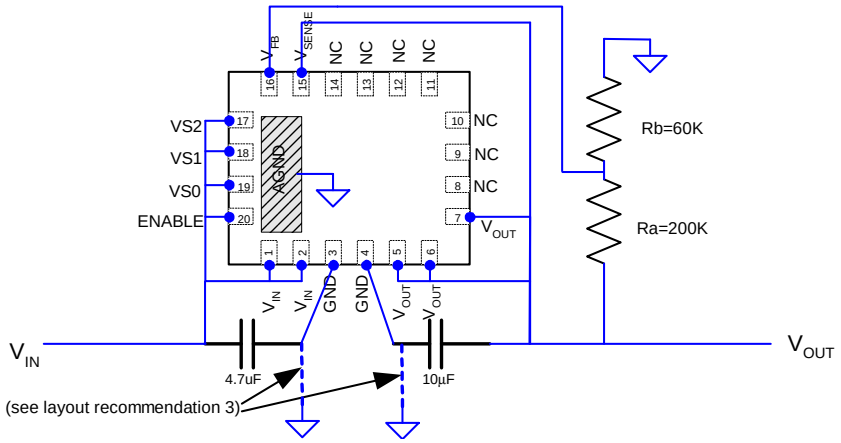


Figure 7. Schematic showing the use of external divider option, Vout = 2.6V.

Figure 8 shows two example board layouts. Note the placement of the input and output capacitors. They are placed close to the device to minimize the physical area of the AC current loops. Note the placement of the vias per recommendation 3.

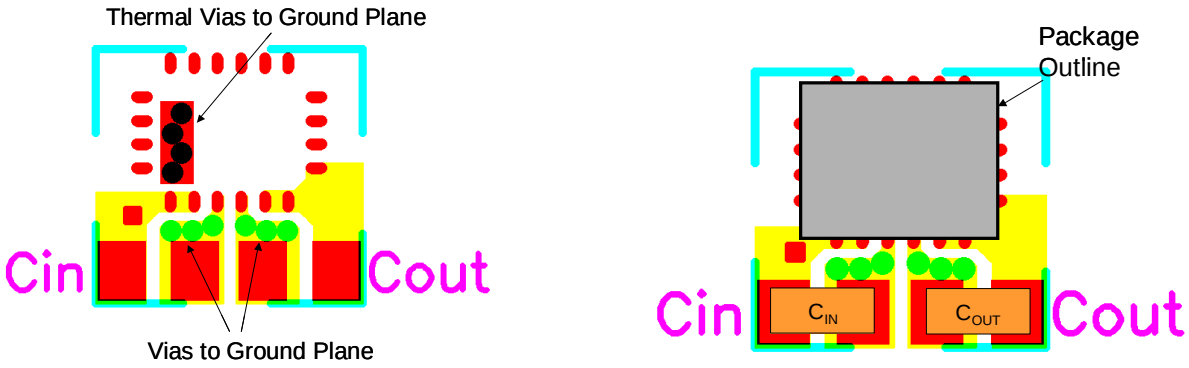


Figure 8. Example layout showing PCB top layer, as well as demonstrating use of vias from input, output filter capacitor local grounds, and thermal pad, to PCB system ground.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom Of Package

Enpirion has developed a break-through in package technology that utilizes the lead frame as part of the electrical circuit. The lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, it does require some special considerations.

As part of the package assembly process, lead frame construction requires that for mechanical support, some of the lead-frame metal be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EP53x2QI should be clear of any metal except for the large thermal pad. The “grayed-out” area in Figure 9 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.

NOTE: Clearance between the various exposed metal pads, the thermal ground pad, and the perimeter pins, meets or exceeds JEDEC requirements for lead frame package construction (JEDEC MO-220, Issue J, Date May 2005). The separation between the large thermal pad and the nearest adjacent metal pad or pin is a minimum of 0.20mm, including tolerances. This is shown in Figure 10.

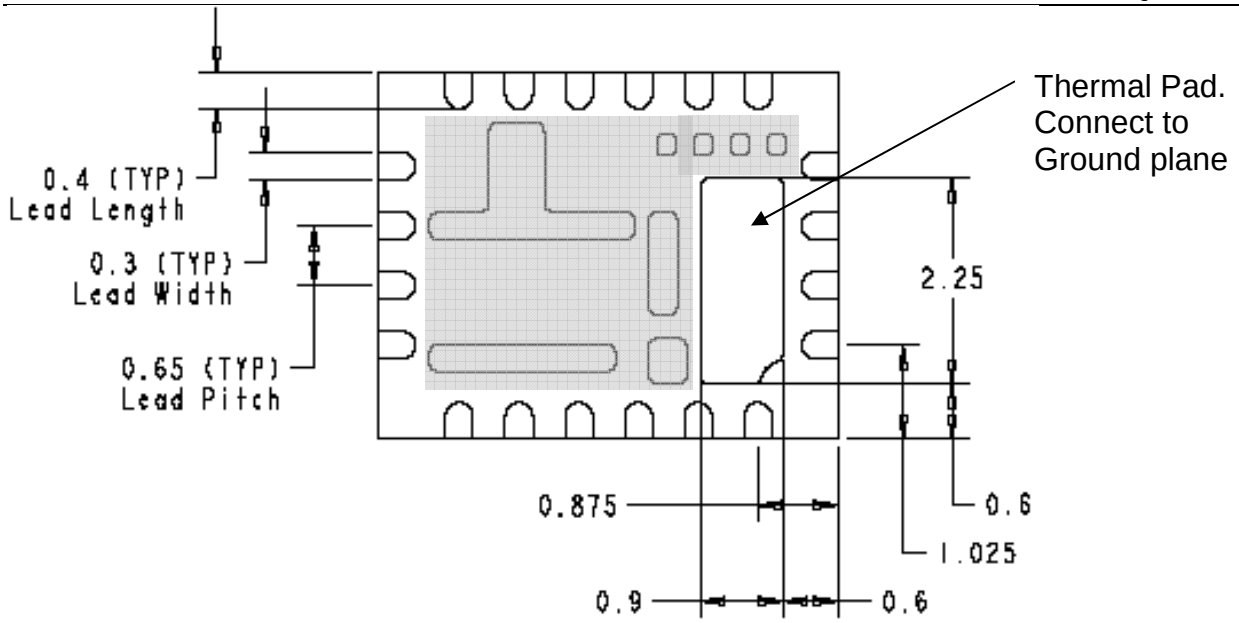


Figure 9. Exposed metal and mechanical dimensions of the package . The gray area represents the bottom metal no-connect area. This area should be clear of any traces, planes, or vias, on the top layer of the PCB.

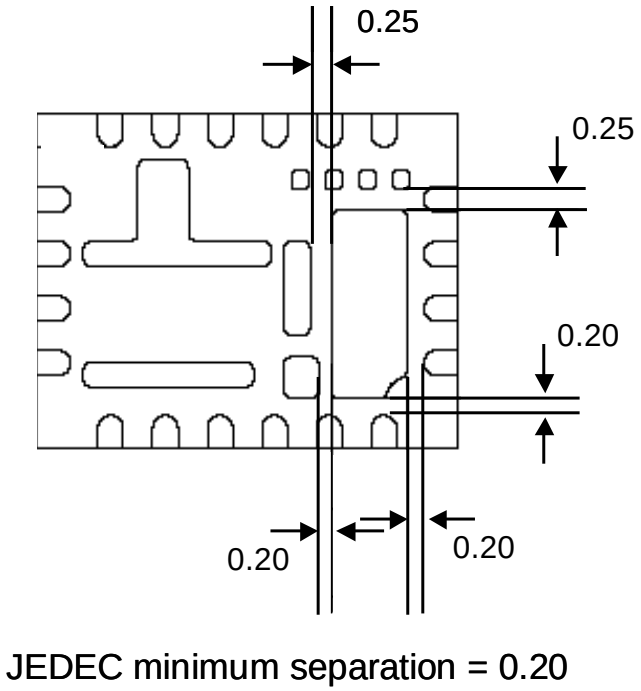


Figure 10. Exposed pad clearances; the Enpirion lead frame package complies with JEDEC requirements.

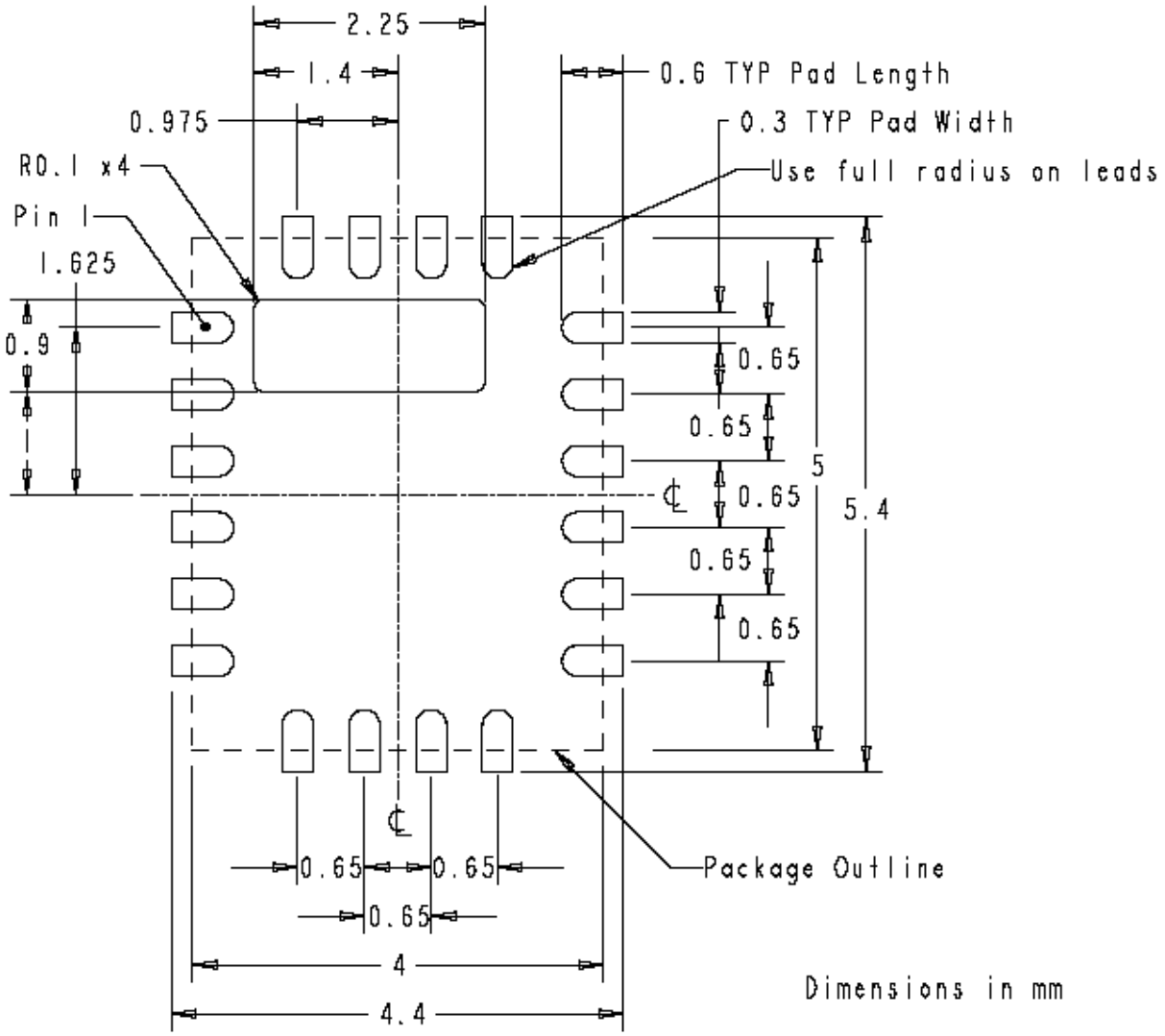


Figure 11. Recommended PCB Solder Mask Openings.

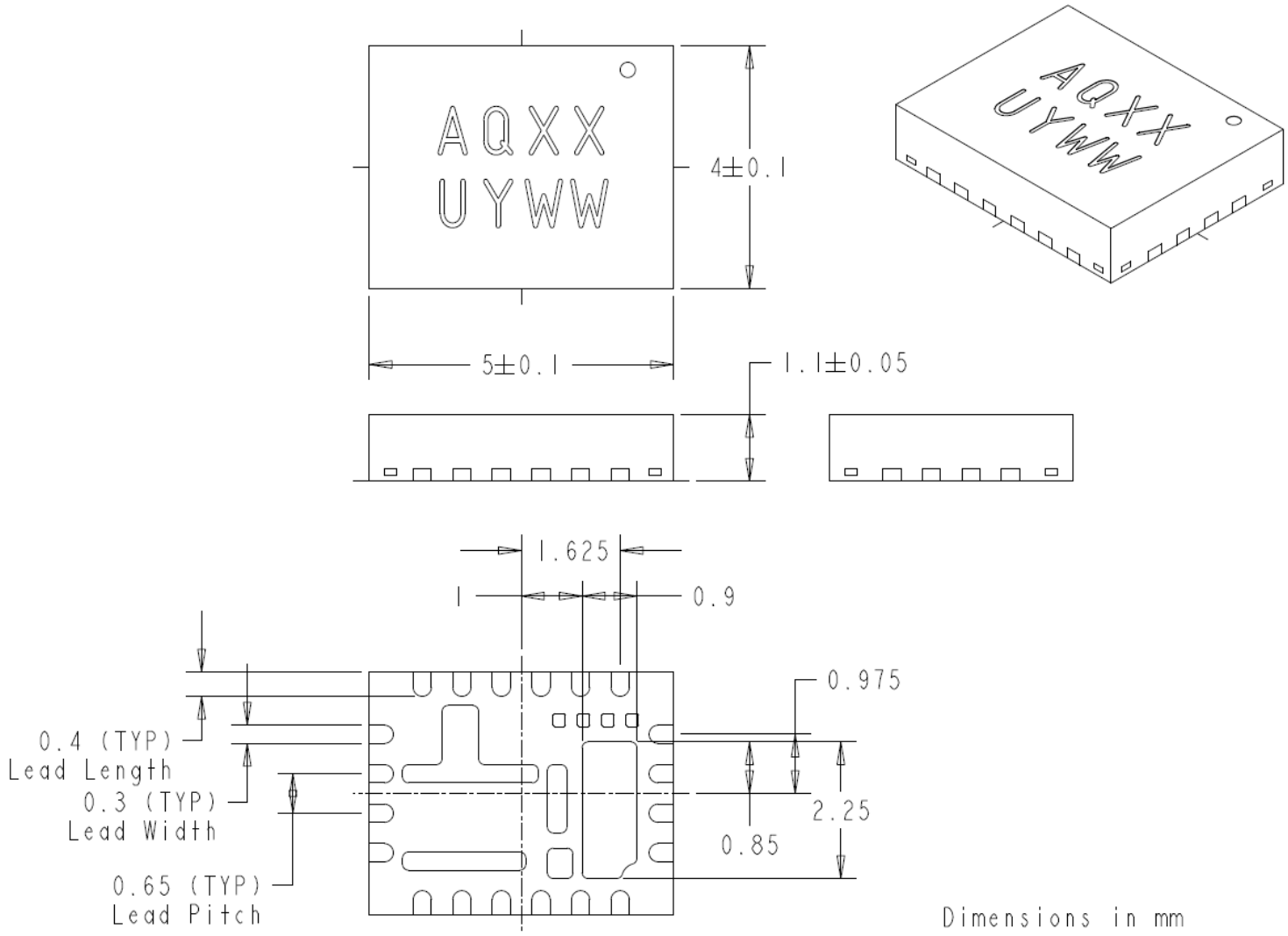


Figure 12. Package mechanical dimensions.

Contact Information

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