- Blocking (BWIF = 165kHz): 64dBc at frequency offset = 1MHz and 48dBc at 225kHz
- High image rejection: 55dB at 315MHz/433.92MHz and 47dB at 868.3MHz/915MHz without calibration
- Supported data rate in buffered mode 0.5Kbit/s to 80Kbit/s (120Kbit/s NRZ)
- Supports pattern-based wake-up and start of frame identification
- Flexible service configuration concept with on-the-fly (OTF) modification (in IDLEMode) of SRAM service parameters (data rate, …)
    - Each service consists of
        - One service-specific configuration part
        - Three channel-specific configuration parts
    - Three service configurations are located in EEPROM
    - Two service configurations are located in SRAM and can be modified via SPI or embedded application software
- Digital RSSI with very high relative accuracy of ±1dB thanks to digitized IF processing
- Programmable clock output derived from crystal frequency
- 1024byte EEPROM data memory for transceiver configuration
- SPI interface for Rx/Tx data access and transceiver configuration
- 500Kbit SPI data rate for short periods on SPI bus and host controller
- On demand services (SPI or API) without polling or telegram reception
- Integrated temperature sensor
- Self check and calibration with temperature measurement
- Configurable EVENT signal indicates the status of the IC to an external microcontroller
- Automatic antenna tuning at Tx center frequency for loop antenna
- Automatic low-power channel polling
- Flexible polling configuration concerning timing, order and participating channels
- Fast Rx/Tx reaction time
- Power-up (typical 1.5ms OFFMode -> TXMode, OFFMode -> RXMode)
- RXMode <-> TXMode switching (typical 500µs)
- Supports mixed ASK/FSK telegrams
- Non-byte aligned data reception and transmission
- Software customization
- Antenna diversity with external switch via GPIO control
- Antenna diversity with internal SPDT switch
- Supply voltage range 1.9V to 3.6V
- Temperature range –40°C to +85C
- ESD protection at all pins (±4kV HBM, ±200V MM, ±750V FCDM)
- Small 5×5mm QFN32 package/pitch 0.5mm
- Suitable for applications governed by EN 300 220 and FCC part 15, title 47

Applications

- Remote Control System
- Home and Building Automation
- Wireless Sensor Networks
- Weather stations
- Battery operated remote controls
- Smoke detectors
- Wireless alarm and security systems

1. General Description

1.1 Introduction

The Atmel® ATA8510/15 is a highly integrated, low-power UHF ASK/FSK RF transceiver with an integrated AVR® microcontroller.

The Atmel ATA8510/15 is partitioned into three sections; an RF front end, a digital baseband and the low-power 8-bit AVR microcontroller. The product is designed for the ISM frequency bands in the ranges of 310MHz to 318MHz, 418MHz to 477MHz and 836MHz to 956MHz. The external part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. The receive path uses a low-IF architecture with an integrated double quadrature receiver and digitized IF processing. This results in high image rejection and excellent blocking performance. The transmit path uses a closed loop fractional-N modulator with Gauss shaping and pre-emphasis functionality for high data rates. In addition, highly flexible and configurable baseband signal processing allows the transceiver to operate in several scanning, wake-up and automatic self-polling scenarios. For example, during polling the IC can scan for specific message content (IDs) and save valid telegram data in the FIFO buffer for later retrieval. The device integrates two receive paths that enable a parallel search for two telegrams with different modulations, data rates, wake-up conditions, etc.

The Atmel ATA8510/15 implements a flexible service configuration concept and supports up to 15 channels. The channels are grouped into five service configurations with three channels each. Three service configurations are located in the EEPROM. Two service configurations are located in the SRAM to allow on-the-fly modifications during IDLEMode via SPI commands or application software. The application software is located in the Flash for Atmel ATA8510. Highly configurable and autonomous scanning capability enables flexible polling scenarios with up to 15 channels. The configuration of the transceiver is stored in a 1024byte EEPROM. The SPI interface enables external control and device reconfiguration.

Table 1-1. Program Memory Comparison of Atmel ATA8510/15 Devices

Device	Atmel Firmware ROM	User Flash	User ROM
Atmel ATA8515	24Kbyte	-	-
Atmel ATA8510	24Kbyte	20Kbyte	-

In the Atmel ATA8510 the internal microcontroller with 20Kbyte user flash can be used to add custom extensions to the Atmel firmware. The Atmel ATA8515 embeds only the firmware ROM without user memory.

The debugWIRE and ISP interface are available for programming purposes.

1.2 System Overview

Figure 1-1. Circuit Overview

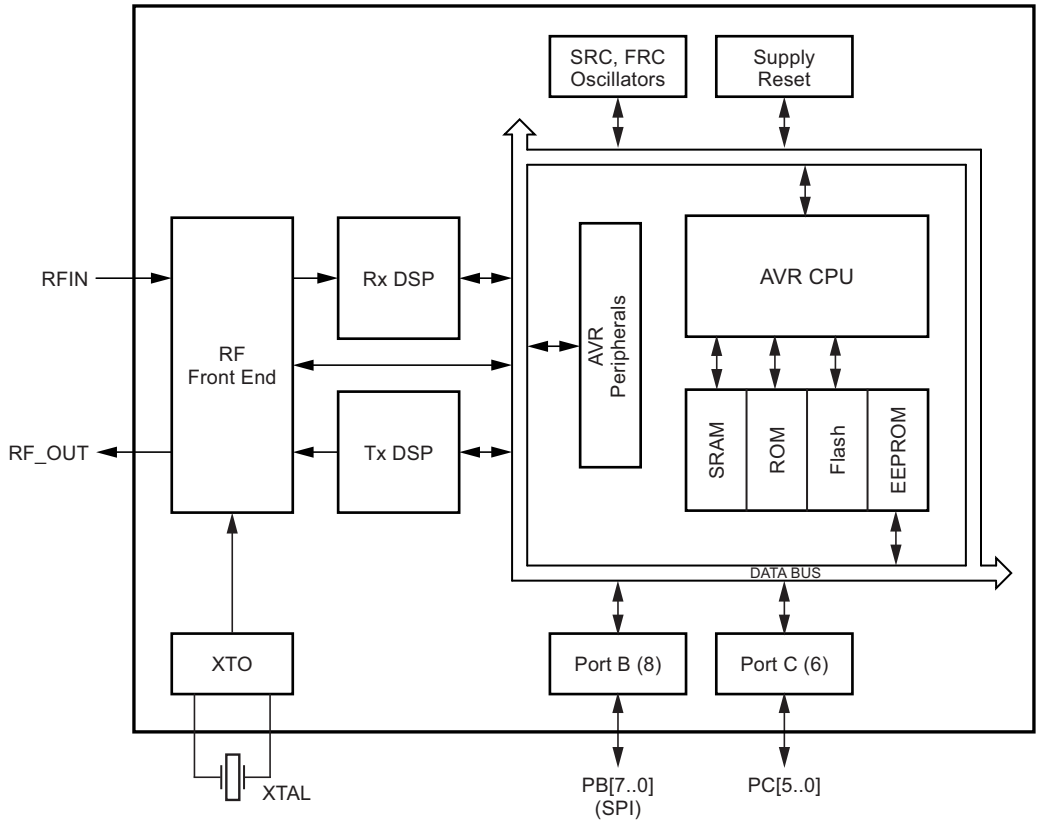


Figure 1-1 shows an overview of the main functional blocks of the Atmel® ATA8510/15. External control of the Atmel ATA8510/15 is performed through the SPI pins SCK, MOSI, MISO, and NSS on port B. The configuration of the Atmel ATA8510/15 is stored in the EEPROM and a large portion of the functionality is defined by the firmware located in the ROM and processed by the AVR®. An SPI command can trigger the AVR to configure the hardware according to settings that are stored in the EEPROM and start up a given system mode (e.g., RXMode, TXMode or PollingMode). Internal events such as “Start of Telegram” or “FIFO empty” are signaled to an external microcontroller on pin 28 (PB6/EVENT).

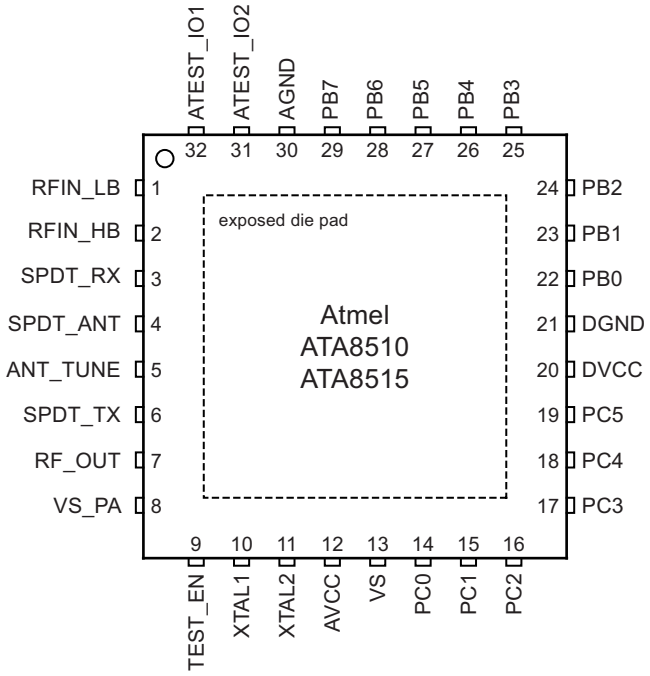
During the start-up of a service, the relevant part of the EEPROM content is copied to the SRAM. This allows faster access by the AVR during the subsequent processing steps and eliminates the need to write to the EEPROM during runtime because parameters can be modified directly in the SRAM. As a consequence the user does not need to observe the EEPROM read/write cycle limitations.

It is important to note that all PWRON and NPWRON pins (PC1..5, PB4, PB7) are active in OFFMode. This means that even if the Atmel ATA8510/15 is in OFFMode and the DVCC voltage is switched off, the power management circuitry within the Atmel ATA8510/15 biases these pins with VS.

AVR ports can be used as button inputs, external LNA supply voltage (RX_ACTIVE), LED drivers, EVENT pin, switching control for additional SPDT switches, general purpose digital inputs, or wake-up inputs, etc. Some functionality of these ports is already implemented in the firmware and can be activated by adequate EEPROM configurations. Other functionality is available only through custom software residing in the 20Kbyte flash program memory (Atmel ATA8510).

1.3 Pinning

Figure 1-2. Pin Diagram



Note: The exposed die pad is connected to the internal die.

Table 1-2. Pin Description

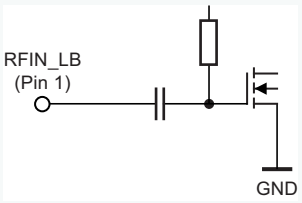
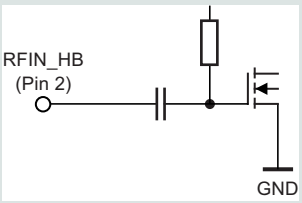
Pin No.	Pin Name	Type	Equivalent Circuit	Description
1	RFIN_LB	Analog		LNA input for low-band frequency range (< 500MHz)
2	RFIN_HB	Analog		LNA input for high-band frequency range (> 500MHz)

Table 1-2. Pin Description (Continued)

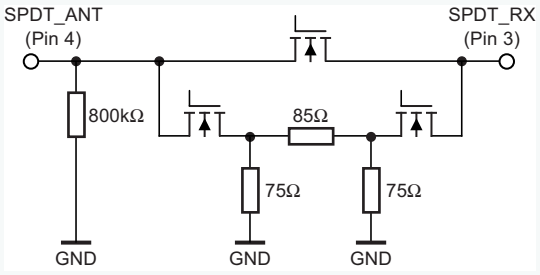
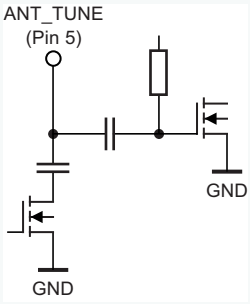
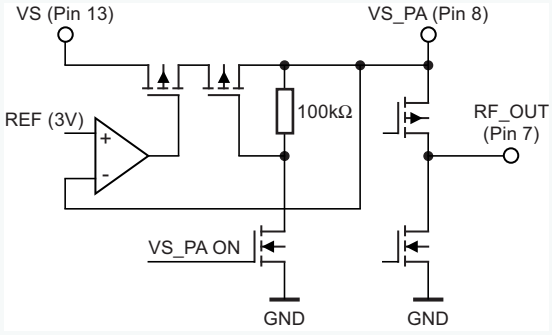
Pin No.	Pin Name	Type	Equivalent Circuit	Description
3	SPDT_RX	Analog		Rx switch output (damped signal output)
4	SPDT_ANT	Analog		Antenna input (RXMode) and output (TXMode) of the SPDT switch
5	ANT_TUNE	Analog		Antenna tuning input
6	SPDT_TX	Analog	See also circuit pin 3 and pin 4 	TXMode input of the SPDT switch
7	RF_OUT	Analog		Power amplifier output
8	VS_PA	Analog		Power amplifier supply, connect to VS

Table 1-2. Pin Description (Continued)

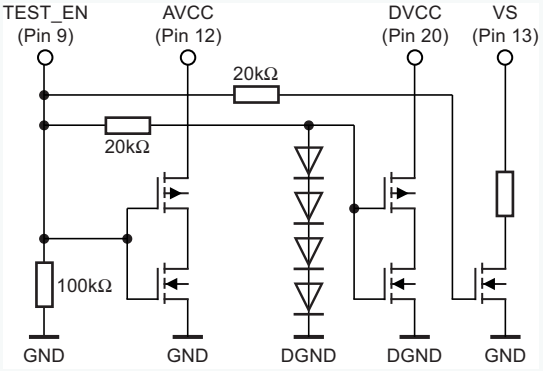
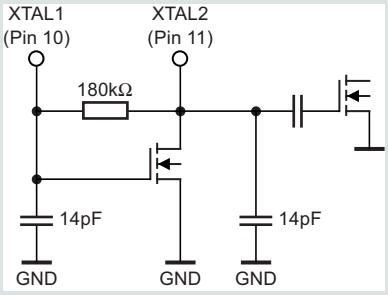
Pin No.	Pin Name	Type	Equivalent Circuit	Description	
9	TEST_EN	–		Test enable, connected to GND in application	
10	XTAL1	Analog		Crystal oscillator pin 1 (input)	
11	XTAL2	Analog		Crystal oscillator pin 2 (output)	
12	AVCC	Analog	See Section 4.1 on page 22	RF front end supply regulator output	
13	VS	Analog	See Section 4.1 on page 22 and pins 7, 8, and 9	Main supply voltage input	
14	PC0	Digital		Main Alternate	: AVR Port C0 : PCINT8 / NRESET / DebugWIRE
15	PC1	Digital		Main Alternate	: AVR Port C1 : NPWRON1 / PCINT9 / EXT_CLK
16	PC2	Digital		Main Alternate	: AVR Port C2 : NPWRON2 / PCINT10 / TRPA
17	PC3	Digital		Main Alternate	: AVR Port C3 : NPWRON3 / PCINT11 / TMDO / TxD
18	PC4	Digital		Main Alternate	: AVR Port C4 : NPWRON4 / PCINT12 / INT0 / TMDI / RxD
19	PC5	Digital		Main Alternate	: AVR Port C5 : NPWRON5 / PCINT13 / TRPB / TMDO_CLK

Table 1-2. Pin Description (Continued)

Pin No.	Pin Name	Type	Equivalent Circuit	Description	
20	DVCC	–	See Section 4.1 on page 22	Digital supply voltage regulator output	
21	DGND	–	See Section 4.1 on page 22	Digital ground	
22	PB0	Digital		Main Alternate	: AVR Port B0 : PCINT0 / CLK_OUT
23	PB1	Digital		Main Alternate	: AVR Port B1 : PCINT1 / SCK
24	PB2	Digital		Main Alternate	: AVR Port B2 : PCINT2 / MOSI (SPI Master Out Slave In)
25	PB3	Digital		Main Alternate	: AVR Port B3 : PCINT3 / MISO (SPI Master In Slave Out)
26	PB4	Digital		Main Alternate	: AVR Port B4 : PWRON / PCINT4 / LED1 (strong high side driver)
27	PB5	Digital		Main Alternate	: AVR Port B5 : PCINT5 / INT1 / NSS
28	PB6	Digital		Main Alternate	: AVR Port B6 : PCINT6 / EVENT (firmware controlled external micro-controller event flag)
29	PB7	Digital		Main Alternate	: AVR Port B7 : NPWRON6/ PCINT7/ RX_ACTIVE (strong high side driver) / LED0 (strong low side driver)
30	AGND	–	See Section 4.1 on page 22	Analog ground	
31	ATEST_IO2	–		RF front end test I/O 2 connected to GND in application	
32	ATEST_IO1	–		RF front end test I/O 1 connected to GND in application	
	GND	–	See Section 4.1 on page 22	Ground/backplane on exposed die pad	

1.4 Typical Applications

1.4.1 Typical 3V Application with External Microcontroller

Figure 1-3. Typical 3V Application with External Microcontroller

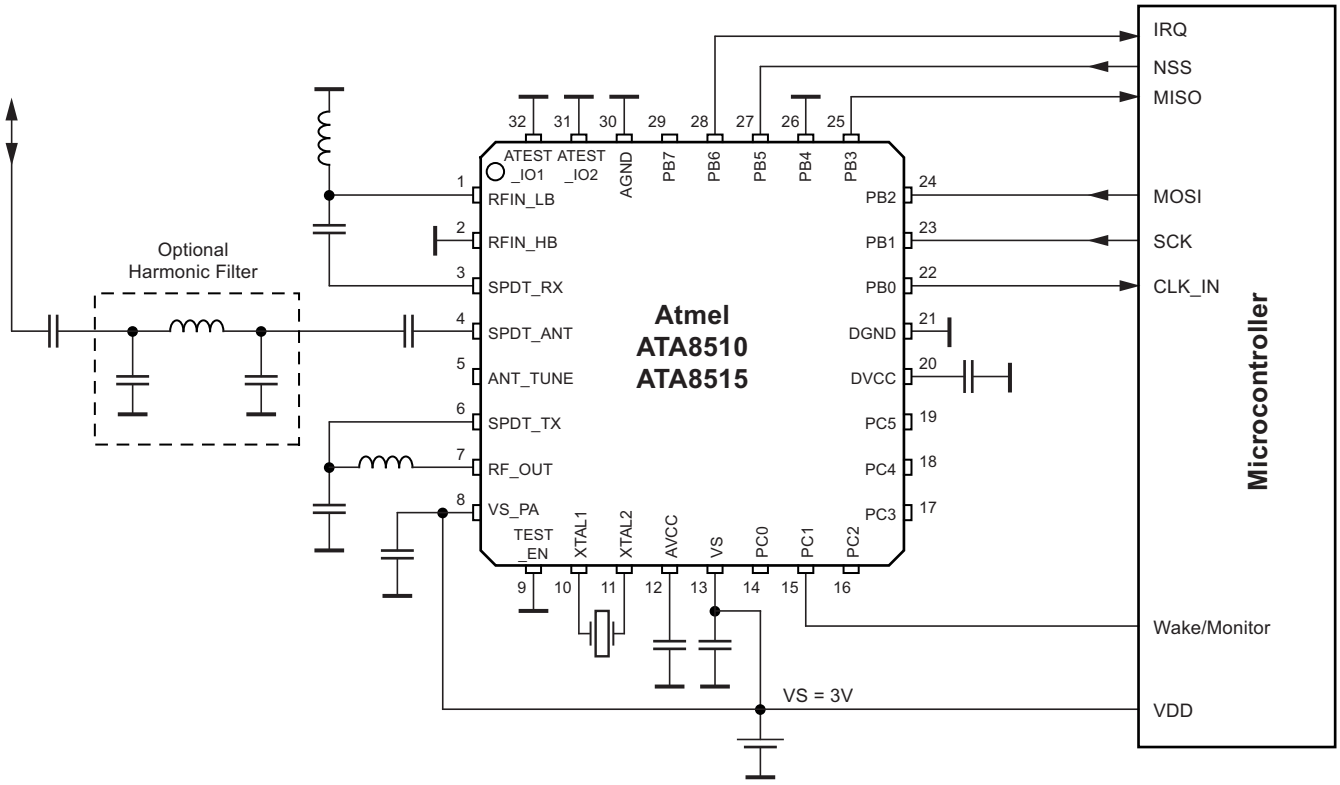


Figure 1-3 shows a typical application circuit with an external host microcontroller for the 315MHz or 433.92MHz band running from a 3V lithium cell. The Atmel® ATA8510/15 stays in OFFMode until NPWRON1 (PC1) is used to wake it up. In OFFMode the Atmel ATA8510/15 draws typically less than 5nA (600nA maximum at 3.6V/85°C).

In OFFMode all Atmel ATA8510/15 AVR® ports PB0..PB7 and PC0..PC5 are switched to input. PC0..PC5 and PB7 have internal pull-up resistors ensuring that the voltage at these ports is VS. PB0..PB6 are tri-state inputs and require additional consideration. PB1, PB2, and PB5 have defined voltages since they are connected to the output of the external microcontroller. PB4 is connected to ground to avoid unwanted power-ups. PB0, PB3 and PB6 do not require external circuitry since the internal circuit avoids transverse currents in OFFMode. The external microcontroller has to tolerate the floating inputs. Otherwise additional pull-down resistors are required on these floating lines.

Typically, the key fob buttons are connected to the external microcontroller and the Atmel ATA8510/15 wake-up is done by pulling NPWRON1 (pin 15) to ground. If there are not enough ports for button inputs on the microcontroller, it is possible to connect up to four additional buttons to the ports PC2..PC5. In this case, the occurrence of a port event (button pressed) generates an event on pin 28. The corresponding port event is available in the event registers.

A PCB trace loop antenna is typically used in this type of application. An internal antenna tuning procedure tunes the resonant frequency of this loop antenna to the Tx frequency. This is accomplished with an integrated variable capacitor on the ANT_TUNE pin. RF_OUT and RF_IN are optimally matched to the SPDT_TX and SPDT_RX pins of the integrated Rx/Tx switch. The SPDT_ANT pin has an impedance of 50Ω for both the Rx and Tx functions. The DC output voltage of the power amplifier is required at the SPDT_TX pin for proper operation. Also, the RFIN pin needs a DC path to ground, which is easily achieved with the matching shunt inductor. The impedance of the loop antenna is transformed to 50Ω with three capacitors, two of them external and one built-in at the ANT_TUNE pin.

Together with the fractional-N PLL within the Atmel® ATA8510/15, an external crystal is used to fix the Rx and Tx frequency. Accurate load capacitors for this crystal are integrated to reduce the system part count and cost. Only four supply blocking capacitors are needed to decouple the different supply voltages AVCC, DVCC, VS, and VS_PA of the Atmel ATA8510/15. The exposed die pad is the RF and analog ground of the Atmel ATA8510/15. It is connected directly to AGND via a fused lead. For applications operating in the 868.3MHz or 915MHz frequency bands a high-band RF input, RFIN_HB, is supplied and must be used instead of RFIN_LB. The Atmel ATA8510/15 is controlled using specific SPI commands via the SPI interface, and an internal EEPROM for application specific configurations.

1.4.2 Typical 3V Stand-Alone Application

Figure 1-4. Typical 3V Stand-alone Application

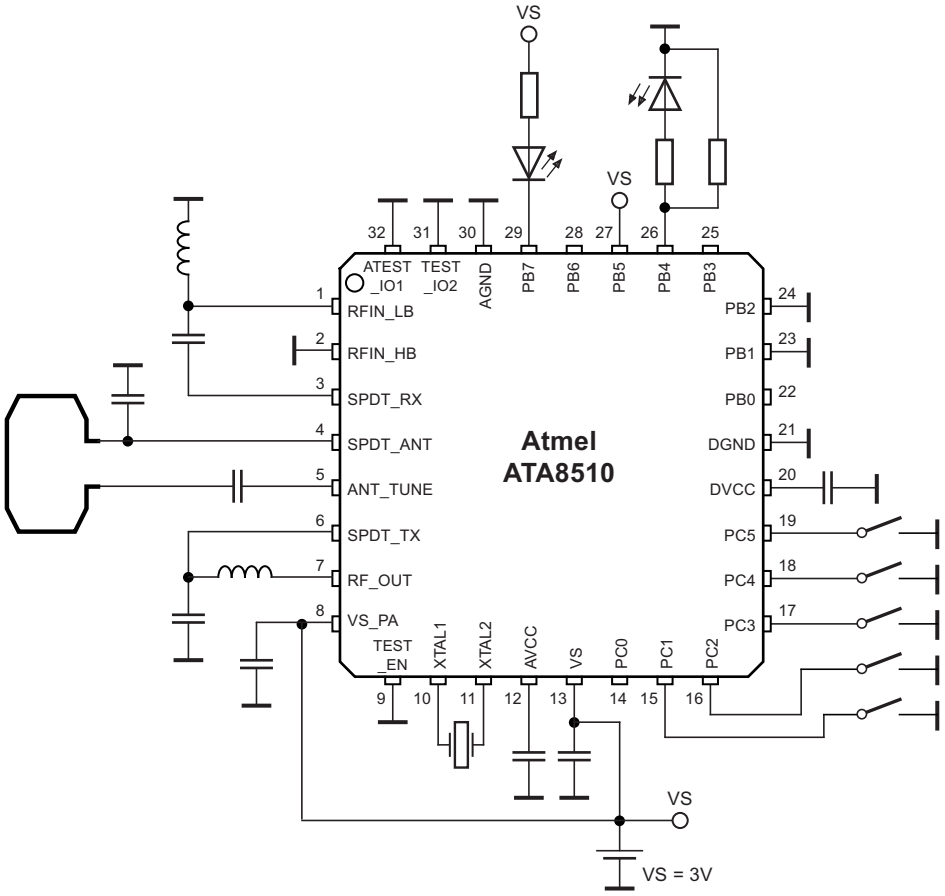


Figure 1-4 shows a stand-alone key fob application circuit for 315MHz or 433.92MHz running from a 3V lithium cell. The Atmel ATA8510/15 stays in OFFMode until one of the NPWRON ports PC1..PC5 is pulled to ground level, waking up the circuit. The NPWRON ports PC1..PC5 have internal 50kΩ pull-up resistors and can be left open if not used.

The user application software within the 20Kbyte Flash (Atmel ATA8510) is used to control the Atmel ATA8510/15 transceiver together with the firmware in the 24Kbyte ROM. The Atmel ATA8515 is not suitable for this application. The RF and decoupling circuitry is similar to Figure 1-3 on page 9.

In this application, an LED is connected to PB7. Alternatively, an additional wake-up button can be used on PB7 instead of an LED. An LED can also be connected to PB4. However, note the additional pull-down resistor connected in parallel that is needed to prevent transverse currents in OFFMode. This special case only applies to PB4 because of its active input characteristics (PWRON).

2. System Functional Description

2.1 Overview

2.1.1 Service-based Concept

The Atmel® ATA8510/15 is a highly configurable UHF transceiver. The configuration is stored in an internal 1024-byte EEPROM. The master system control is performed by firmware. General chip-wide settings are loaded from the EEPROM to hardware registers during system initialization. During start-up of a transmit or receive mode the specific settings are loaded from the EEPROM or SRAM to the current service in the SRAM and from there to the corresponding hardware registers.

A complete configuration set of the transceiver is called “service” and includes RF settings, demodulation settings, and telegram handling information. Each service contains three channels which differ in the RF receive or transmit frequencies.

The Atmel ATA8510/15 supports five services which can be configured in various ways to meet customer requirements. Three service configurations are located in the EEPROM space. They are fixed configurations which should not be changed during runtime.

Two service configurations are located in the SRAM space and can be modified by USER SW in a Flash application or by an SPI command during IDLEMode.

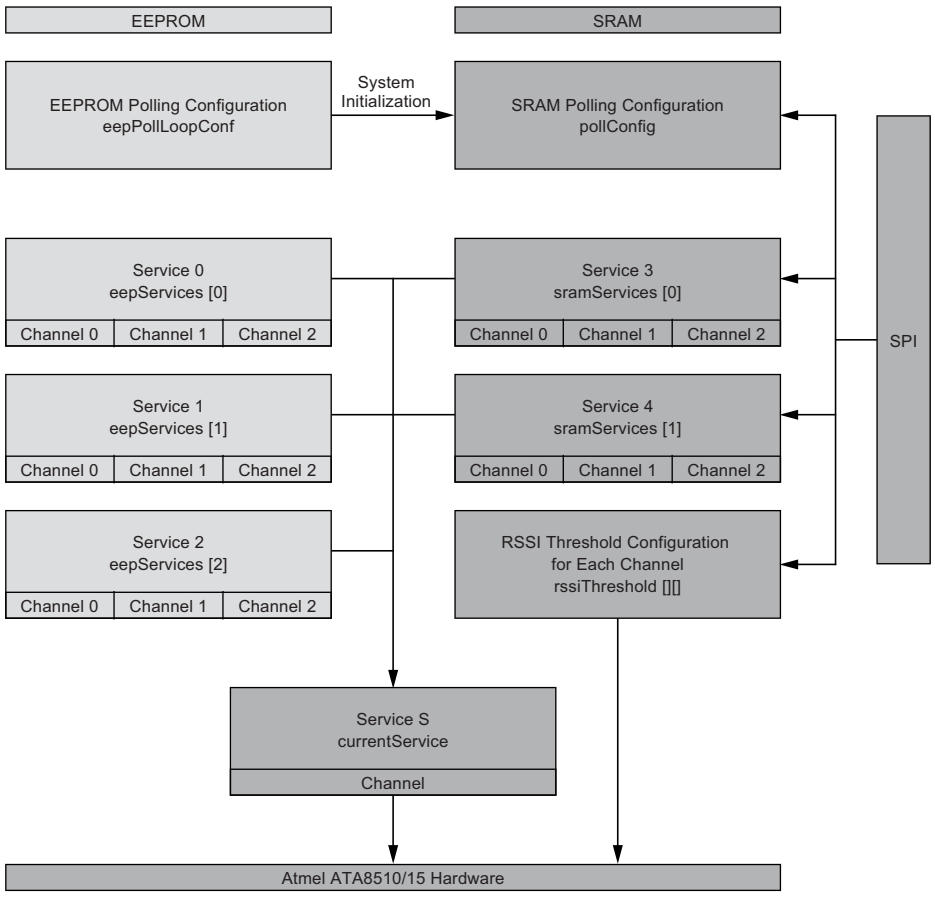
A service consists of

- One service-specific configuration part
- Three channel-specific configuration parts

Further configurations for PollingMode and RSSI are available and can be modified in IDLEMode via an SPI command and/or User SW.

Figure 2-1 gives an overview on the service based-concept.

Figure 2-1. Service-based Concept Overview



2.1.2 Supported Telegrams

2.1.2.1 Telegram Structure

The Atmel® ATA8510/15 supports the transmission and reception of a wide variety of telegrams and protocols. Generally no special structure is required from a telegram to be received or transmitted by the Atmel ATA8510/15. However, designated hardware and software features are built in for the blocks that are depicted in Figure 2-2. Using this structure or parts of it can increase the sensitivity and robustness of the broadcast.

Figure 2-2. Telegram Structure

Desync:

The de-synchronization is usually a coding violation with a length of several symbols that should provoke a defined restart of the receiver. The use of a de-synchronization leads to more deterministic receiver behavior, reducing the required preamble length. This can be favorable in timing-critical and energy-critical applications.

Preamble:

The preamble is a pattern that is sent before the actual data payload to synchronize the receiver and provide the starting point of the payload. A very regular pattern (e.g., 1-0-1-0...) is recommended for synchronization (“wake-up pattern, WUP”, sometimes also called “pre-burst”) while a unique, well-defined pattern of up to 32 symbols is required to mark the start of the data payload (“start frame identifier, SFID” or “start bit”). In polling scenarios the WUP can be tens or hundreds of ms long.

Data Payload:

The data payload contains the actual information content of the telegram. It can be NRZ or Manchester-coded. The length of the payload is application dependent, typically 1..64 bytes.

Checksum:

A checksum can be calculated across the data payload to verify that the data have been received correctly. A typical example is an 8-bit CRC checksum. Data bits at the beginning of the payload can be excluded from the CRC calculation.

Stop Sequence:

The stop sequence is a short data pattern (typically 2 to 6 symbols) to mark the end of the telegram. A coding violation can be used to prevent additional (non-deterministic) data from being received.

2.1.2.2 NRZ and Manchester Coding

Within this document the following wording is used:

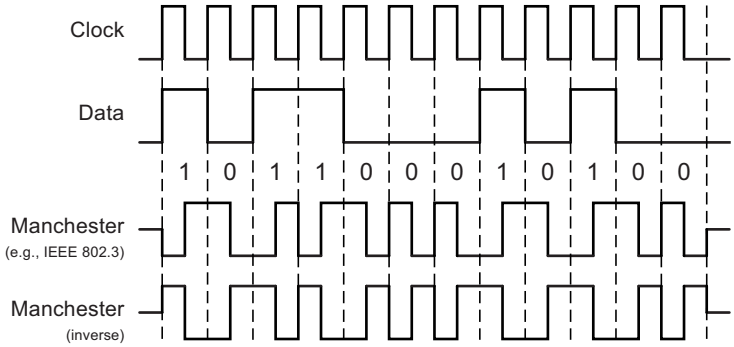
The expression data “bit” describes the real information content that is to be broadcast. This information can be coded in “symbols” (sometimes also called “chips”) which are then physically transmitted from sender to receiver. The receiver has to decode the “symbols” back into data “bits” to access the information. The “symbol rate” is therefore always greater or equal to the “bit rate”.

The Atmel ATA8510/15 supports two coding modes: Manchester coding and non-return-to-zero (NRZ) coding.

NRZ coding is implemented in a straightforward manner: One bit is represented by one symbol.

Manchester coding implements two symbols per data bit. There is always a transition between the two symbols of one data bit so that one data bit always consists of a “0” and a “1”. The polarity can be either way as shown in Figure 2-3 on page 13.

Figure 2-3. Manchester Code

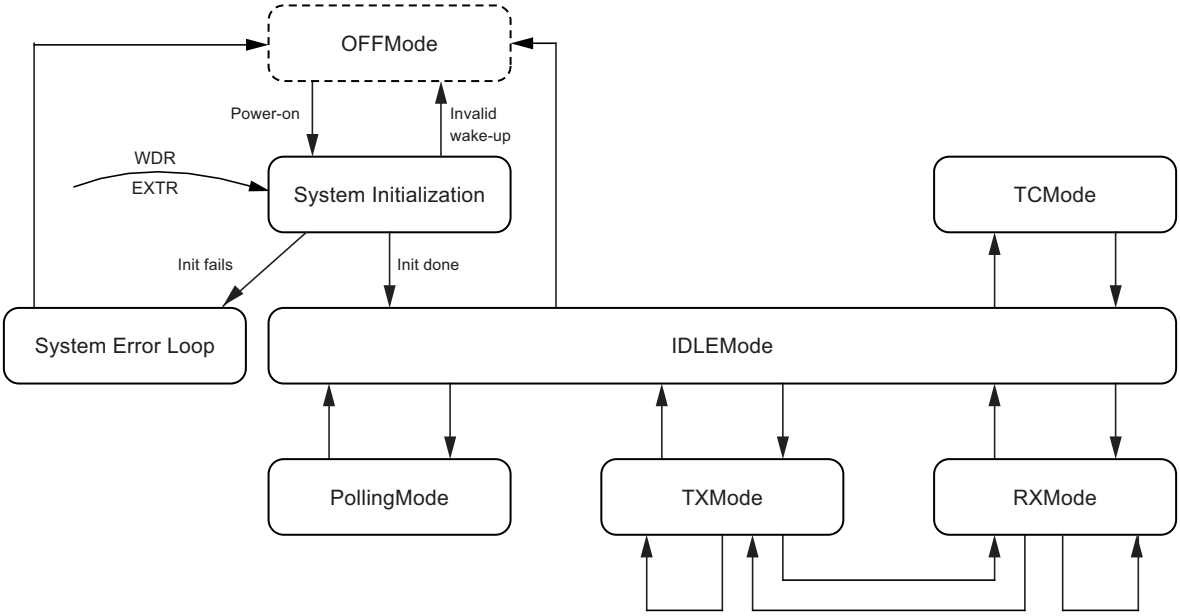


Manchester coding has many advantages such as simple clock recovery, no DC component, and error detection by code violation. Drawbacks are the coding/decoding effort and the increased symbol rate which is twice the data rate.

2.2 Operating Modes Overview

This section gives an overview of the operating modes supported by the Atmel® ATA8510/15 as shown in Figure 2-4.

Figure 2-4. Operating Modes Overview



After connecting the supply voltage to the VS pin, the Atmel ATA8510/15 always starts in OFFMode. All internal circuits are disconnected from the power supply. Therefore, no SPI communication is supported. The Atmel ATA8510/15 can be woken up by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence. After the system initialization the Atmel ATA8510/15 reaches the IDLEMode.

The IDLEMode is the basic system mode supporting SPI communication and transitions to all other operating modes. There are two options of the IDLEMode requiring configuration in the EEPROM settings:

- IDLEMode(RC) with low power consumption using the fast RC (FRC) oscillator for processing
- IDLEMode(XTO) with active crystal oscillator for high accuracy clock output or timing measurements

The transmit mode (TXMode) enables data transmission using the selected service/channel configurations. It is usually enabled by the SPI command “Set System Mode”, or directly after power-on, when selected in the EEPROM setting.

The receive mode (RXMode) provides data reception on the selected service/channel configuration. The precondition for data reception is a valid preamble. The receiver continuously scans for a valid telegram and receives the data if all pre-configured checks are successful. The RXMode is usually enabled by the SPI command “Set System Mode”, or directly after power-on, when selected in the EEPROM setting.

In PollingMode the receiver is activated for a short period of time to check for a valid telegram on the selected service/channel configurations. The receiver is deactivated if no valid telegram is found and a sleep period with very low power consumption elapses. This process is repeated periodically in accordance with the polling configuration. The initial settings are stored in the EEPROM and copied during firmware initialization to the SRAM. This allows modification of the PollingMode timing and service/channel configuration during IDLEMode.

The tune and check mode (TCMode) offers calibration and self-checking functionality for the VCO, and FRC oscillators as well as for antenna tuning, temperature measurement, and polling cycle accuracy. This mode is activated via the SPI command “Calibrate and Check”. When selected in the EEPROM settings, tune and check tasks are also used during system initialization after power-on. Furthermore, they can also be activated periodically during PollingMode.

Table 2-1 shows the relations between the operating modes and their corresponding power supplies, clock sources, and sleep mode settings.

Table 2-1. Operating Modes versus Power Supplies and Oscillators

Operation Mode	AVR Sleep Mode	DVCC	AVCC	XTO	SRC	FRC
OFFMode	-	off	off	off	off	off
IDLEMode(RC)	Active mode Power-down(1)	on	off off	off off	on on	on off
IDLEMode(XTO)	Active mode Power-down(1)		on on	on on	on on	off off
TXMode	Active mode		on	on	on	off
RXMode	Active mode		on	on	on	off
PollingMode(RC) - Active period - Sleep period	 Active mode Power-down(1)		 on off	 on off	 on on	 on off
PollingMode(XTO) - Active period - Sleep period	 Active mode Power-down(1)		 on on	 on on	 on on	 off off

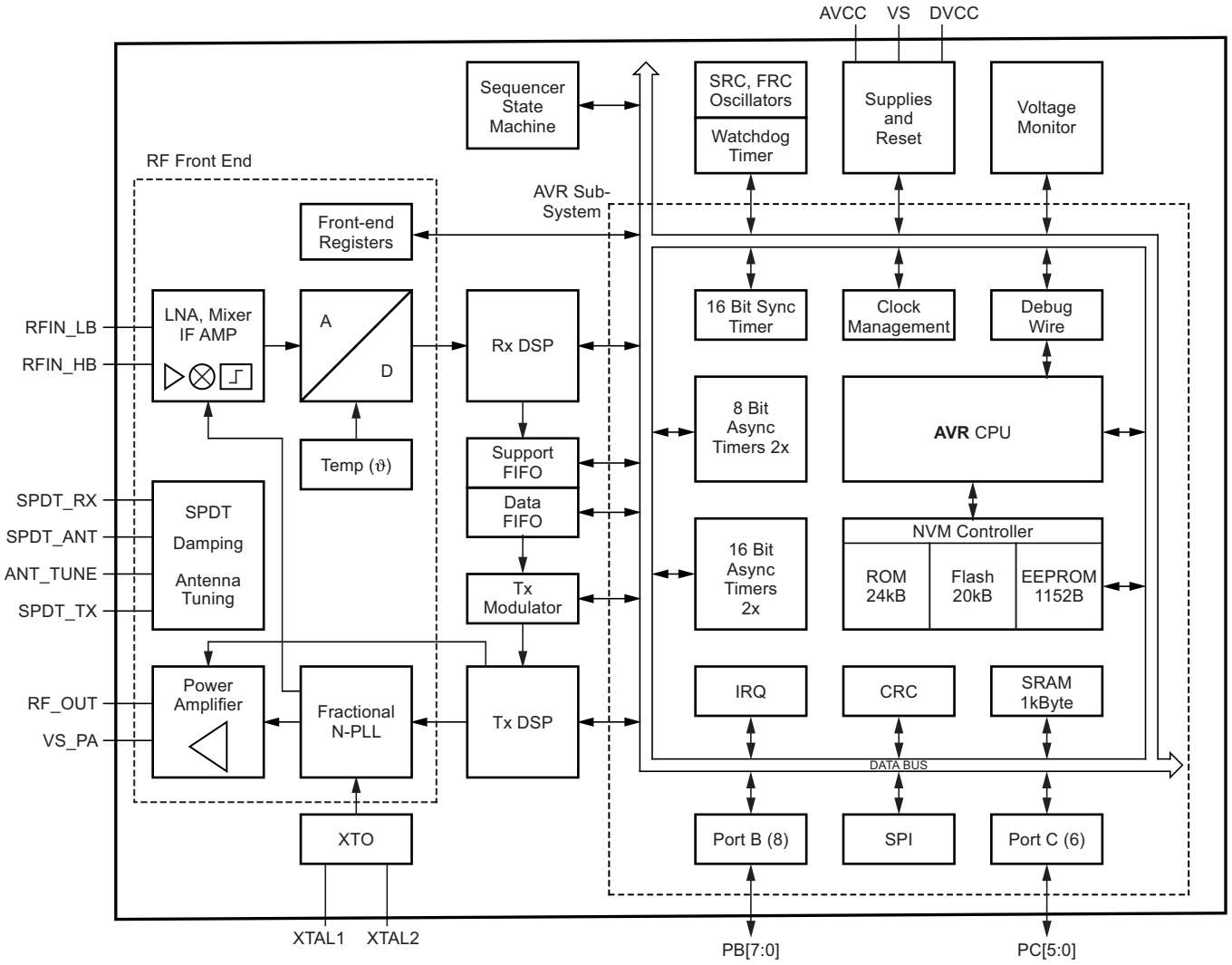
Notes: 1. During IDLEMode(RC) and IDLEMode(XTO) the AVR® microcontroller enters sleep mode to reduce current consumption. The sleep mode of the microcontroller section can be defined in the EEPROM. The power-down mode is recommended for keeping current consumption low.

3. Hardware

3.1 Overview

The Atmel® ATA8510/15 consists of an analog front end, digital signal processing blocks (DSP), an 8-bit AVR® sub-system and various supply modules such as oscillators and power regulators. A hardware block diagram of the Atmel ATA8510/15 is shown in Figure 3-1.

Figure 3-1. Block Diagram



Together with the fractional-N PLL, the crystal oscillator (XTO) generates the local oscillator (LO) signal for the mixer in RXMode. The RF signal comes either from the low-band input (RFIN_LB) or from the high-band input (RFIN_HB) and is amplified by the low-noise amplifier (LNA) and down-converted by the mixer to the intermediate frequency (IF) using the LO signal. A 10dB IF amplifier with low-pass filter characteristic is used to achieve enhanced system sensitivity without affecting blocking performance.

After the mixer, the IF signal is sampled using a high-resolution analog-to-digital converter (ADC).

Within the Rx digital signal processing (Rx DSP) the received signal from the ADC is filtered by a digital channel filter and demodulated. Two data receive paths, path A and path B, are included in the Rx DSP after the digital channel filter. In addition, the receive path can be configured to provide the digital output of an internal temperature sensor (Temp(ϑ)).

In TXMode the fractional-N PLL generates the Tx frequency. The power amplifier (PA) generates an RF output power signal programmable from –10dBm to +14dBm at RF_OUT. The FSK modulation is performed by changing the frequency setting of the fractional-N PLL dynamically with Tx digital signal processing (Tx DSP). Digital preemphasis and digital Gauss filtering can be activated in the Tx DSP in order to achieve higher data rates or reduce occupied bandwidth. The ASK modulation is performed by switching the power amplifier on and off. An ASK shaping filter is available to reduce the transmitted bandwidth of the modulated PA output signal. The shaping filter can also be used at the start and end of an FSK transmission.

With the single pole double throw (SPDT) switch the RF signal from the antenna is switched to RFIN in RXMode and from RF_OUT to the antenna in TXMode. An adjustable capacitor and an RF level detector on ANT_TUNE are used to tune the center frequency of loop antennas to reduce tolerances and capacitive proximity effects.

The system is controlled by an AVR® CPU with 24KB firmware ROM and 20KB user flash for the Atmel® ATA8510. 1024-byte EEPROM, 1024-byte SRAM, and other peripherals are supporting the transceiver handling. Two GPIO ports, PB[7:0] and PC[5:0], are available for external digital connections, for example, as an alternate function the SPI interface is connected to port B. The Atmel ATA8510/15 is controlled by the EEPROM configuration and SPI commands and the functional behavior is mainly determined by firmware in the ROM. Much of the configuration can be modified by the EEPROM settings. The firmware running on the AVR gives access to the hardware functionality of the Atmel ATA8510/15. Extensions to this firmware can be added in the 20KB of Flash memory for the Atmel ATA8510. The Rx DSP and Tx DSP registers are addressed directly and accessible from the AVR. A set of sequencer state machines is included to perform Rx and Tx path operations (such as enable, disable, receive, transmit) which require a defined timing parallel to the AVR program execution.

The power management contains low-dropout (LDO) regulators and reset circuits for the supply voltages VS, AVCC and DVCC, of the Atmel ATA8510/15. In OFFMode all the supply voltages AVCC and DVCC, are switched off to achieve very low current consumption. The Atmel ATA8510/15 can be powered up by activating the PWRON pin or one of the NPWRON[6:1] pins because they are still active in OFFMode. The AVCC domain can be switched on and off independently from DVCC. The Atmel ATA8510/15 includes two idle modes. In IDLEMode(RC) only the DVCC voltage regulator, the FRC and SRC oscillators are active and the AVR uses a power-down mode to achieve low current consumption. The same power-down mode can be used during the inactive phases of the PollingMode. In IDLEMode(XTO) the AVCC voltage domain as well as the XTO are additionally activated.

An integrated watchdog timer is available to restart the Atmel ATA8510/15 when it is not served within the configured time-out period.

3.2 Receive Path

3.2.1 Overview

The receive path consists of a low-noise amplifier (LNA), mixer, IF amplifier, analog-to-digital converter (ADC), and an Rx digital signal processor (Rx DSP). The fractional-N PLL and the XTO deliver the local oscillator frequency in RXMode. The receive path is controlled by the RF front-end registers.

Two separate LNA inputs, one for low-band and one for high-band, are provided to obtain optimum performance matching for each frequency range and to allow multi-band applications. A radio frequency (RF) level detector at the LNA output and a switchable damping included into the single-pole double-trough (SPDT) switch is used in the presence of large blockers to achieve enhanced system blocking performance.

The mixer converts the received RF signal to a low intermediate frequency (IF) of about 250kHz. A double-quadrature architecture is used for the mixer to achieve high image rejection. Additionally, the third-order suppression of the local oscillator (LO) harmonics makes receiving without a front-end SAW filter less critical, such as in a car key fob application.

An IF amplifier provides additional gain and improves the receiver sensitivity by 2-3dB. Because of built-in filter function, the in-band compression is degraded by 10dB, while the out-of-band compression remains unchanged.

The ADC converts the IF signal into the digital domain. Due to the high effective resolution of the ADC, the channel filter and received signal strength indicator (RSSI) can be realized in the digital signal domain. Therefore, no analog gain control (AGC) potentially leading to critical timing issues or analog filtering is required in front of the ADC. This leads to a receiver front end with excellent blocking performance up to the 1dB compression point of the LNA and mixer, and a steep digital channel filter can be used.

The Rx DSP performs the channel filtering and converts the digital output signal of the ADC to the baseband for demodulation. Due to the digital realization of these functions the Rx DSP can be adapted to the needs of many different applications. Channel bandwidth, data rate, modulation type, wake-up criteria, signal checks, clock recovery, and many other properties are configurable. The RSSI value is realized completely in the digital signal domain, enabling very high relative and absolute accuracy that is only deteriorated by the gain errors of the LNA, mixer, and ADC.

Two independent receive paths A and B are integrated in the Rx DSP after the channel filter and allow the use of different data rates, modulation types, and protocols without the need to power up the receive path more than once to decide which signal should be received. This results in a reduced polling current in several applications.

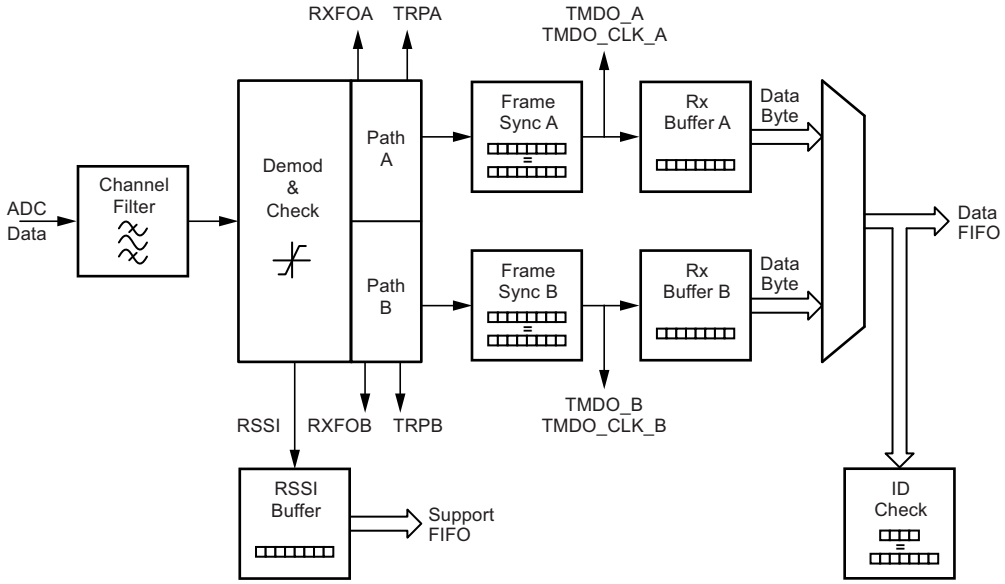
The integration of remote keyless entry (RKE), passive entry and go (PEG) and tire-pressure monitoring systems (TPM) into one module is simplified because completely different protocols can be supported and a low polling current is achieved. It is even possible to configure different receive RF bands for different applications by using the two LNA inputs. For example, a TPM receiver can be realized at 433.92MHz while a PEG system uses the 868MHz ISM band with multi-channel communication.

3.2.2 Rx Digital Signal Processing (Rx DSP)

The Rx digital signal processing (DSP) block performs the digital filtering, decoding, checking, and byte-wise buffering of the Rx samples that are derived from the ADC as shown in Figure 3-2. The Rx DSP provides the following outputs:

- Raw demodulated data at the TRPA/B pins
- Decoded data at the TMDO and TMDO_CLK pins
- Buffered data bytes toward the data FIFO and ID check block
- Auxiliary information about the signal such as the received signal strength indication (RSSI) and the frequency offset of the received signal from the selected center frequency (RXFOA/B)

Figure 3-2. Rx DSP Overview



The channel filter determines the receiver bandwidth. Its output is used for both receiving paths A and B, making it necessary to configure the filter to match both paths. The receiving paths A and B are identical and consist of an ASK/FSK demodulator with attached signal checks, a frame synchronizer which supports pattern-based searches for the telegram start and a 1-byte hardware buffer with integrated CRC checker for the received data.

Depending on the signal checks, one path is selected which writes the received data to the data FIFO and optionally to the ID check block.

The RSSI values are determined by the demodulator and written via the RSSI buffer to the support FIFO where the latest 16 values are stored for further processing.

3.3 Transmit Path

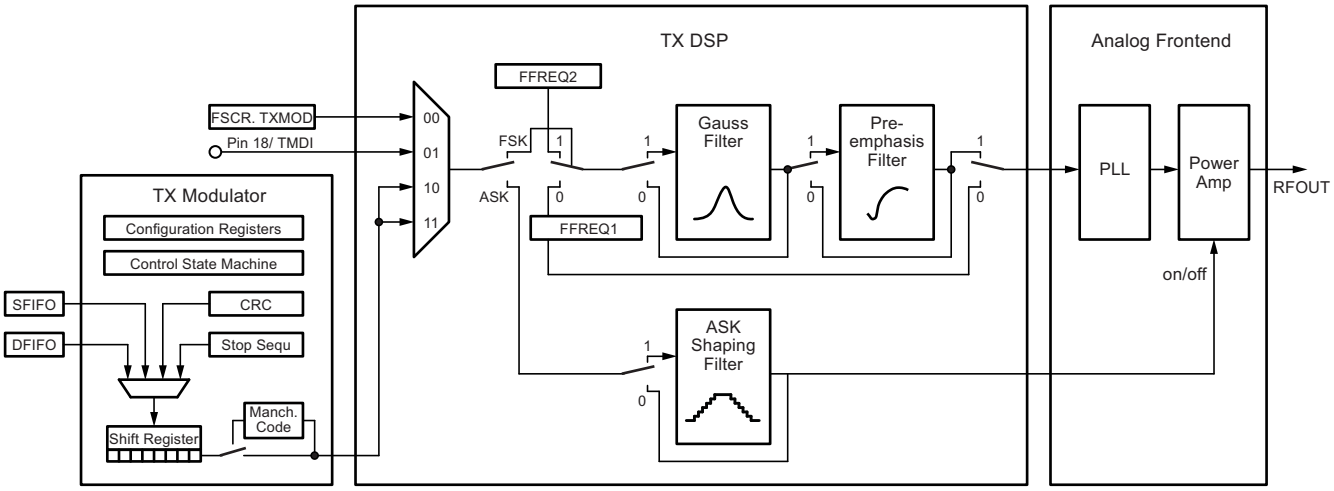
The Atmel® ATA8510/15 integrates a transmitter that is capable of sending data with various options:

- Frequency bands 310MHz to 318MHz, 418MHz to 477MHz, 836MHz to 956MHz
- Data rates up to 80kBit/s Manchester or 120Ksym/s NRZ in buffered and transparent mode
- ASK or FSK modulation
- Transparent or buffered mode
- ASK shaping filter
- Gauss-shaping digital filter

This section describes the hardware blocks that are integrated to perform the transmit functionality.

Figure 3-3 shows a block diagram of the transmit data path.

Figure 3-3. Transmit Data Path



The transmission data source can be selected from a register bit, the transparent input pin 18 (TMDI), and the Tx modulator that fetches the data from the DFIFO and SFIFO.

If ASK/OOK modulation is selected, the data stream is used to directly switch the power amplifier on and off. The transmitted carrier frequency is set by the PLL frequency synthesizer.

If FSK modulation is selected, the data stream is used to switch between two frequencies that are generated by the PLL frequency synthesizer. The power amplifier is constantly on. Power ramping (ASK shaping) can be used during on and off switching. To reduce the occupied bandwidth a digital Gauss-shaping filter can be enabled. For data rates above 20kHz Manchester or 40kHz NRZ-coding a digital preemphasis filter has to be enabled to compensate for the PLL loop filter.

3.4 AVR Controller

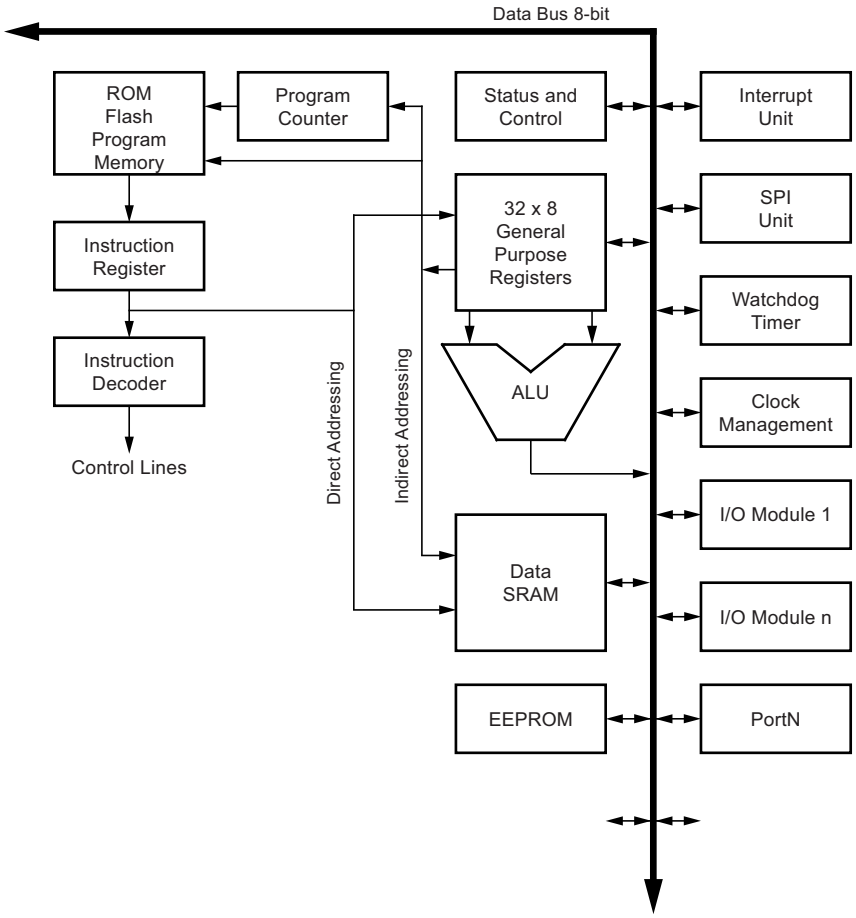
3.4.1 AVR Controller Sub-System

The AVR® controller sub-system consists of the AVR CPU core, its program memory, and a data bus with data memory and peripheral blocks attached. The receive path and the transmit path also have their user interfaces connected to the data bus.

3.4.2 CPU Core

The main function of the CPU core is to ensure correct program execution. For this reason, the CPU core must be able to access memories, perform calculations, control peripherals, and handle interrupts.

Figure 3-4. Overview of Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture—with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system reprogrammable Flash memory and ROM.

The fast-access register file contains 32 × 8-bit general purpose working registers with a single clock cycle access time. This allows a single-cycle arithmetic and logic unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed, and the result is stored back in the register file - in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in the Flash program memory. Referred to as ‘X,’ ‘Y,’ and ‘Z’ registers, these higher 16-bit function registers are described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The program flow is provided by conditional and unconditional jump and call instructions which are able to directly address the entire address space. Most AVR® instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

The program memory space is divided in two sections, the boot program section and the application program section. Both sections have dedicated lock bits for write and read/write protection. The store program memory (SPM) instruction that writes into the application Flash memory section must reside in the boot program section.

During interrupts and subroutine calls, the return address of the program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM—the stack size is thus only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the stack pointer (SP) in the reset routine before subroutines or interrupts are executed. The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as control registers, SPI, and other I/O functions. The I/O memory can be accessed directly, or as the data space locations following those of the register file, 0x20 - 0x5F. In addition, the circuit has extended I/O space from 0x60 - 0x1FF and SRAM where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

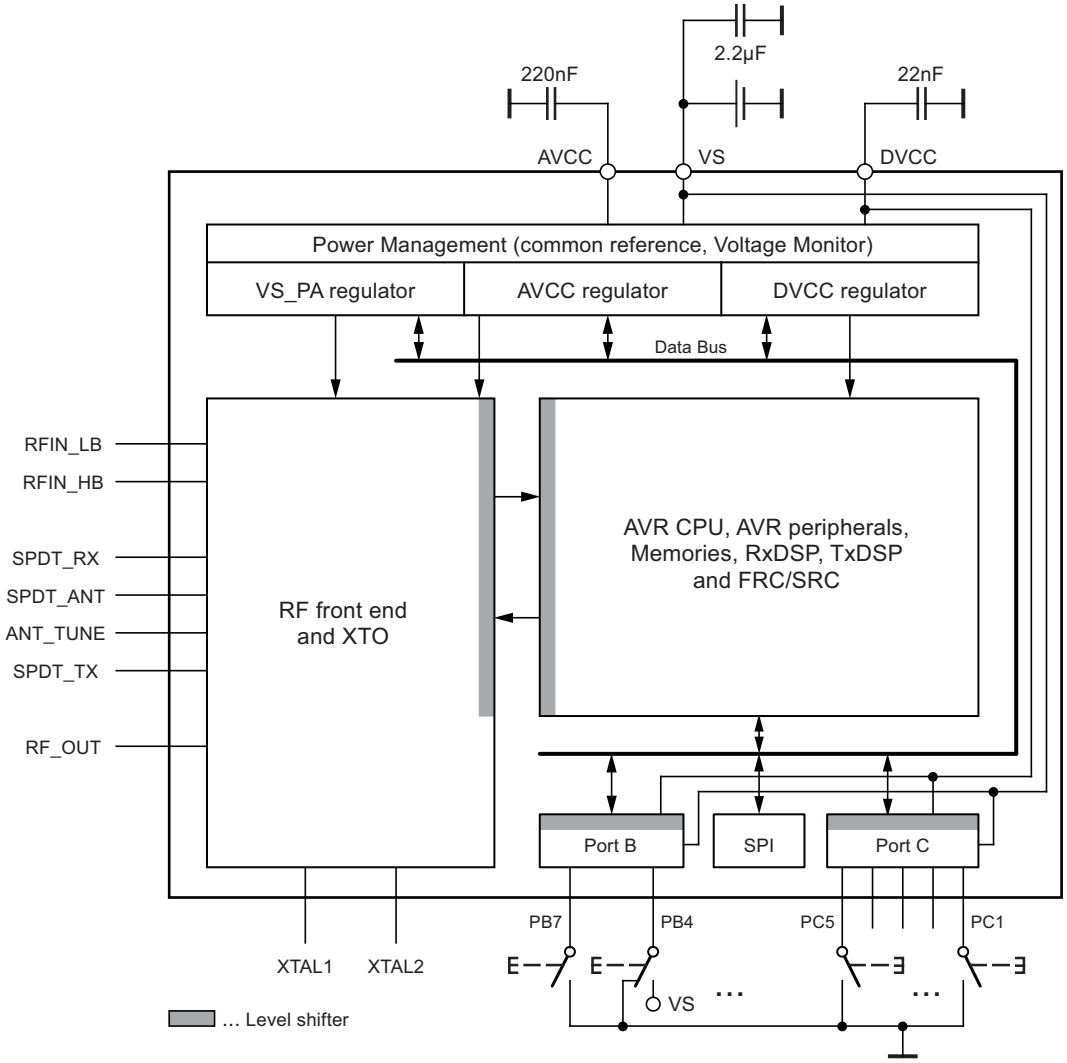
3.5 Power Management

The IC has four power domains:

1. VS – Unregulated battery voltage input
2. DVCC – Internally regulated digital supply voltage. Typical value is 1.35V.
3. AVCC – Internally regulated RF front end and XTO supply. Typical value is 1.85V.

The Atmel® ATA8510/15 can be operated from V_S= 1.9V to 3.6V.

Figure 3-5. Power Supply Management

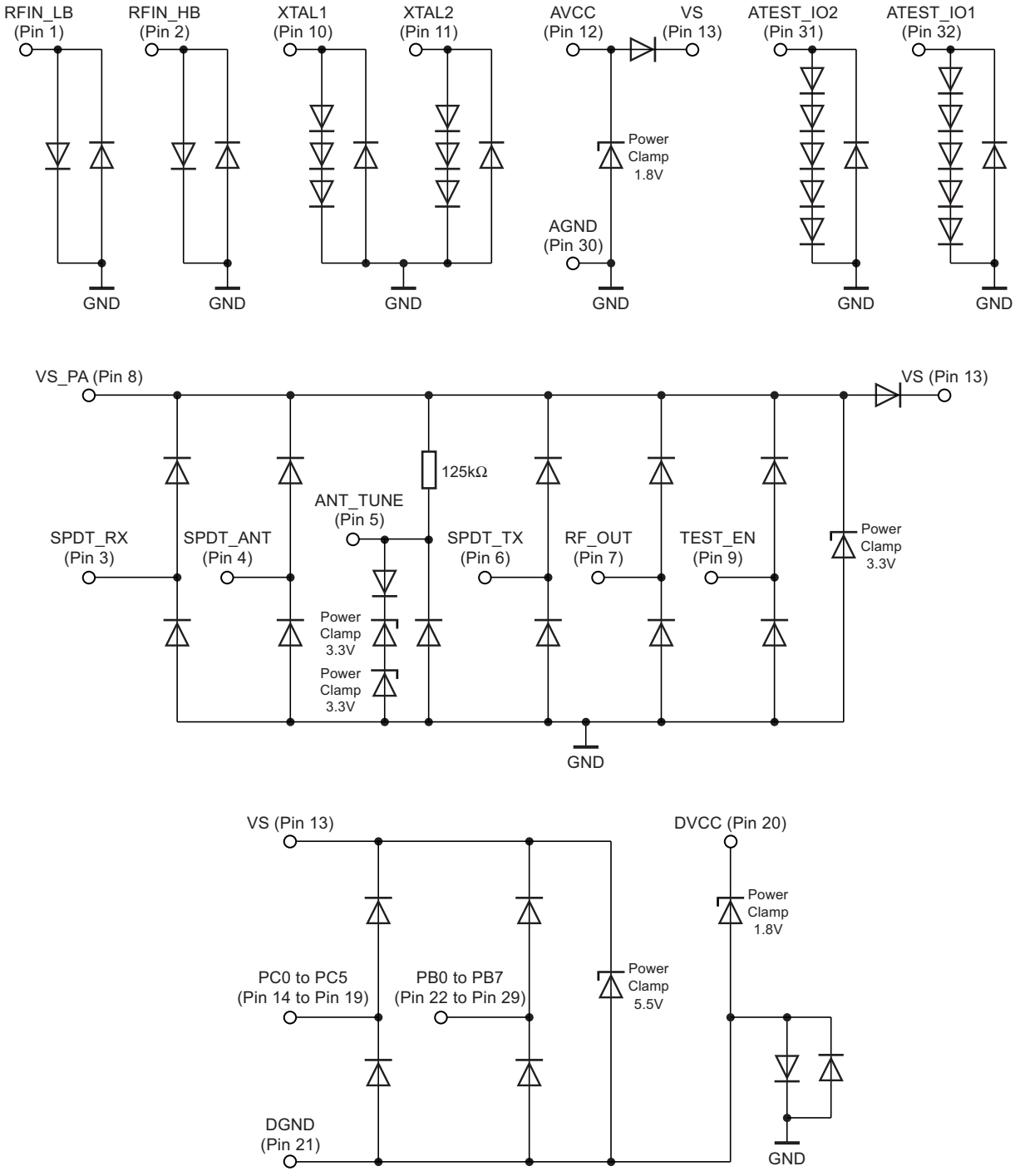


4. Electrical Characteristics

4.1 ESD Protection Circuits

GND is the exposed die pad of the Atmel® ATA8510/15 which is internally connected to AGND (pin 30). All zener diodes shown in Figure 4-1 (marked as power clamps) are realized with dynamic clamping circuits and not physical zener diodes. Therefore, DC currents are not clamped to the shown voltages.

Figure 4-1. Atmel ATA8510/15 ESD Protection Circuit



4.2 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	Tj		+150	°C
Storage temperature	Tstg	–55	+125	°C
Ambient temperature	Tamb	–40	+85	°C
Supply voltage	V_{VS}	–0.3	4.0	V
Supply voltage PA (1.9..3.6V application)	V_{VS_PA}	–0.3	4.0	V
Maximum input level (input matched to 50Ω)	P_{in_max}		+10	dBm
ESD (Human Body Model) all pins	HBM	–4	+4	kV
ESD (Machine Model) all pins	MM	–200	+200	V
ESD (Field Induced Charged Device Model) all pins	FCDM	–750	+750	V
Maximum RF amplitude at pin 5 (ANT_TUNE)(1)	ANTTUNE		4.0	Vp
Maximum peak voltage at pin 4 (SPDT_ANT)(1)	SPDTANT	–0.3	VS + 0.3	V
Maximum peak voltage at pin 6 (SPDT_TX)(1)	SPDTTX	–0.3	VS + 0.3	V

Note: 1. Customer application needs to be designed properly

4.3 Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal Resistance, Junction Ambient, Soldered according to JEDEC	R_{th_JA}	35	K/W

4.4 Supply Voltages and Current Consumption

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel® EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.00	Supply voltage range VS	3V application *1	13	V_{VS}	1.9	3.0	3.6	V	A
1.05	Supply voltage rise time		13	V_{VS_rise}			1	V/µs	D
1.10	Supply voltage range VS_PA	3V application *1	8	V_{VS_PA}	1.9	3	3.6	V	A
1.20	OFFMode Current consumption	3V application *1 T_{amb} = 25°C T_{amb} = 85°C	8, 13	$I_{OFFMode\_3V}$		5	150 600	nA nA	B B
1.30	IDLEMode(RC) Current consumption	SRC active, AVR in power-down mode, temperature range –40°C to +65°C	13	$I_{IDLEMode(RC)}$		50	90	µA	B
1.40	IDLEMode(XTO) Current consumption	XTO active, AVR in power-down mode	13	$I_{IDLEMode(XTO)}$		250	400	µA	B
1.60	IDLEMode(XTO) Current consumption	With active CLK_OUT f_{XTO}/6 = 4.05MHz $C_{LOAD\_CLK\_OUT}$ = 10pF V_{VS} = 3.6V AVR running with f_{XTO}/4 = 6.076MHz	13, 22	$I_{IDLEMode(XTO)\_CLK\_OUT2}$		1.3	2.5	mA	B
1.80	RXMode Current consumption	AVR running with f_{XTO}/4 f_{RF} = 315MHz *1 f_{RF} = 433.92MHz f_{RF} = 868.3MHz *1 f_{RF} = 915MHz *1	13	$I_{RXMode1}$		9.2 9.8 10.4 10.5	12.7 13.2 14.6 14.7	mA	B A A B
2.00	TXMode Current consumption	V_{VS} = 3V Pout = +6dBm f_{RF} = 315MHz *1 f_{RF} = 433.92MHz f_{RF} = 868.3MHz *1 f_{RF} = 915MHz *1 Pout = +10dBm *1 f_{RF} = 315MHz *1 f_{RF} = 433.92MHz f_{RF} = 868.3MHz *1 f_{RF} = 915MHz *1 Pout = +14dBm *1 f_{RF} = 315MHz *1 f_{RF} = 433.92MHz f_{RF} = 868.3MHz *1 f_{RF} = 915MHz *1	(7), 8, 13	I_{TXMode}		8.9 9.4 11.5 11.7 13.1 13.8 17.4 17.4 24.3 26.3 32.7 33.5	11 12 14.5 15 17 18.5 22.5 23 33 36 45 46	mA	B B B B B B B B B B B B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.5 RF Receiving Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with [*1].

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Frequency Ranges and Frequency Resolution of PLL for RXMode, TXMode and PollingMode									
3.00	RF operating frequency range 315MHz low-band	FECR.LBNHB = '1' FECR.S4N3 = '0'	1, 7	$f_{Range\_LB1\_315}$	310	315	318	MHz	A
3.10	RF operating frequency range 433MHz low-band	FECR.LBNHB = '1' FECR.S4N3 = '1'	1, 7	$f_{Range\_LB2\_433}$	418	433.92	477	MHz	B
3.30	RF operating frequency range High-band	FECR.LBNHB = '0' FECR.S4N3 = '0'	2, 7	$f_{Range\_B4\_868}$	836	868.3	956	MHz	B
3.40	Frequency resolution PLL	Low-band $f_{XTO}/2^{18}$ High-band $f_{XTO}/2^{17}$	1, 2, 7	DF_{PLL}		92.72 185.43		Hz	B B
RXMode and PollingMode Receive Characteristics IF bandwidth specifications are examples usable for parameter extrapolation if other IF bandwidth values are used									
4.00	Receiver 3dB bandwidth	Programmable digital IF filter	1, 2	BW_{IF}	25		366	kHz	B
4.10	ASK and FSK transparent mode data rate Manchester mode	at 25kHz IF-BW at 50kHz IF-BW at 80kHz IF-BW at 165kHz IF-BW at 237kHz IF-BW at 366kHz IF-BW	1, 2	DR_{TM}	0.25		7 14 20 50 80 80	Kbit/s	B B B B B B
4.20	Modulation index FSK	η = frequency_deviation / symbol_rate recommended	1, 2	η	0.5 0.75	1	360 1.25		B B
4.30	Frequency deviation	Maximum usable frequency deviation is baseband clock dependant f_{DEV_Max} = CLK_BB/8 at 25kHz IF-BW at 50kHz IF-BW at 80kHz IF-BW at 165kHz IF-BW at 237kHz IF-BW at 366kHz IF-BW	1, 2	f_{DEV}	 ±0.375 ±0.75 ±1.2 ±2.5 ±3.5 ±5.4		 ±9 ±18 ±26 ±60 ±93 ±93	kHz	 B B B B B B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.5 RF Receiving Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with [*1].

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.40	ASK and FSK transparent mode symbol rate NRZ mode	Used to receive NRZ, Keyloq, PPM, 1/3 2/3 Coded telegrams at 25kHz IF-BW at 50kHz IF-BW at 80kHz IF-BW at 165kHz IF-BW at 237kHz IF-BW at 366kHz IF-BW	1, 2	SR_{TM_OPT}	0.5		 14 28 40 100 160 160	 Ksym/s	 B B B B B B
4.70	Data rate tolerance FSK and ASK	Loss of sensitivity <1dB	1, 2	DR_{TOL}	–10		+10	%	B
4.80	Buffered data rate Manchester and NRZ mode	TMDO output will be buffered internally and readout via SPI interface Manchester mode NRZ mode	1, 2	$DR_{Buffered}$	 0.25 0.5		 80 120	 Kbit/s Ksym/s	 B B
4.90	FSK Sensitivity level 315MHz/ 433.92MHz Manchester encoded Receiving 100bit Packets with 9 of 10 Packets Error Free or BER = 10^-3 Continuous RX measured at TMDO output or buffered via SPI for DR < $DR_{Buffered}$	FSK at 25kHz IF bandwidth T_{amb} = 25°C 0.75Kbit/s ±0.75kHz 5Kbit/s ±2.4kHz	(1), 17, 19	 $SFSK_{B25\_R0.75}$ $SFSK_{B25\_R5\_2.4}$	–3dB	 –122.5 –113.5	+3dB	dBm	 B B
5.00		FSK at 80kHz IF bandwidth T_{amb} = 25°C 2.4Kbit/s ±2.4kHz 20Kbit/s ±20kHz	(1), 17, 19	 $SFSK_{B80\_R2\_4}$ $SFSK_{B80\_R20}$	–3dB	 –117 –108.5	+3dB	dBm	 B B
5.10		FSK at 165kHz IF bandwidth T_{amb} = 25°C 5Kbit/s ±5kHz 40Kbit/s ±40kHz	(1), 17, 19	 $SFSK_{B165\_R5}$ $SFSKB_{165\_R40}$	–3dB	 –114 –105.5	+3dB	dBm	 B B
5.20		FSK at 366kHz IF bandwidth T_{amb} = 25°C 20Kbit/s ±20kHz 80Kbit/s ±80 kHz	(1), 17, 19	 $SFSK_{B366\_R20}$ $SFSK_{B366\_R80}$	–3dB	 –107.5 –100.5	+3dB	dBm	 B B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.5 RF Receiving Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.30	ASK Sensitivity level 315MHz/ 433.92MHz Manchester encoded Receiving 100bit Packets with 9 of 10 Packets Error Free or BER = 10^-3 Continuous RX measured at TMDO output or buffered via SPI for DR < $DR_{Buffered}$	ASK at 25kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C 0.5Kbit/s 5Kbit/s	(1), 17, 19	$SASK_{B25\_R0\_5}$ $SASK_{B25\_R5}$	–3dB	–125 –117.5	+3dB	dBm	B B
5.40		ASK at 80kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C 1Kbit/s 20Kbit/s	(1), 17, 19	$SASK_{B80\_R1}$ $SASK_{B80\_R20}$	–3dB	–121.5 –110.5	+3dB	dBm	B B
5.50		ASK at 165kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C 1Kbit/s 40Kbit/s	(1), 17, 19	$SASK_{B165\_R1}$ $SASK_{B165\_R40}$	–3dB	–120.5 –107.5	+3dB	dBm	B B
5.60		ASK at 366kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C 1Kbit/s 80Kbit/s	(1), 17, 19	$SASK_{B366\_R1}$ $SASK_{B366\_R80}$	–3dB	–118.5 –103.5	+3dB	dBm	B B
5.70	Sensitivity change High-band	High-band 868.3MHz compared to low-band sensitivity to be added to min/typ/max values of parameters no. 4.90 to 5.60	(2)	ΔS_{HB}	1	1	1	dB	B
5.80	Sensitivity change Full ambient temperature range	T_{amb} = –40°C to +85°C Low-band *1 High-band $S = S_{FSK\_ASK} + \Delta S$	(1) (2)	ΔS_{Tamb_LB} ΔS_{Tamb_HB}	–1.5 –2		2 3	dB dB	C C
5.90	Sensitivity change NRZ	Compared to Machester NRZ using no more than 8 succeeding ‘0’ or ‘1’ symbols FSK ASK $S = S_{FSK\_ASK} + \Delta S$	(1, 2)	ΔS_{NRZ}	–1 0	0 2	2 4	dB	C C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.5 RF Receiving Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with [*1].

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6.00	Sensitivity change TRPA/B raw data	Compared to matched filter TMDO signal on pin 17, Manchester encoded ASK FSK $S = S_{FSK\_ASK} + \Delta S$	(1, 2), 16, 17, 19	ΔS_{RAW_DATA}		2.5 1.5		dB	B B
6.20	Sensitivity change for frequency deviations lower than configured	Configured for maximum f_{DEVM}· sensitivity degradation at f_{DEVM} / 3 compared to f_{DEVM} $S = S_{FSK\_ASK} + \Delta S$	(1, 2)	$\Delta S_{:fdevM\_3}$		2	3	dB	C
6.30	Value change from ASK level to OOK level	To calculate OOK values from ASK 100% level of carrier values Example: 2.4Kbit at 165kHz IF bandwidth ASK: 100% level of Carrier –117dBm = OOK: –111dBm $S_{OOK} = S_{ASK} + \Delta_{OOK}$	(1, 2)	Δ_{OOK}	6	6	6	dB	D
6.90	315MHz/ 433MHz blocking Manchester encoded useful signal level increased 3dB above sensitivity level blocking measured relative to useful signal level Receiving 100bit Packets with 9 of 10 Packets Error Free or BER = 10^-3 Continuous RX Excluding spurious receiving frequencies	At 25kHz IF bandwidth, FSK, T_{amb} = 25°C 2.4Kbit/s ± 2.4kHz	(1, 2)	fdist. ≥ 50kHz fdist. ≥ 100kHz fdist. ≥ 225kHz fdist. ≥ 450kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist. ≥ 10MHz		40 46 58 64 73 78 78		dBc	C C C C C C C
7.00		At 80kHz IF bandwidth, FSK, T_{amb} = 25°C 10Kbit/s ± 10kHz	(1, 2)	fdist. ≥ 150kHz fdist. ≥ 225kHz fdist. ≥ 450kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist. ≥ 10MHz		45 52 58 67 71 71		dBc	C C C C C C
7.10		At 165kHz IF bandwidth, FSK, T_{amb} = 25°C 20Kbit/s ± 20kHz	(1, 2)	fdist. ≥ 225kHz fdist. ≥ 450kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist. ≥ 10MHz		48 54 64 68 68		dBc	C C C C C
7.20		At 366kHz IF bandwidth, FSK, T_{amb} = 25°C 20Kbit/s ± 20kHz	(1, 2)	fdist. ≥ 500kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist. ≥ 10MHz		55 64 68 68		dBc	C C C C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.5 RF Receiving Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.30	868MHz/ 915MHz blocking Manchester encoded useful signal level increased 3dB above unblocked sensitivity level blocking measured relative to useful signal level	At 25kHz IF bandwidth, FSK, T_{amb} = 25°C 2.4Kbit/s ± 2.4kHz	(1, 2)	fdist. ≥ 50kHz fdist. ≥ 100kHz fdist. ≥ 225kHz fdist. ≥ 450kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist.>10MHz		34 40 52 58 67 75 75		dBc	C C C C C C C
7.40		At 80kHz IF bandwidth, FSK, T_{amb} = 25°C 10Kbit/s ± 10kHz	(1, 2)	fdist. ≥ 150kHz fdist. ≥ 225kHz fdist. ≥ 450kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist.>10MHz		39 46 52 62 68 68		dBc	C C C C C C
7.50	Receiving 100 Bit Packets with 9 of 10 Packets Error Free or BER = 10^-3	At 165kHz IF bandwidth, FSK, T_{amb} = 25°C 20Kbit/s ± 20kHz	(1, 2)	fdist. ≥ 225kHz fdist. ≥ 450kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist.>10MHz		42 48 58 65 65		dBc	C C C C C
7.60	Continuous RX Excluding spurious receiving frequencies	At 366kHz IF bandwidth, FSK, T_{amb} = 25°C 20Kbit/s ± 20kHz	(1, 2)	fdist. ≥ 500kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist.>10MHz		49 58 65 65		dBc	C C C C
7.70	Image rejection	Low-band High-band no adaptive algorithm used, therefore, numbers valid if large disturber applied before useful signal	(1, 2)	IM_{RED}	45 38	55 47		dB dB	A A
7.80	Blocking $3f_{LO}$, $5f_{LO}$	Low-band: $3 \times f_{LO} - f_{IF}$ $5 \times f_{LO} + f_{IF}$ High-band $3 \times f_{LO} - f_{IF}$ $5 \times f_{LO} + f_{IF}$	(1, 2)	BL_{NfLO}	27 28	32 33 39 45	37 38	dB	C C C C
7.90	Nominal IF frequency	RxDSP property depends on nominal RF frequency and DIV_IF $f_{IF} = f_{RF} / (DIV\_IF*6)$		f_{IF}	242	251	276	kHz	B
8.10	System input referred compression point	No AGC is used, therefore, the full dynamic is available receiving signals at sensitivity level on pin	(1, 2)	ICP_{1dB}		–45		dBm	B
8.20	System input referred 3rd-order intercept point	Low-band High-band	(1, 2)	IIP3		–35 –37		dBm	C

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Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.5 RF Receiving Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.30	Max, useful RX input level without damping	System works from sensitivity level up to that level with BER = 10^{-3}	(1, 2)	P_{In_max1}	–10	+10		dBm	C
8.40	Max. useful RX input level with damping	System works from sensitivity level up to that level with BER = 10^{-3}	4	P_{In_max2}	+5	+10		dBm	C
8.50	Input impedance	Measured on application board, RC parallel equivalent circuit 315MHz 433.92MHz 868.3MHz 915MHz	 1 1 2 2	Z_{in}	–20%	 870 2.9 400 2.9 340 1.4 330 1.4	+20%	 Ω pF Ω pF Ω pF Ω pF	 C C C C C C C C
8.60	LNA amplitude detector switch level	Firmware switches SPDT to damping on if a level above $S_{Gainswitch}$ is present during start of RXMode	(1, 2)	$P_{Gainswitch}$		–39		dBm	B
8.70	SPDT switch RX insertion loss	Damping off Sensitivity matching RF_IN with SPDT to 50Ω compared to matching RF_IN directly to 50Ω Low-band, 433.92MHz High-band, 868MHz	(3, 4)	IL_{Switch_RX}		 0.7 1.0	 1.1 1.4	 dB dB	 C C
8.80	SPDT switch RX damping ON	Same matching as parameter no. 8.70 This influences the blocking behavior if measured at pin 4 Low-band High-band	(3, 4)	D_{switch}	 14 17	 15 18	 16 19	 dB dB	 C C
8.90	LO spurious at LNA input	freq > 1GHz freq < 1GHz	(1, 2)	$P_{LO\_LNA\_IN}$		–60 –86	–50 –60	dBm	C C

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Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.5 RF Receiving Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.00	RSSI accuracy	$P_{RFIN\_LB(HB)}$ = –70dBm Low-band High-band	(1, 2), 4	$RSSI_{ABS\_ACCU}$	 –5.0 –5.5		 +5.0 +5.5	dB	B
9.10	RSSI relative accuracy	Measurement range –100dBm to –50dBm	(1, 2), 4	$RSSI_{REL\_ACCU}$	–1		+1	dB	B
9.20	RSSI resolution	DSP property	(1, 2), 4	$RSSI_{RES}$		0.5		dB/ value	D

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Pin number in brackets mean, that they are measured matched to 50Ω on the application board.

4.6 RF Transmit Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Frequency Ranges and Frequency Resolution of PLL									
See parameters 3.00 to 3.40 on page 25									
TXMode Transmit Characteristics									
10.00	Output power range	T_{amb} = 25°C	(7)	P_{Range}	–12		+14.5	dBm	B
10.10	Output power programming steps	Optimum load impedance for each power step. Up to two times higher steps for fixed load impedance.	(7)	ΔP_{OUT}		0.4		dB	C
10.20	Output power at 6dBm	T_{amb} = 25°C using 6dBm matching FEPAC = 35 (low-band) FEPAC = 36 (high-band)	(7)	P_{out_6dBm}	–1.5dB	6	+1.5dB	dBm	B
10.30	Output 2nd harmonic at 6dBm	T_{amb} = 25°C using 6dBm matching 315MHz, FEPAC = 35 433.92MHz, FEPAC = 35 868.3MHz, FEPAC = 36 915MHz, FEPAC = 36	(7)	$HM2_{6dBm}$		–30 –36 –35 -35		dBc	C C C C
10.40	Output 3rd harmonic at 6dBm	T_{amb} = 25°C using 6dBm matching 315MHz, FEPAC = 35 433.92MHz, FEPAC = 35 868.3MHz, FEPAC = 36 915MHz, FEPAC = 36	(7)	$HM3_{6dBm}$		–33 –41 –58 –58		dBc	C C C C
10.50	TXMode current consumption at 6dBm	6dBm matching 315MHz, FEPAC = 35 433.92MHz, FEPAC = 35 868.3MHz, FEPAC = 36 915MHz, FEPAC = 36	(7), 8, 13	I_{TXMode_6dBm}		8.7 9.1 11.5 11.7	11 12 14.5 15	mA	B B B B
10.60	Output power at 10dBm	T_{amb} = 25°C using 10dBm matching FEPAC = 46 (low-band) FEPAC = 47 (high-band)	(7)	P_{out_10dBm}	–1.5dB	10	+1.5dB	dBm	B
10.70	Output 2nd harmonic at 10dBm	T_{amb} = 25°C using 10dBm matching 315MHz, FEPAC = 46 433.92MHz, FEPAC = 46 868.3MHz, FEPAC = 47 915MHz, FEPAC = 47	(7)	$HM2_{10dBm}$		–24 –28 –24 –27		dBc	C C C C
10.80	Output 3rd harmonic at 10dBm	T_{amb} = 25°C using 10dBm matching 315MHz, FEPAC = 46 433.92MHz, FEPAC = 46 868.3MHz, FEPAC = 47 915MHz, FEPAC = 47	(7)	$HM3_{10dBm}$		–25 –34 –50 –55		dBc	C C C C

* Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = Characterized on samples, D = Design parameter. Pin numbers in brackets mean, that they are measured matched to 50Ω on the application board

4.6 RF Transmit Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.90	TXMode current consumption at 10dBm	10dBm matching 315MHz, FEPAC = 46 433.92MHz, FEPAC = 46 868.3MHz, FEPAC = 47 915MHz, FEPAC = 47	(7), 8, 13	I_{TXMode_10dBm}		13.1 13.8 17.4 17.4	17 18.5 22.5 23	mA	B B B B
11.00	Output power at 14dBm	T_{amb} = 25°C using 14dBm matching FEPAC = 56 (low-band) FEPAC = 57 (high-band)	(7)	P_{out_14dBm}	–1.5dB	14	+1.5dB	dBm	B
11.10	Output 2nd harmonic at 14dBm	T_{amb} = 25°C using 14dBm matching 315MHz, FEPAC = 56 433.92MHz, FEPAC = 56 868.3MHz, FEPAC = 57 915MHz, FEPAC = 57	(7)	$HM2_{14dBm}$		 –30 –30 –24 –24		dBc	 C C C C
11.20	Output 3rd harmonic at 14dBm	T_{amb} = 25°C using 14dBm matching 315MHz, FEPAC = 56 433.92MHz, FEPAC = 56 868.3MHz, FEPAC = 57 915MHz, FEPAC = 57	(7)	$HM3_{14dBm}$		 –30 –31 –50 –51		dBc	 C C C C
11.30	TXMode current consumption at 14dBm	14dBm matching 315MHz, FEPAC = 56 433.92MHz, FEPAC = 56 868.3MHz, FEPAC = 57 915MHz, FEPAC = 57	(7), 8, 13	I_{TXMode_14dBm}		24.3 26.3 32.7 33.5	33 36 45 46	mA	B B B B
11.40	Output power change 1 full temperature and supply voltage range	Low-band, High-band 0 to ≤10dBm V_{VS} = 3.0V V_{VS} = 1.9V to 3.6V $P = P_{out} + \Delta P$	(7)	$\Delta P_{TambVs1}$	 –1.5 –5.5		 +1.5 +2.5	dB	 C C
11.50	Output power change 2 full temperature and supply voltage range	High-band >10dBm to 14dBm V_{VS} = 3.0V V_{VS} = 2.1V to 3.6V $P = P_{out} + \Delta P$	(7)	$\Delta P_{TambVs2}$	 –3 –6		 +1.5 +3	dB	 C C
11.60	Spurious emission	Low-band: at $\pm f_{XTO}$ at $\pm f_{AVR}$ (f_{XTO} / 4) at $\pm f_{CLK\_OUT}$ (f_{XTO} / 6) High-band: at $\pm f_{XTO}$ at $\pm f_{AVR}$ (f_{XTO} / 4) at $\pm f_{CLK\_OUT}$ (f_{XTO} / 6)	(7)	SP_{TX}		 –80 –85 –80 –72 –85 –78	 –65 –65 –65 –60 –60 –60	dBc	 B C C B C C

* Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = Characterized on samples, D = Design parameter. Pin numbers in brackets mean, that they are measured matched to 50Ω on the application board

4.6 RF Transmit Characteristics (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with [*1].

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.70	TX transparent data rate in Manchester and NRZ mode	Manchester mode NRZ mode pre-emphasis enabled for symbol rates higher than 40Kbit	18, 7	$DR_{TX\_TM\_MAN}$ $DR_{TX\_TM\_NRZ}$			80 160	Kbit/s Ksym/s	B B
11.80	TX buffered data rate in Manchester and NRZ mode	Manchester mode NRZ mode		$DR_{TX\_BUF\_MAN}$ $DR_{TX\_BUF\_NRZ}$			80 120	Kbit/s Ksym/s	B B
11.90	TX buffered data rate programming step in Manchester and NRZ mode	AVR running with $f_{XTO}/4$	7	ΔDR_{BUF}			1	%	D
Antenna Tuning and SPDT in TXMode									
12.00	Antenna tuning capacitor range	FEAT.ANTN(3:0) = 0 to 15	5	C_{TUNE_RANGE}	4		9	pF	B
12.10	Antenna tuning capacitor resolution	4bits controlled with RF front-end register FEAT.ANT(3:0) available	5	C_{TUNE_RES}		0.16	0.2	pF	C
12.20	Antenna tuning series resistance	The series resistance influences the quality factor of the loop antenna and causes radiated Tx power losses	5	$C_{TUNE\_SRESIST}$		2.5	4	Ω	C
12.30	Antenna tuning maximum RF amplitude	If higher levels occur in application an external capacitor to GND is needed to reduce the amplitude.	5	$C_{TUNE\_RFAMP\_MAX}$			3	V_p	D
12.40	SPDT insertion loss TX	Transmitted power using matching RF_OUT with SPDT to 50Ω compared to matching RF_OUT directly to 50Ω Low-band High-band	(4, 6)	IL_{Switch_TX}		 0.5 0.7	 1.1 1.2	 dB dB	 C C
12.45	Maximum peak voltage on SPDT_ANT (pin 4)		4	$V_{PEAK\_SPDT\_ANT}$	–0.3		VS + 0.3	V	D
12.50	Maximum peak voltage on SPDT_TX (pin 6)		6	$V_{PEAK\_SPDT\_TX}$	–0.3		VS + 0.3	V	D

* Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = Characterized on samples, D = Design parameter. Pin numbers in brackets mean, that they are measured matched to 50Ω on the application board

4.7 Oscillators and CLK_OUT

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances, quartz parameters C_m = 4fF and C_0 = 1pF unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13.00	CLK_OUT equivalent internal capacitance	Used for current calculation	13, 22	C_{CLK}		7.5	10	pF	C
13.10	Supply current increase CLK_OUT active	Calculation can be applied to all operation modes except OFFMode	13	ΔI_{CLK}	$(C_{CLK} + C_{LOAD\_CLK\_OUT}) \times V_{VS} \times f_{OUT}$			A	C
13.30	XTO frequency range		10, 11	f_{xto}	23.8	24.305	26.2	MHz	C
13.40	XTO pulling due to internal capacitance and XTO tolerance	C_m = 4fF, T_{amb} = 25°C	10, 11	ΔF_{XTO1}	–10		+10	ppm	B
13.50	XTO pulling due to temperature and supply voltage	C_m = 4fF T_{amb} = –40°C to +85°C	10, 11	ΔF_{XTO2}	–4		+4	ppm	B
13.60	Maximum C_0 of XTAL	XTAL parameter	10, 11	C_{0_max}		1	2	pF	D
13.70	XTAL, C_m motional capacitance	XTAL parameter	10, 11	C_m		4	10	fF	D
13.80	XTAL, real part of XTO impedance at start-up	C_m = 4fF, C_0 = 1pF	10, 11	R_{m_start1}	950			Ω	B
13.90	XTAL, real part of XTO impedance at start-up	C_m = 4fF, C_0 = 1pF, T_{amb} < 85°C	10, 11	R_{e_start2}	1100			Ω	B
14.00	XTAL, maximum R_m after start-up	XTAL parameter	10, 11	R_{m_max}	110			Ω	D
14.10	Internal load capacitors	Including ESD and package capacitance. XTAL has to be specified for 7.5pF load capacitance (incl. 1pF PCB capacitance per pin)	10, 11	C_{L1}, C_{L2}	13.3	14	14.7	pF	B
14.20	Slow RC oscillator frequency	Polling cycle can be calibrated ±2% accurate with f_{XTO}	22	f_{SRC}	–10%	125	+10%	kHz	A
14.30	Fast RC oscillator frequency	FRC oscillator can be calibrated ±2% accurate with f_{XTO}	22	f_{FRC}	–5%	6.36	+5%	MHz	A

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

4.8 I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with [*1].

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
15.00	Input low voltage	PC0 to PC5 PB0 to PB7	14-19 22-29	V_{IL}	–0.3		0.2 x V_{VS}	V	A
15.05	Input low leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19 22-29	I_{IL}			–1	µA	A
15.10	Input high voltage	PC0 to PC5 PB0 to PB7	14-19 22-29	V_{IH}	0.8 x V_{VS}		V_{VS} + 0.3	V	A
15.15	Input high leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19 22-29	I_{IH}			1	µA	A
15.20	Output low voltage	I_{OL} = 0.2mA	14-19 22-29	V_{OL_3V}			0.1 x V_{VS}	V	A
15.30	Output high voltage	I_{OH} = –0.2mA	14-19 22-29	V_{OH_3V}	0.9 x V_{VS}			V	A
15.40	I/O pin pull-up resistor	OFFMode: see port B and port C	14-19 22-29	R_{PU}	30	50	70	kΩ	A
15.50	Output low voltage for strong LED low-side driver (PB7)	Configurable on pin PB7 I_{LOAD} = 1.5mA	29	V_{OL_STR1}			0.1 x V_{VS}	V	A
15.60	Output high voltage for strong LED/LNA high-side driver (PB7, PB4)	Configurable on pin PB7 and PB4 I_{LOAD} = –1.5mA	26, 29	V_{OH_STR1}	0.9 x V_{VS}			V	A
15.70	Output low voltage for strong ISP low-side driver (PB3)	Activated in ISP mode I_{OL} = 1.7mA, V_{Vs} > 2.5V T_{amb} = –40°C to +65°C	25	V_{OL_STR2}			0.1 x V_{VS} 0.1 x V_{VS}	V V	B B
15.80	Output high voltage for strong ISP high-side driver (PB3)	Activated in ISP mode I_{OH} = –1.7mA, V_{Vs} > 2.5V T_{amb} = –40°C to +65°C	25	V_{OH_STR2}	0.9 x V_{VS} 0.9 x V_{VS}			V V	B B
15.90	CLK_OUT output frequency	XTO, FRC or SRC related clock f_{CLK_OUT} = f_{OSC}/(2*CLKOD)	22	f_{CLK_OUT}			4.5	MHz	B
16.00	CLK_OUT duty cycle	$C_{LOAD\_CLK\_OUT}$ = 10pF f_{CLK_OUT} = 4.5MHz	22	DTY_{CLK_OUT}	45		55	%	A
16.10	I/O pin output delay time (rising edge)	3V application C_{Load} = 10pF	14-19 22-29	$T_{del\_rise\_3V}$	13.6	17.5	22.4	ns	D
16.20	I/O pin rise time (0.1 × V_{VS} to 0.9 × V_{VS})	3V application C_{Load} = 10pF	14-19 22-29	T_{rise_3V}	20.7	23.9	28.4	ns	D
16.30	I/O pin slew rate (rising edge)	3V application C_{Load} = 10pF	14-19 22-29	$T_{sr\_rise\_3V}$	0.115	0.100	0.084	V/ns	D

*) Type means: A = 100% tested at voltage and temperature limits, B = 100 % correlation tested, C = Characterized on samples, D = Design parameter

4.8 I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5 (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
16.40	I/O pin output delay time (falling edge)	3V application C_{Load} = 10pF	14-19 22-29	$T_{del\_fall\_3V}$	13.7	17.4	22.7	ns	D
16.50	I/O pin fall time (0.9 × V_{VS} to 0.1 × V_{VS})	3V application C_{Load} = 10pF	14-19 22-29	T_{fall_3V}	16.2	19.2	22.5	ns	D
16.60	I/O pin slew rate (falling edge)	3V application C_{Load} = 10pF	14-19 22-29	$T_{sr\_fall\_3V}$	0.148	0.125	0.106	V/ns	D

*) Type means: A = 100% tested at voltage and temperature limits, B = 100 % correlation tested, C = Characterized on samples, D = Design parameter

4.9 Hardware Timings

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to + 85°C, V_{VS} =1.9V to 3.6V over all process tolerances. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz. Standard Atmel EEPROM Settings are used if marked with *1.

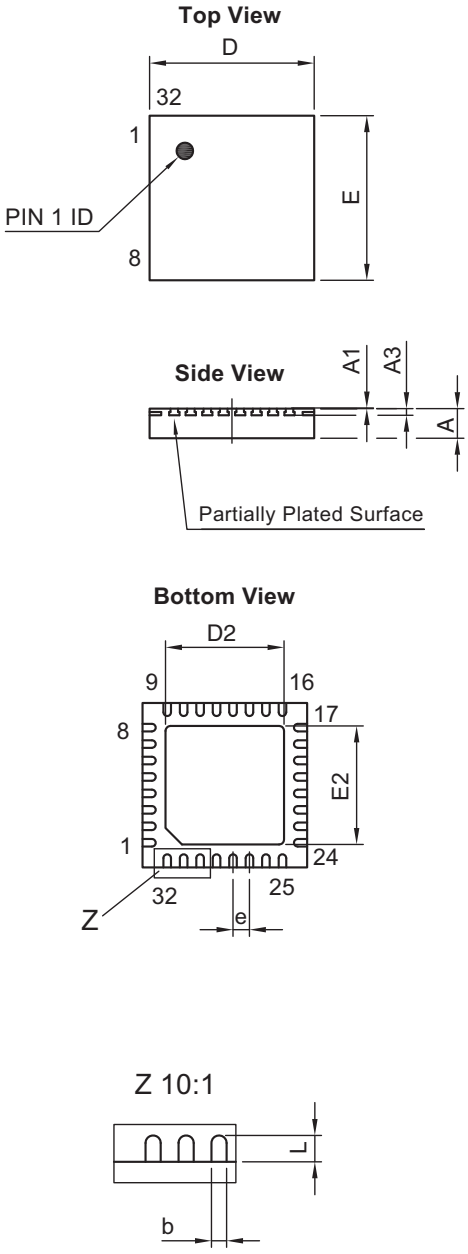
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
17.00	Start-up Time XTO	AVCC already enabled and ready C0 < 1.5pF 4fF < Cm < 15fF R_m < 110Ω R_m < 800Ω	10, 11	T_{Start_XTO}	90	130	250 1500	µs µs	B C
17.10	Erase and Write EEPROM	using ISP commands or SPI command “Write EEPROM”	14, 23, 24, 25	$T_{EE\_ER\_WR}$			10	ms	B
17.20	Erase Only EEPROM	using ISP commands	14, 23, 24, 25	T_{EE_ER}			5	ms	B
17.30	Write Only EEPROM	using ISP commands	14, 23, 24, 25	T_{EE_WR}			5	ms	B
17.50	System Initialisation Startup Time	PWRON = ‘1’ or NPWRON = ‘0’ to INTERNAL RESET removal	13,20	$T_{SYSINIT1}$	80		200	µs	B

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

5. Ordering Information

Extended Type Number	Package	Remarks
ATA8510-GHQW	QFN32	5mm × 5mm, 6k tape and reel, PB-free, 20Kbyte user Flash
ATA8515-GHQW	QFN32	5mm × 5mm, 6k tape and reel, PB-free

6. Package Information



technical drawings according to DIN specifications

Dimensions in mm

Two Step Singulation process

COMMON DIMENSIONS (Unit of Measure = mm)				
SYMBOL	MIN	NOM	MAX	NOTE
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	4.9	5	5.1	
D2	3.5	3.6	3.7	
E	4.9	5	5.1	
E2	3.5	3.6	3.7	
L	0.35	0.4	0.45	
b	0.2	0.25	0.3	
e		0.5		

10/18/13

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: VQFN_5x5_32L** Exposed pad 3.6x3.6		6.543-5124.03-4	1

7. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9315G-INDCO-08/15	• Section 2.2 “Operating Modes Overview” on pages 13 to 14 updated
9315F-INDCO-11/14	• Section 4.4 “Supply Voltages and Current Consumption” on page 24 updated • Section 4.8 “I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5” on pages 36 to 37 updated • Section 5 “Ordering Information” on page 38 updated
9315E-INDCO-09/14	• Section 4.5 “RF Receiving Characteristics” on pages 25 to 31 updated • Section 6 “Package Information” on page 38 updated
9315D-INDCO-07/14	• Features on page 2 updated • Section 1.3 “Pinning” on pages 5 to 6 updated • Section 1.4 “Typical Applications” on pages 9 to 10 updated • Section 2.2 “Operating Modes Overview” on page 15 updated • Section 3 “Hardware” on pages 16 to 17 updated • Section 3.5 “Power Management” on page 22 updated • Section 4 “Electrical Characteristics” on pages 22, 23, 34 and 35 updated
9315C-INDCO-04/14	• “Atmel Confidential” removed on all pages
9315BX-INDCO-03/14	• ATA8505 renamed to ATA8515 on all pages • Section 5 “Ordering Information” on page 38 updated

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