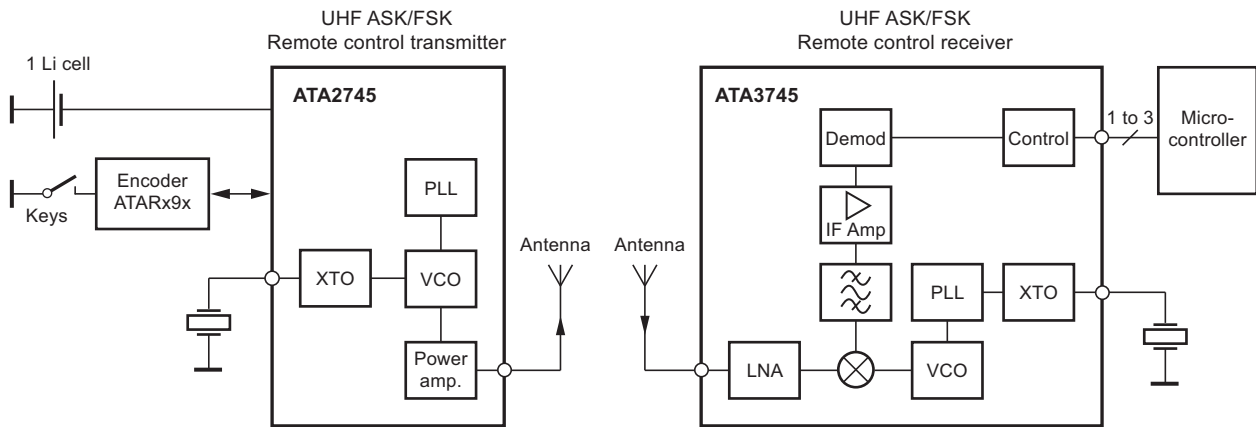
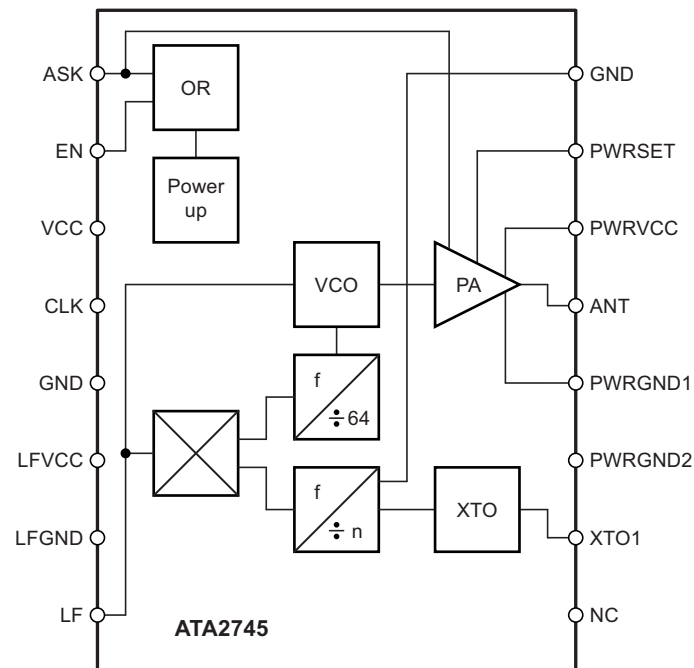


**Figure 1-1.** System Block Diagram

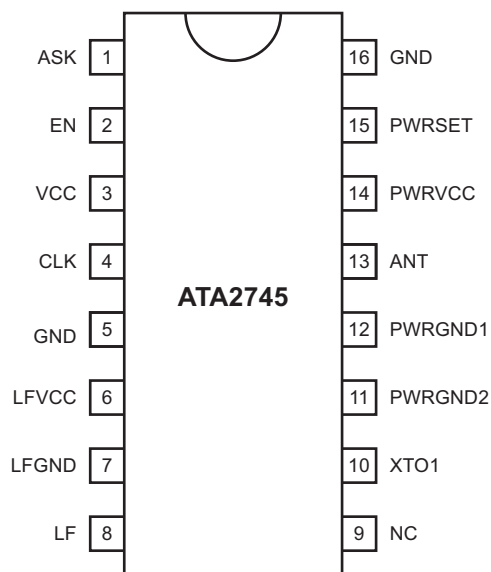


**Figure 1-2.** Block Diagram



## 2. Pin Configuration

**Figure 2-1.** Pinning SSO16



**Table 2-1.** Pin Description

Pin	Symbol	Function
1	ASK	Modulation input ASK
2	EN	Enable input
3	VCC	Supply voltage
4	CLK	Clock output
5	GND	Ground
6	Lfvcc	Supply voltage VCO
7	LFGND	VCO ground
8	LF	Circuit PLL loop
9	NC	Not connected
10	XTO1	Connection for crystal
11	PWRGND2	Power GND2
12	PWRGND1	Power GND1
13	ANT	RF output
14	PWRVCC	Supply voltage power amplifier
15	PWRSET	Applied to VCC
16	GND	Ground

### 3. General Description

The fully integrated VCO and the single-ended open-collector output allow particularly simple, low-cost RF miniature transmitters to be assembled. The single-ended output enables a considerably simplified adaptation of both a magnetic loop antenna of any form or a  $\lambda / 4$  antenna. This is because the load impedance must not be balanced as would be the case with a differential output.

The XTO's frequency can be selected to be either 13.56 MHz or 9.844 MHz (USA). At these frequencies, crystals have a very fast start-up time ( $< 1.5$  ms), whereby a wait time of 5 ms to 10 ms is required until the transmitter IC is locked. This means that the processor does not need to poll a lock detect output.

### 4. Functional Description

#### 4.1 ASK Transmission

The ATA2745 is activated by  $EN = V_S$ .  $V_{ASK}$  must remain 0V for 5 ms, then the output power can be modulated by means of pin ASK.  $V_{EN}$  remains equal to  $V_S$  during the transmission of the message. The ASK input activates the power amplifier and the PLL.

#### 4.2 Take-over of the Clock Pulse in the Microcontroller

The clock of the crystal oscillator can be used for clocking the microcontroller. The ATAR090 and ATAR890 have the special feature of starting with an integrated RC oscillator to switch on the ATA2745 with  $V_{EN} = V_S$ . 5 ms later, the 3.39-MHz clock frequency is present, so that the message can be sent with crystal accuracy.

### 5. Application Circuit

The following component values are recommendations for a typical application.  $C_4$ ,  $C_5$ , and  $C_6$  are block capacitors. The values of these capacitors depend on the board layout.  $C_4 = 1$  nF,  $C_5 = 1$  nF, and  $C_6 = 22$  nF are typically used here. For  $C_5$ , the impedance between  $f = 100$  MHz and  $f = 1$  GHz should be as low as possible.

$C_{Loop1}$  and  $C_{Loop2}$  are selected so that the antenna oscillates in resonance and the matching to the appropriate impedance transformation is possible.

$L_{Feed}$  is an inductor for the antenna's DC current supply. A typical value is  $L_{Feed} = 220$  nH.  $L_{Feed}$  can be either printed on the PC board or be a discrete component.

## 5.1 Output Power Measurement

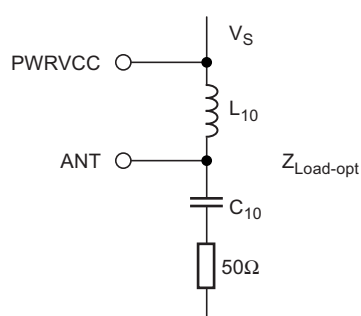
The following output network (Figure 5-1 on page 5) can be used for output power evaluation, the exact values of  $L_{10}$  and  $C_{10}$  are dependent on the layout.

$L_{10}$  and  $C_{10}$  form the transformation network to adopt the output impedance of the IC to  $50\Omega$ . The following table shows the values for an output power of 2 mW and an  $R_{PWRSET} = 1.2\text{ k}\Omega$ .

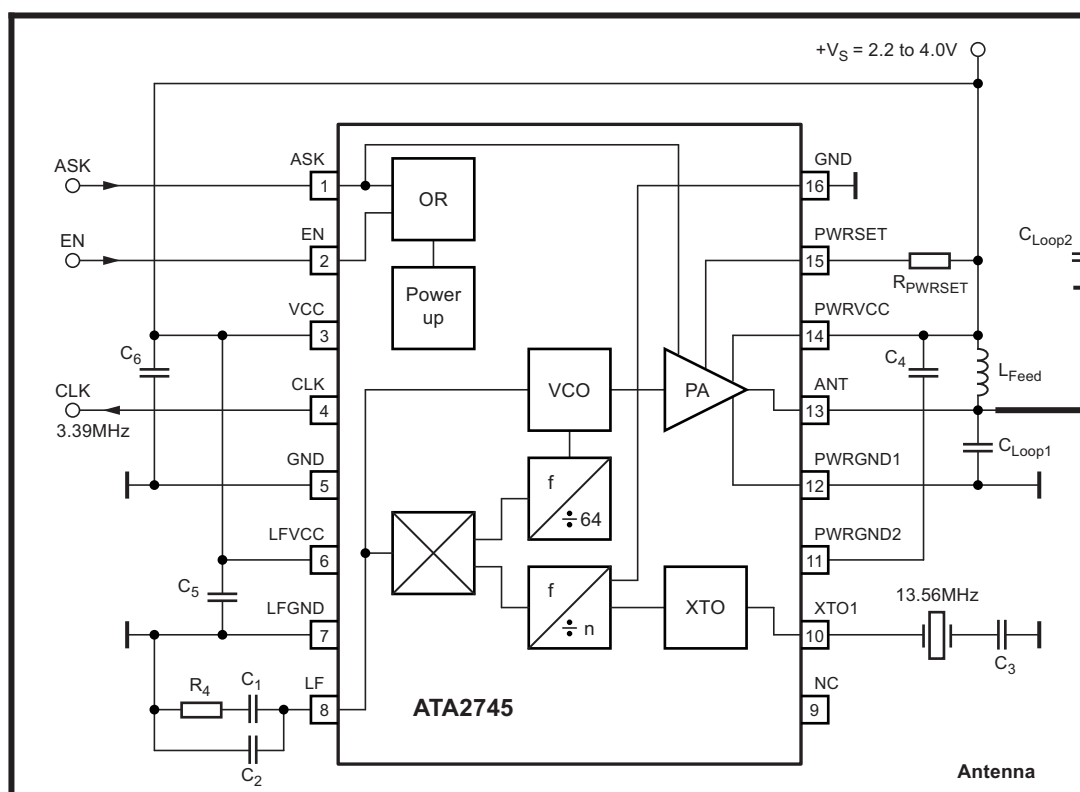
**Table 5-1.** Transformation Network

f [MHz]	C10 [pF]	L10 [nH]	$Z_{Load-opt}$ [ $\Omega$ ]
315	2.7	56	$260 + j330$
433.92	1.8	33	$185 + j268$

**Figure 5-1.** Measurement Output Network



**Figure 5-2.** Application Circuit



## 6. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	$V_S$		6	V
Power dissipation	$P_{tot}$		250	mW
Junction temperature	$T_J$		150	°C
Storage temperature	$T_{stg}$	–55	125	°C
Ambient temperature	$T_{amb}$	–40	85	°C

Electrostatic sensitive device.  
Observe precautions for handling.



## 7. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	180	K/W

## 8. Electrical Characteristics

All parameters are referred to GND (pin 5),  $V_S = 3V$ ,  $T_{amb} = 25^\circ C$ , unless otherwise specified

The possible operating ranges refer to different circuit conditions:  $V_S = 2.2V$  to  $4.0V$  at  $T_{amb} = -40^\circ C$  to  $+85^\circ C$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply current (power down)	$V_{ASK}, V_{FSK} \leq 0.3V, V_S < 3.6V$	$I_{Soff}$		2	10	$\mu A$
Supply current (power up, output OFF)	$V_{ASK} = GND, V_{EN} = V_S, V_S = 3V$	$I_{Son}$		4.7	6.2	mA
Supply current (power up, output ON)	$V_{ASK} = V_S, V_S = 3V, R_{PWRSET} = 1.2 k\Omega$	$I_{Stransmit}$		10	12.5	mA
Output power	$V_S = 3V, T_{amb} = 25^\circ C, f = 433.92 MHz$ $R_{PWRSET} = 1.2 k\Omega$	$P_{Ref}$	1	3	5	dBm
Output power variation for $f = 315 MHz$ compared to $f = 433.92 MHz$	$f = 315 MHz$ $P_{out} = P_{Ref} + \Delta P_{Ref}$	$\Delta P_{Ref}$		1.5		dB
Maximum peak output antenna voltage	At $P_{out} = 2.0 mW$ , the load impedance must be selected to meet the $V_{out}$ maximum requirement, the supply current is not dependent on the load impedance tolerance	$V_{outmax}$		$V_S - 0.7V$		$V_{(peak)}$
Spurious emission	$f_o \pm (n \times f_{PC})$ where $f_{PC} = 6.78 MHz$ Load capacitance at CLK $\leq 3 pF$ $f = 230 MHz$ to $470 MHz$ $f < 230 MHz, f > 470 MHz$	Em Em			–40 –58	dBc dBc
Oscillator frequency XTO	Crystal frequency = 13.56 MHz	$f_{XTO}$	13.56 – 30 ppm	13.56	13.56 + 30 ppm	MHz

## 8. Electrical Characteristics (Continued)

All parameters are referred to GND (pin 5),  $V_S = 3V$ ,  $T_{amb} = 25^{\circ}C$ , unless otherwise specified

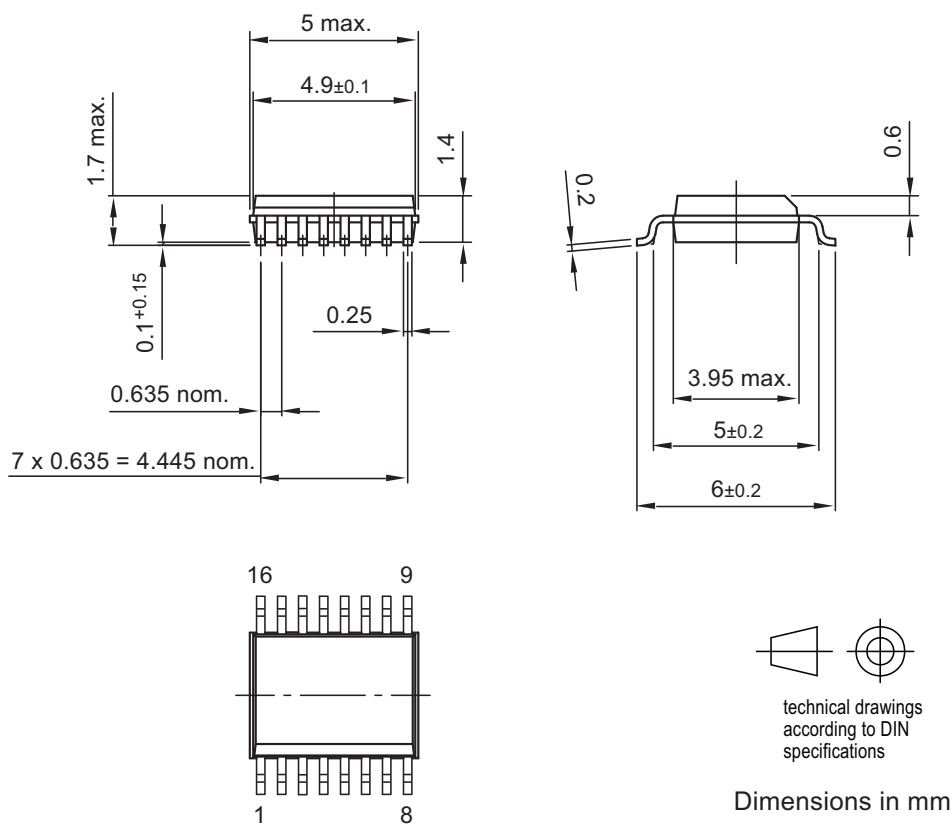
The possible operating ranges refer to different circuit conditions:  $V_S = 2.2V$  to  $4.0V$  at  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Loop bandwidth	For best LO noise Loop filter components: $C_2 = 3.9\text{ nF}$ , $C_1 = 15\text{ nF}$ , $R_4 = 220\Omega$	$B_{Loop}$		100		kHz
Phase noise PLL	Referring to the phase comparator $f_{PC} = 6.78\text{ MHz}$	$PN_{PLL}$		-111	-105	dBc/Hz
Phase noise VCO	At 1 MHz At 36 MHz	$PN_{VCO}$ $PN_{VCO}$		-90 -122		dBc/Hz
Frequency range of the VCO		$f_{VCO}$	310		440	MHz
Clock output (CMOS microcontroller compatible)		$Clk_{out}$		$f_{out} / 128$		MHz
Load capacitance at CLK		$C_{CLK}$			10	pF
Series resonance R of the crystal	$f_{XTO} = 13.56\text{ MHz}$ $f_{XTO} = 9.84\text{ MHz}$	$R_s$ $R_s$			80 100	$\Omega$
ASK modulation frequency rate	Duty cycle of the modulation signal = 50%	$f_{modASK}$	0		20	kHz
CLK output - Output current Low - Output current Low - Output current High - Output current High	$V_{CLK} = 0.2 \times V_S$ $V_{CLK} = 0.3 \times V_S$ $V_{CLK} = 0.8 \times V_S$ $V_{CLK} = 0.7 \times V_S$	$I_{ol}$ $I_{ol}$ $I_{oh}$ $I_{oh}$	150 200 -150 -200		100	$\mu A$ $\mu A$ $\mu A$ $\mu A$
ASK input - Low level input voltage - High level input voltage - Input current High		$V_{ASKl}$ $V_{ASKh}$ $I_{ASKh}$	1.7		0.3 140	V V $\mu A$
Enable ASK - Low level input voltage - High level input voltage - Input current High		$V_{EN}$ $V_{FSKl}$ $V_{FSKh}$ $I_{FSKh}$	1.7		0.3 140	V V $\mu A$

## 9. Ordering Information


Extended Type Number	Package	Remarks
ATA2745M-TCQY	SSO16	Taped and reeled, Pb-free

## 10. Package Information



Package acc. JEDEC MO 137 AB

02/05/99

 <b>Package Drawing Contact:</b> packagedrawings@atmel.com	<b>TITLE</b> Package: SSO16	<b>GPC</b>	<b>DRAWING NO.</b> 6.543-5060.01-4	<b>REV.</b> 2

## 11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4898B-RKE-08/06	<ul style="list-style-type: none"><li>• Put datasheet in a new template</li><li>• Section 9 “Ordering Information” on page 8 changed</li></ul>





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