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REVISION HISTORY

12/08—Rev. B to Rev. C

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12/97—Rev. A to Rev. B

Changes to Specifications Section 2

x/97—Rev. 0 to Rev. A

Changes to Specifications Section 2

7/97—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = full operating range, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE	−40		+85	°C	$T_A = T_{MIN}$ to T_{MAX}.
POWER SUPPLY					
Voltage	4.5	5.0	5.5	V	
Current		20	50	µA	V_{IL}, V_{IH} = CMOS levels.
		200	500	µA	V_{IL}, V_{IH} = TTL levels.
$\overline{\text{STROBE}}$ AND $\overline{\text{PB RESET}}$ INPUTS					
Input High Level	2.0		V_{CC} + 0.3	V	
Input Low Level	−0.3		+0.8	V	
INPUT LEAKAGE CURRENT					
($\overline{\text{STROBE}}$, TOLERANCE)	−1.0		+1.0	µA	
TD		1.6		µA	
OUTPUT CURRENT					
RESET	8	10		mA	V_{CC} is at 4.5 V to 5.5 V.
$\overline{\text{RESET}}$/RESET	−8	−12		mA	V_{CC} is at 4.5 V to 5.5 V.
OUTPUT VOLTAGE					
$\overline{\text{RESET}}$/RESET	V_{CC} − 0.5	V_{CC} − 0.1		V	When sourcing less than 500 µA, RESET remains within 0.5 V of V_{CC} on power-down until V_{CC} drops below 2.0 V. When sinking less than 500 µA, $\overline{\text{RESET}}$ remains within 0.5 V of GND on power-down until V_{CC} drops below 2.0 V.
$\overline{\text{RESET}}$/RESET High Level			0.4	V	
$\overline{\text{RESET}}$/RESET Low Level	2.4			V	
1 V OPERATION					
RESET Output Voltage		V_{CC} − 0.1		V	When sourcing less than 50 µA.
$\overline{\text{RESET}}$ Output Voltage		0.1		V	When sinking less than 50 µA.
V_{CC} TRIP POINT					
5%	4.5	4.62	4.74	V	TOLERANCE = GND.
10%	4.25	4.37	4.49	V	TOLERANCE = V_{CC}.
CAPACITANCE					
Input ($\overline{\text{STROBE}}$, TOLERANCE)			5	pF	T_A = 25°C.
Output (RESET, $\overline{\text{RESET}}$)			7	pF	T_A = 25°C.
$\overline{\text{PB RESET}}$					
Time	20			ms	$\overline{\text{PB RESET}}$ must be held low for a minimum of 20 ms to guarantee a reset.
Delay	1	4	20	ms	
RESET ACTIVE TIME	250	610	1000	ms	
$\overline{\text{STROBE}}$					
Pulse Width	70			ns	
Timeout Period	62.5	150	250	ms	TD = 0 V.
	250	600	1000	ms	TD = floating.
	500	1200	2000	ms	TD = V_{CC}.
V_{CC}					
Fall Time	10			µs	Guaranteed by design.
Rise Time	0			µs	Guaranteed by design.
V_{CC} FAIL DETECT TO RESET OUTPUT DELAY					RESET and $\overline{\text{RESET}}$ are logically correct.
			50	µs	After V_{CC} falls below the set tolerance voltage (see Figure 9).
	250	610	1000	ms	After V_{CC} rises above the set tolerance voltage.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	5.5 V
Logic Inputs	−0.3 V to V_{CC} + 0.3 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Power Dissipation	
N-8[1]	1000 mW
RW-16, RM-8[2]	900 mW
R-8[2]	900 µW

[1] Derate by 13.5 mW/°C above 25°C.
[2] Derate by 12 mW/°C above 25°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead PDIP (N-8)	100	°C/W
16-Lead SOIC_W (RW-16)	73	°C/W
8-Lead MSOP (RM-8)	206	°C/W
8-Lead SOIC_N (R-8)	153	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

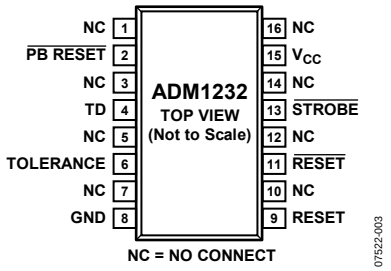


Figure 3. RW-16 Pin Configuration

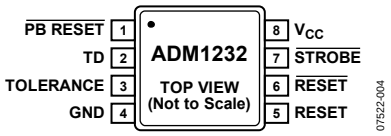


Figure 4. RM-8 Pin Configuration

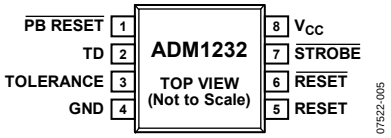


Figure 5. N-8 and R-8 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
RW-16	**N-8, R-8, RM-8**	**Mnemonic**	**Description**
1, 3, 5, 7, 10, 12, 14, 16		NC	No Connection.
2	1	$\overline{\text{PB RESET}}$	Push-Button Reset Input. This debounced input ignores pulses of less than 1 ms and is guaranteed to respond to pulses greater than 20 ms.
4	2	TD	Time Delay Set. This input allows the user to select the maximum amount of time that the ADM1232 allows the $\overline{\text{STROBE}}$ input to remain inactive—that is, $\overline{\text{STROBE}}$ is not receiving any high-to-low transitions—without forcing the ADM1232 to generate a RESET pulse. See the Specifications section, Figure 8, and the $\overline{\text{STROBE}}$ Timeout Selection section.
6	3	TOLERANCE	Tolerance Input. This input determines how much the supply voltage is allowed to decrease (as a percentage) before a RESET is asserted. Connect this pin to V_{CC} for 10% and to GND for 5%.
8	4	GND	0 V Ground Reference for All Signals.
9	5	RESET	Active High Logic Output. This pin is asserted when any of the following events occurs: V_{CC} decreases below the amount specified by the TOLERANCE input; when $\overline{\text{PB RESET}}$ is forced low; if there are no high-to-low transitions within the limits set by TD at $\overline{\text{STROBE}}$; and during power-up.
11	6	$\overline{\text{RESET}}$	Inverse of RESET. This pin has an open-drain output.
13	7	$\overline{\text{STROBE}}$	The $\overline{\text{STROBE}}$ input is used to monitor the activity of a microprocessor. If there are no high-to-low transitions within the time specified by TD, a reset is asserted.
15	8	V_{CC}	Power Supply Input, 5 V.

CIRCUIT INFORMATION

PB RESET

The $\overline{\text{PB RESET}}$ input makes it possible to manually reset a system using either a standard push-button switch or a logic low input. An internal debounce circuit provides glitch immunity when used with a switch, reducing the effects of glitches on the line. The debounce circuit is guaranteed to cause the ADM1232 to assert a reset if $\overline{\text{PB RESET}}$ is brought low for more than 20 ms and is guaranteed to ignore low inputs of less than 1 ms.

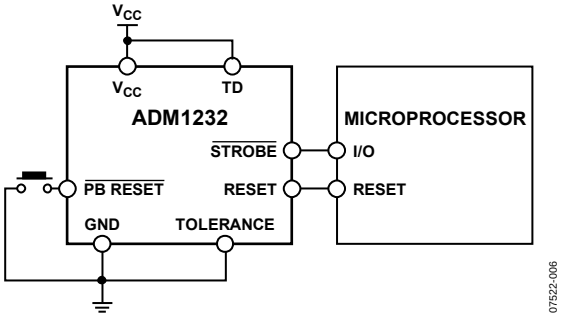


Figure 6. Typical Push-Button Reset Application

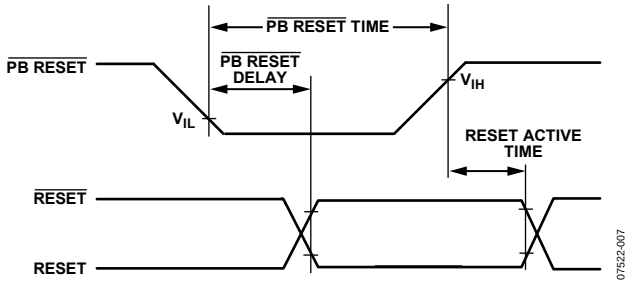


Figure 7. $\overline{\text{PB RESET}}$

STROBE TIMEOUT SELECTION

TD (time delay) set is used to set the strobe timeout period. The strobe timeout period is the maximum time between high-to-low transitions that $\overline{\text{STROBE}}$ accepts before a reset is asserted (see Figure 8). The strobe timeout settings are listed in Table 5.

Table 5. Strobe Timeout Settings

Condition	Min	Typ	Max	Unit
TD = 0 V	62.5	150	250	ms
TD = Floating	250	600	1000	ms
TD = V_{CC}	500	1200	2000	ms

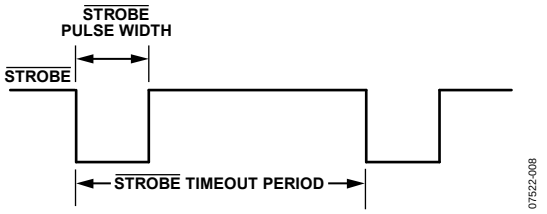


Figure 8. $\overline{\text{STROBE}}$ Parameters

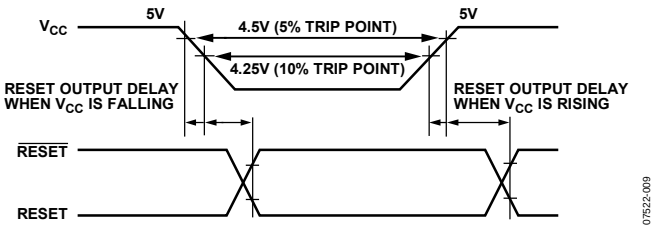


Figure 9. Reset Output Delay

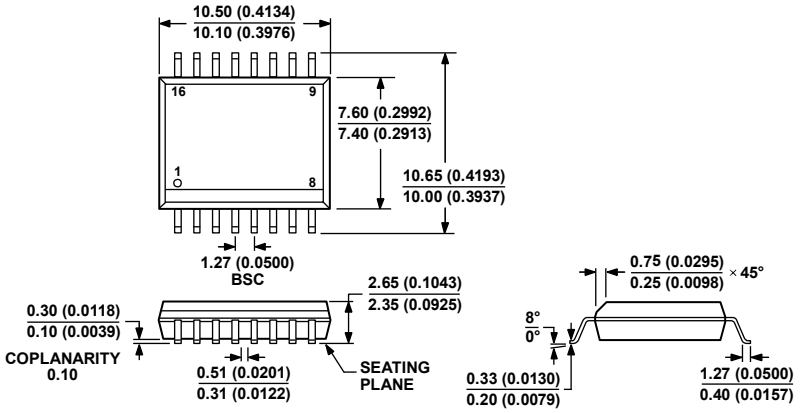
TOLERANCE

The TOLERANCE input is used to determine the level at which V_{CC} can vary below 5 V without the ADM1232 asserting a reset. Connecting TOLERANCE to GND selects a −5% tolerance level and causes the ADM1232 to generate a reset if V_{CC} falls below 4.75 V. If TOLERANCE is connected to V_{CC}, a −10% tolerance level is selected, which causes the ADM1232 to generate a reset if V_{CC} falls below 4.5 V. See the parameters for the V_{CC} trip point in the Specifications section for more information.

RESET AND $\overline{\text{RESET}}$ OUTPUTS

$\overline{\text{RESET}}$ is capable of sourcing and sinking current, whereas $\overline{\text{RESET}}$ is an open-drain MOSFET that sinks current only. Therefore, it is necessary to pull this output high.

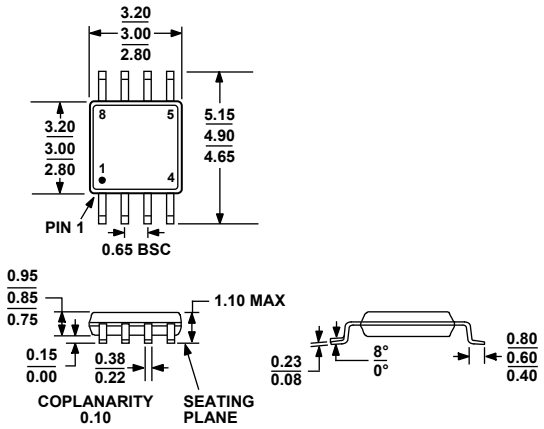
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

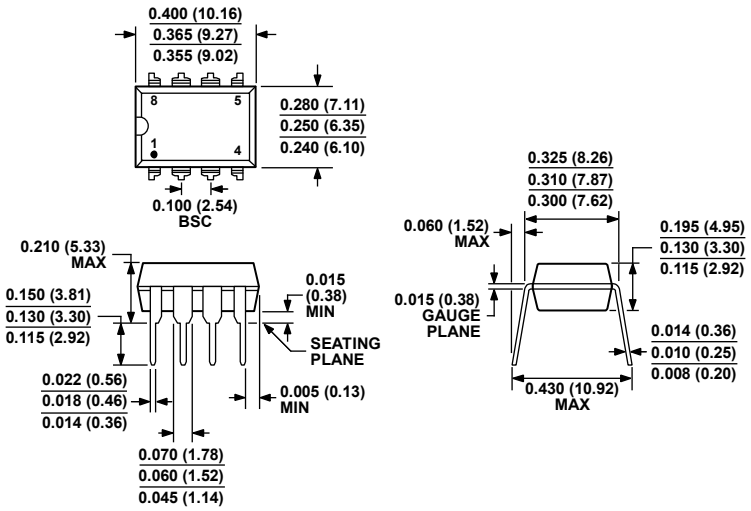
032707-B

Figure 10. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

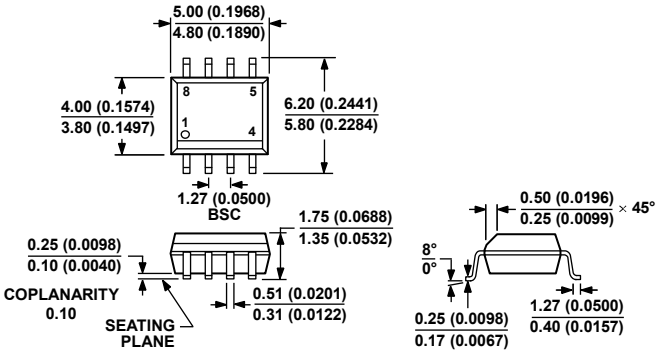
Figure 11. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 12. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 13. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options	Branding
ADM1232ARM	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	M2A
ADM1232ARM-REEL	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	M2A
ADM1232ARM-REEL7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	M2A
ADM1232ARMZ[1]	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	M4W
ADM1232ARMZ-REEL[1]	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	M4W
ADM1232ARMZ-REEL7[1]	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	M4W
ADM1232AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADM1232ANZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADM1232ARW	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W], Wide Body	RW-16	
ADM1232ARW-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W], Wide Body	RW-16	
ADM1232ARW-REEL7	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W], Wide Body	RW-16	
ADM1232ARWZ[1]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W], Wide Body	RW-16	
ADM1232ARWZ-REEL[1]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W], Wide Body	RW-16	
ADM1232ARWZ-REEL7[1]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W], Wide Body	RW-16	
ADM1232ARN	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM1232ARN-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM1232ARN-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM1232ARNZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM1232ARNZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM1232ARNZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

[1] Z = RoHS Compliant Part.

NOTES

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