ADG431/ADG432/ADG433–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{DD} to V_{SS}	V	
R_{ON}	17		Ω typ	V_D = ±8.5 V, I_S = –10 mA;
	24	26	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
R_{ON} vs. V_D (V_S)	15		% typ	
R_{ON} Drift	0.5		%/°C typ	
R_{ON} Match	5		% typ	V_D = 0 V, I_S = –10 mA
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.05		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		nA typ	V_D = V_S = ±15.5 V;
	±0.35	±3	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.02	µA max	
C_{IN} Digital Input Capacitance	9		pF typ	
DYNAMIC CHARACTERISTICS[1]				V_{DD} = +15 V, V_{SS} = –15 V
t_{ON}	90		ns typ	R_L = 300 Ω, C_L = 35 pF;
		165	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	60		ns typ	R_L = 300 Ω, C_L = 35 pF;
		130	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG433 Only)	25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		pF typ	f = 1 MHz
C_D (OFF)	9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = –16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		µA typ	
	0.1	0.2	µA max	
I_{SS}	0.0001		µA typ	
	0.1	0.2	µA max	
I_L	0.0001		µA typ	
	0.1	0.2	µA max	
Power Dissipation		7.7	µW max	

NOTES

[1]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply (V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
R_{ON}	28		Ω typ	0 < V_D < 8.5 V, I_S = –10 mA;
	42	45	Ω max	V_{DD} = 10.8 V
R_{ON} vs. V_D (V_S)	20		% typ	
R_{ON} Drift	0.5		%/°C typ	
R_{ON} Match	5		% typ	V_D = 0 V, I_S = –10 mA
LEAKAGE CURRENTS				V_{DD} = 13.2 V
Source OFF Leakage I_S (OFF)	±0.04		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.04		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, Is (ON)	±0.01		nA typ	V_D = V_S = 12.2 V/1 V;
	±0.3	±3	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.01	µA max	
C_{IN} Digital Input Capacitance	9		pF typ	
DYNAMIC CHARACTERISTICS[1]				V_{DD} = 12 V, V_{SS} = 0 V
t_{ON}	165		ns typ	R_L = 300 Ω, C_L = 35 pF;
		240	ns max	V_S = 8 V; Test Circuit 4
t_{OFF}	60		ns typ	R_L = 300 Ω, C_L = 35 pF;
		115	ns max	V_S = 8 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG433 Only)	25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = 10 V; Test Circuit 5
Charge Injection	25		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		pF typ	f = 1 MHz
C_D (OFF)	9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 13.2 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		µA typ	
	0.03	0.1	µA max	
I_L	0.0001		µA typ	
	0.03	0.1	µA max	V_L = 5.25 V
Power Dissipation		1.9	µW max	

NOTES
[1]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Truth Table (ADG431/ADG432)

ADG431 In	ADG432 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG433)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted.)

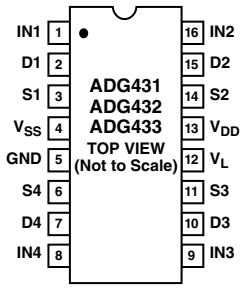
V_{DD} to V_{SS} . . . . . 44 V
V_{DD} to GND . . . . . –0.3 V to +25 V
V_{SS} to GND . . . . . +0.3 V to –25 V
V_L to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2] . . . . . V_{SS} – 2 V to V_{DD} + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . . 30 mA
Peak Current, S or D . . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
Plastic Package, Power Dissipation . . . . . 470 mW
θ_{JA}, Thermal Impedance . . . . . 117°C/W
Lead Temperature, Soldering (10 sec) . . . . . 260°C
SOIC Package, Power Dissipation . . . . . 600 mW
θ_{JA}, Thermal Impedance . . . . . 77°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG431/ADG432/ADG433 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION (DIP/SOIC)



ORDERING GUIDE

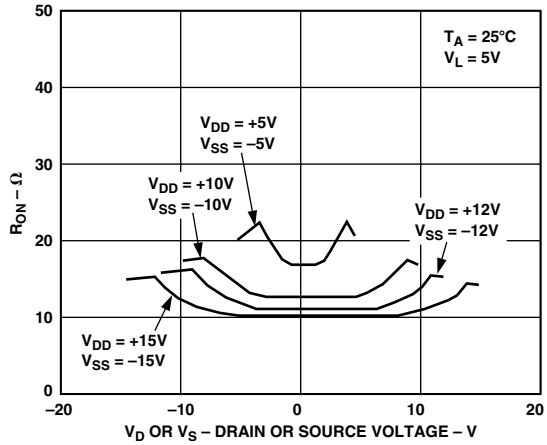
Model	Temperature Range	Package Option[1]
ADG431BN	–40°C to +85°C	N-16
ADG431BR	–40°C to +85°C	R-16A
ADG431ABR	–40°C to +85°C	R-16A[2]
ADG432BN	–40°C to +85°C	N-16
ADG432BR	–40°C to +85°C	R-16A
ADG432ABR	–40°C to +85°C	R-16A[2]
ADG433BN	–40°C to +85°C	N-16
ADG433BR	–40°C to +85°C	R-16A
ADG433ABR	–40°C to +85°C	R-16A[2]

NOTES
[1]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC).
[2]Trench isolated, latch-up proof parts. See Trench Isolation section.

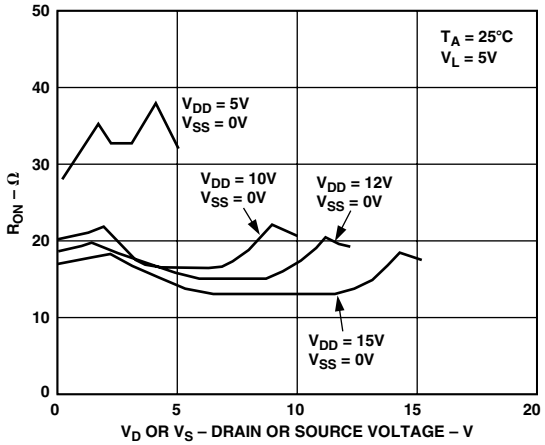
TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
R_{ON} vs. V_D (V_S)	The variation in R_{ON} due to a change in the analog input voltage with a constant load current.
R_{ON} Drift	Change in R_{ON} vs. temperature.
R_{ON} Match	Difference between the R_{ON} of any two switches.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.

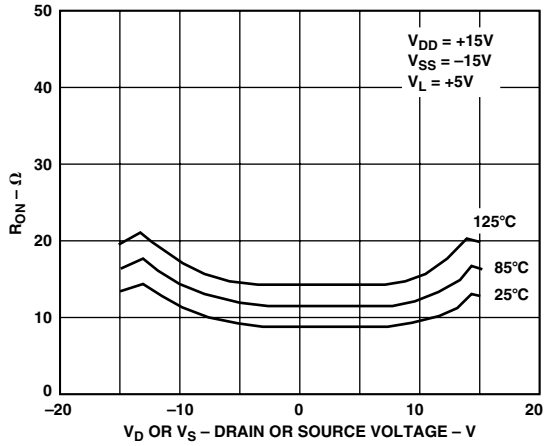
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Input Capacitance to ground of a digital input.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.



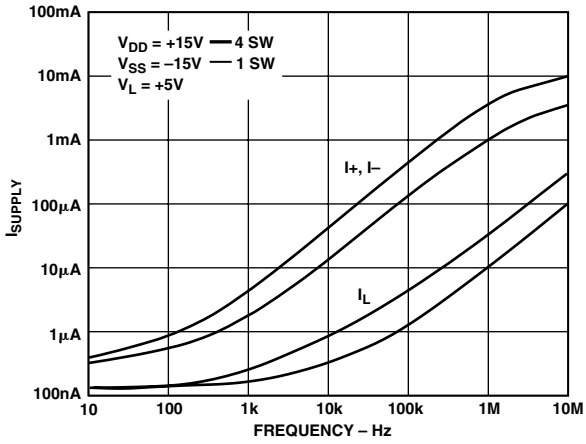
TPC 1. On Resistance as a Function of V_D (V_S) Dual Supplies



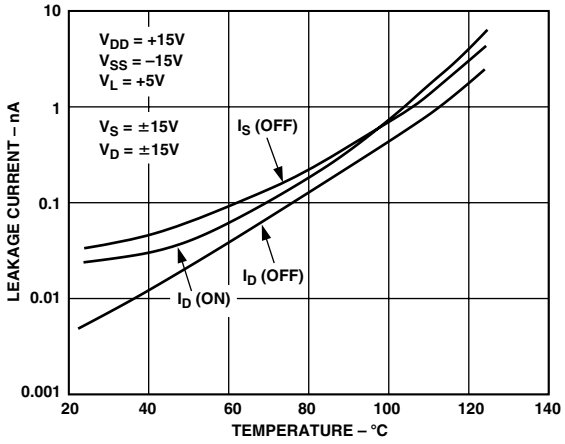
TPC 4. On Resistance as a Function of V_D (V_S) Single Supply



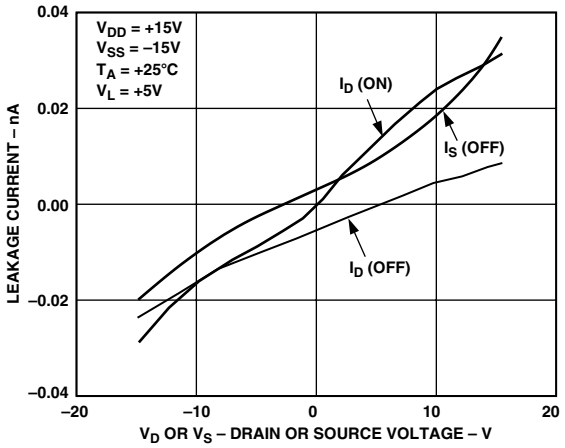
TPC 2. On Resistance as a Function of V_D (V_S) for Different Temperatures



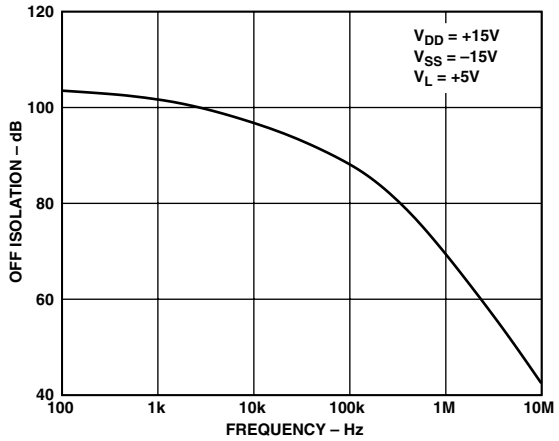
TPC 5. Supply Current vs. Input Switching Frequency



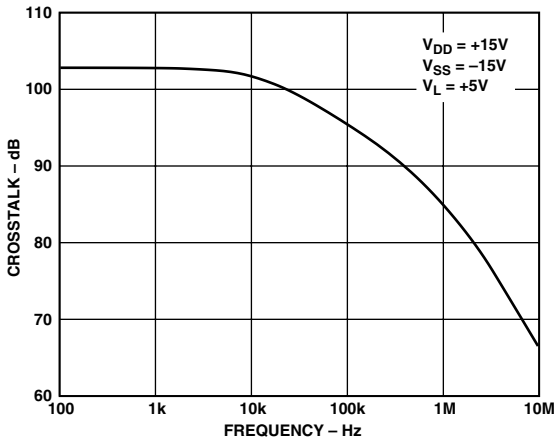
TPC 3. Leakage Currents as a Function of Temperature



TPC 6. Leakage Currents as a Function of V_D (V_S)



TPC 7. Off Isolation vs. Frequency



TPC 8. Crosstalk vs. Frequency

TRENCH ISOLATION

In the ADG431A, ADG432A and ADG433A, an insulating oxide layer (trench) is placed between the NMOS and PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors from a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.

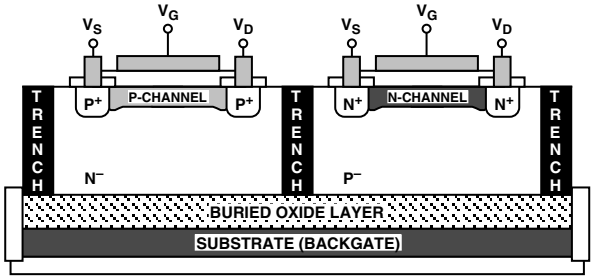


Figure 1. Trench Isolation

APPLICATION

Figure 2 illustrates a precise, fast sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG431/ADG432/ADG433 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 μV/μs.

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±10 V input range. Both the acquisition and settling times are 850 ns.

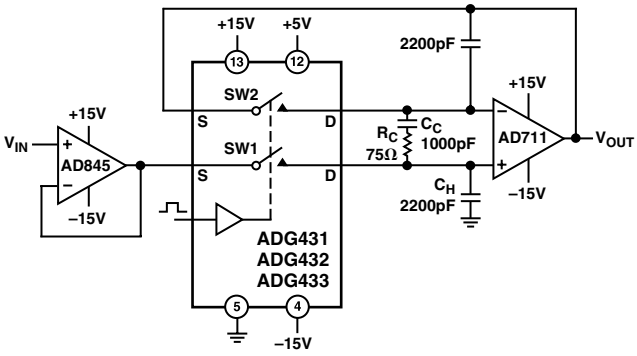
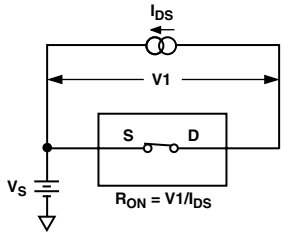
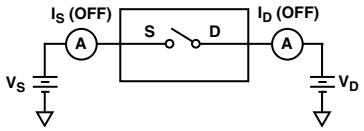


Figure 2. Fast, Accurate Sample-and-Hold

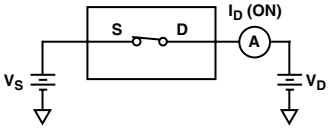
Test Circuits



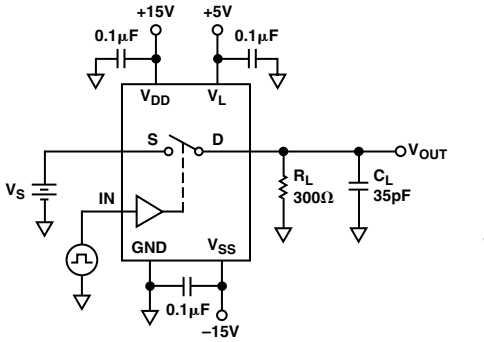
Test Circuit 1. On Resistance

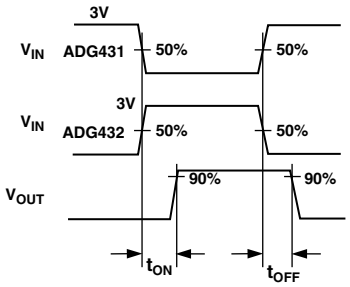


Test Circuit 2. Off Leakage

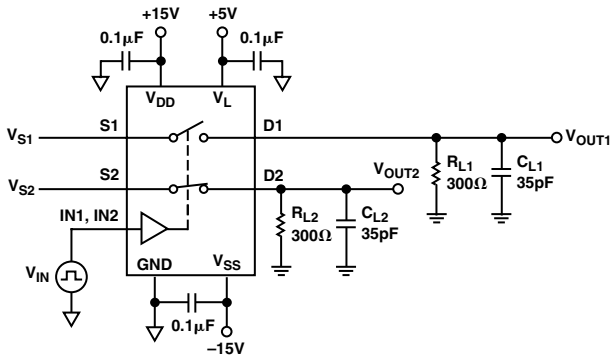


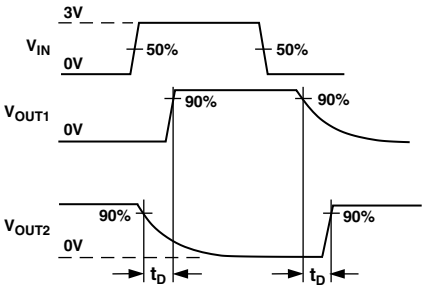
Test Circuit 3. On Leakage



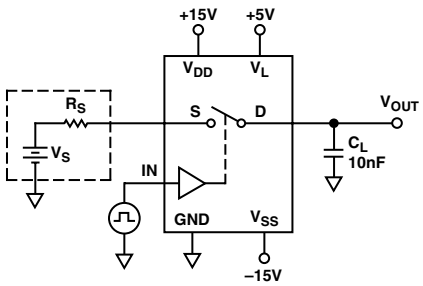


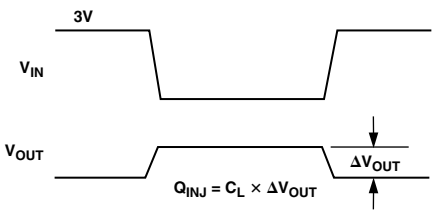
Test Circuit 4. Switching Times



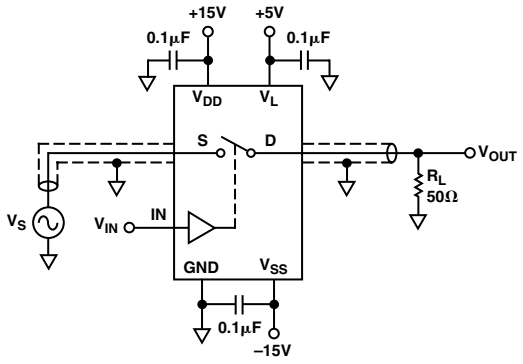


Test Circuit 5. Break-Before-Make Time Delay

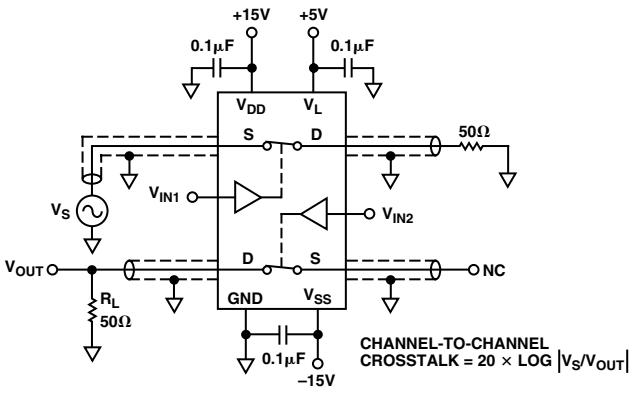




Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

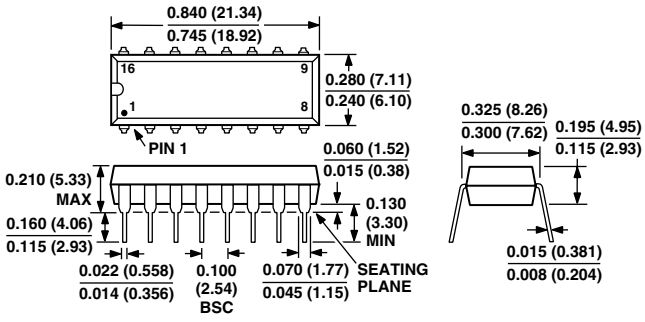
C00050b–0–3/01(C)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

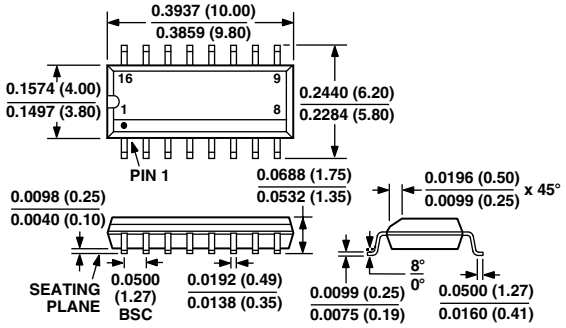
16-Lead Plastic DIP (Narrow)

(N-16)



16-Lead SOIC

(R-16A)



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ADG431/ADG432/ADG433–Revision History

Location **Page**

Data Sheet changed from REV. B to REV. C.