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4/05—Rev. 0 to Rev. A

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7/04—Revision 0: Initial Version

DC SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, A_{IN} = −1 dBFS, full scale = 1.0 V, internal reference, differential analog and clock inputs, unless otherwise noted.

Table 1.

			AD9480-250			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				8		Bits
ACCURACY						
No Missing Codes	Full	VI		Guaranteed		
Offset Error	25°C	I	−40		+40	mV
Gain Error[1]	25°C	I	−6.0		+6.0	% FS
Differential Nonlinearity (DNL)						
AD9480BSUZ-250	Full	VI	−0.5	±0.28	+0.5	LSB
AD9480ASUZ-250	Full	VI	−0.85	±0.35	+0.85	LSB
Integral Nonlinearity (INL)	Full	VI	−0.9	±0.26	+0.9	LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		30		µV/°C
Gain Error	Full	V		0.03		%FS/°C
Reference	Full	V		±0.025		mV/°C
REFERENCE						
Internal Reference Voltage	Full	VI	0.97	1.0	1.03	V
Output Current[2]	25°C	IV			1.5	mA
I_{VREF} Input Current[3]	25°C	I			100	µA
I_{SENSE} Input Current[2]	25°C	I			10	µA
ANALOG INPUTS (VIN+, VIN−)						
Differential Input Voltage Range (FS = 1)[4]	Full	V		1		V p-p
Common-Mode Voltage	Full	VI	1.7	1.9	2.1	V
Input Resistance	25°C	I	8.6	10	10.7	kΩ
	Full	VI	8.4	10	11.2	kΩ
Input Capacitance	25°C	V		4		pF
Analog Bandwidth, Full Power	25°C	V		750		MHz
POWER SUPPLY						
AVDD	Full	IV	3.0	3.3	3.6	V
DRVDD	Full	IV	3.0	3.3	3.6	V
Power Dissipation[5]	25°C	V		590		mW
Power-Down Dissipation	25°C	V		15		mW
I_{AVDD}[5]	Full	VI		145	156	mA
I_{DRVDD}[5]	Full	VI		34	38	mA
Power Supply Rejection Ratio (PSRR)	25°C	V		−4.2		mV/V

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1 V external reference and a 1 V p-p differential analog input).
[2] Internal reference mode; SENSE = AGND.
[3] External reference mode; VREF driven by external 1.0 V reference; SENSE = AVDD.
[4] In FS = 1 V, both analog inputs are 500 mV p-p and out of phase with each other.
[5] Power dissipation and current measured with rated encode and a dc analog input (outputs static). See Figure 13 for active operation.

DIGITAL SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, A_{IN} = −1 dBFS, full scale = 1.0 V, internal reference, differential analog and clock inputs, unless otherwise noted.

Table 2.

			AD9480-250			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS (CLK+, CLK–)						
Differential Input	Full	IV	200			mV p-p
Common-Mode Voltage[1]	Full	VI	1.4	1.5	1.68	V
Input Resistance	Full	VI	4.2	5.5	6.0	kΩ
Input Capacitance	25°C	V		4		pF
LOGIC INPUTS (PDWN, S1)[2]						
PDWN Logic 1 Voltage	Full	IV	2.0			V
PDWN Logic 0 Voltage	Full	IV			0.8	V
PDWN Logic 1 Input Current	Full	VI			±160	µA
PDWN Logic 0 input Current	Full	VI			10	µA
PDWN, S1 Input Resistance	25°C	V		30		kΩ
PDWN, S1 Input Capacitance	25°C	V		4		pF
DIGITAL OUTPUTS						
Differential Output Voltage (V_{OD})[3]	Full	VI	247		454	mV
Output Offset Voltage (V_{OS})	Full	VI	1.125		1.375	V
Output Coding	Full	IV	Twos complement or binary			

[1] The common mode for CLOCK inputs can be externally set, such that 0.9 V < CLK ± < 2.6 V.
[2] S1 is a multilevel logic input, see Table 8.
[3] LVDSBIAS resistor = 3.74 kΩ.

AC SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, A_{IN} = −1 dBFS, full scale = 1.0 V, internal reference, differential analog and clock inputs, unless otherwise noted.

Table 3.

			AD9480-250			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)						
f_{IN} = 19.7 MHz	25°C	V		47		dB
f_{IN} = 70.1 MHz	25°C	I	45	47		dB
f_{IN} = 170 MHz	25°C	I	45	46		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)						
f_{IN} = 19.7 MHz	25°C	V		46.5		dB
f_{IN} = 70.1 MHz	25°C	I	44.8	46.5		dB
f_{IN} = 170 MHz	25°C	I	44.8	46.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)						
f_{IN} = 19.7 MHz	25°C	V		7.6		Bits
f_{IN} = 70.1 MHz	25°C	I	7.3	7.6		Bits
f_{IN} = 170 MHz	25°C	I	7.3	7.6		Bits
WORST SECOND OR THIRD HARMONIC DISTORTION						
f_{IN} = 19.7 MHz	25°C	V		−65		dBc
f_{IN} = 70.1 MHz	25°C	I		−65	−60	dBc
f_{IN} = 170 MHz	25°C	I		−65	−60	dBc
WORST OTHER						
f_{IN} = 19.7 MHz	25°C	V		−70		dBc
f_{IN} = 70.1 MHz	25°C	I		−70	−63	dBc
f_{IN} = 170 MHz	25°C	I		−70	−63	dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[1]						
f_{IN} = 19.7 MHz	25°C	V		−65		dBc
f_{IN} = 70.1 MHz	25°C	I		−65	−60	dBc
f_{IN} = 170 MHz	25°C	I		−65	−60	dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)						
f_{IN1} = 69.3 MHz, f_{IN2} = 70.3 MHz	25°C	V		−68		dBc

[1] Nyquist bin energy ignored.

SWITCHING SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, differential clock input, DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	AD9480-250			Unit
			Min	Typ	Max	
CLOCK						
Maximum Conversion Rate	Full	VI	250			MSPS
Minimum Conversion Rate	Full	VI			20	MSPS
Clock Pulse Width High (t_{EH})	Full	IV	1.2	2		ns
Clock Pulse Width Low (t_{EL})	Full	IV	1.2	2		ns
OUTPUT PARAMETERS						
Valid Time (t_V)[1]	Full	VI	1.9			ns
Propagation Delay (t_{PD})	Full	VI		2.8	3.8	ns
Rise Time (t_R) 20% to 80%	Full	V		0.5		ns
Fall Time (t_F) 20% to 80%	Full	V		0.5		ns
DCO Propagation Delay (t_{CPD})	Full	VI	1.9	2.7	3.7	ns
Data-to-DCO Skew ($t_{PD} - t_{CPD}$)	Full	IV	0	0.1	0.6	ns
Pipeline Latency	25°C	VI		8		Cycles
APERTURE						
Aperture Delay (t_A)	25°C	V		1.5		ns
Aperture Uncertainty (Jitter)	25°C	V		0.25		ps rms

[1] Valid time is approximately equal to minimum t_{PD}. C_{LOAD} equals 5 pF maximum.

TIMING DIAGRAM

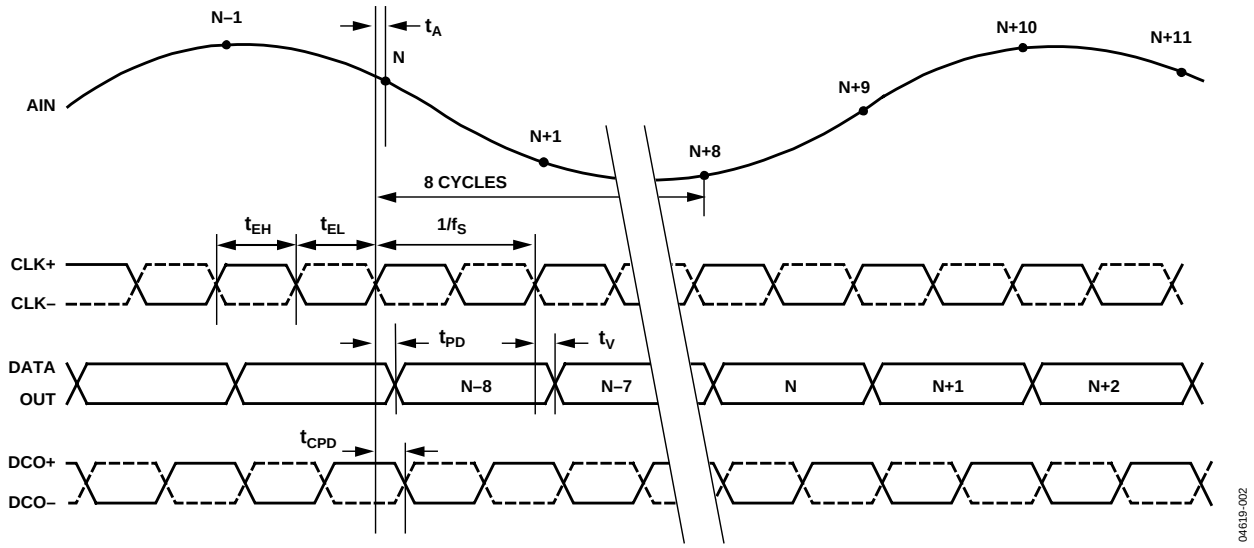


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Thermal impedance (θ_{JA}) = 46.4°C/W (4-layer PCB).

Table 5.

Parameter	Min Rating	Max Rating
ELECTRICAL		
AVDD (With Respect to AGND)	−0.5 V	+4.0 V
DRVDD (With Respect to DRGND)	−0.5 V	+4.0 V
AGND (With Respect to DRGND)	−0.5 V	+0.5 V
Digital I/O (With Respect to DRGND)	−0.5 V	DRVDD + 0.5 V
Analog Inputs (With Respect to AGND)	−0.5 V	AVDD + 0.5 V
ENVIRONMENTAL		
Operating Temperature	−40°C	85°C
Junction Temperature		150°C
Case Temperature		150°C
Storage Temperature		150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Table 6.

Level	Descriptions
I	100% production tested.
II	100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

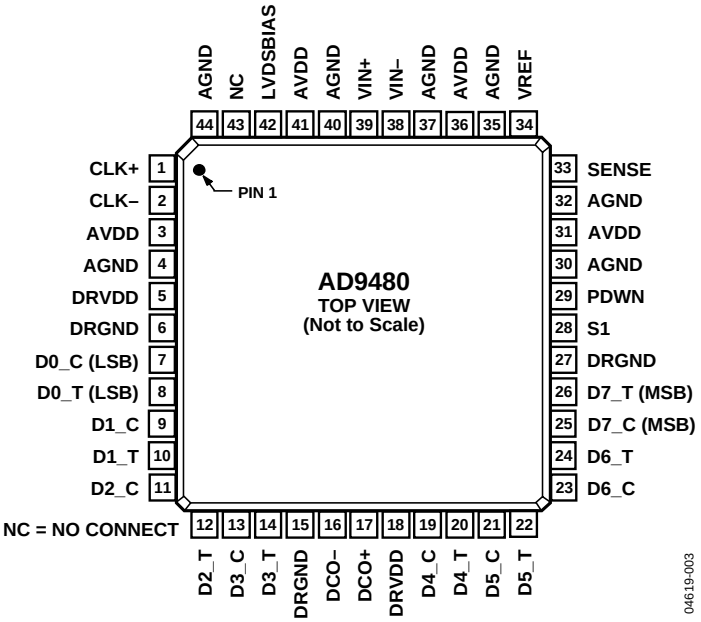


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description	Pin No.	Mnemonic	Description
1	CLK+	Input Clock—True	23	D6_C	Data Output Bit 6—Complement
2	CLK–	Input Clock—Complement	24	D6_T	Data Output Bit 6—True
3	AVDD	3.3 V Analog Supply	25	D7_C	Data Output Bit 7—Complement (MSB)
4	AGND	Analog Ground	26	D7_T	Data Output Bit 7—True (MSB)
5	DRVDD	3.3 V Digital Output Supply	27	DRGND	Digital Ground
6	DRGND	Digital Ground	28	S1	Data Format Select and Duty-Cycle Stabilizer Selection (See Table 8)
7	D0_C	Data Output Bit 0—Complement (LSB)	29	PDWN	Power-Down Selection (AVDD = Power Down)
8	D0_T	Data Output Bit 0—True (LSB)	30	AGND	Analog Ground
9	D1_C	Data Output Bit 1—Complement	31	AVDD	3.3 V Analog Supply
10	D1_T	Data Output Bit 1—True	32	AGND	Analog Ground
11	D2_C	Data Output Bit 2—Complement	33	SENSE	Reference Mode Selection (See Table 9)
12	D2_T	Data Output Bit 2—True	34	VREF	Voltage Reference Input/Output
13	D3_C	Data Output Bit 3—Complement	35	AGND	Analog Ground
14	D3_T	Data Output Bit 3—True	36	AVDD	3.3 V Analog Supply
15	DRGND	Digital Ground	37	AGND	Analog Ground
16	DCO–	Data Clock Output—Complement	38	VIN–	Analog Input—Complement
17	DCO+	Data Clock Output—True	39	VIN+	Analog Input—True
18	DRVDD	3.3 V Digital Output Supply	40	AGND	Analog Ground
19	D4_C	Data Output Bit 4—Complement	41	AVDD	3.3 V Analog Supply
20	D4_T	Data Output Bit 4—True	42	LVDSBIAS	LVDS Output Current Adjust
21	D5_C	Data Output Bit 5—Complement	43	NC[1]	No Connect (Leave Floating)
22	D5_T	Data Output Bit 5—True	44	AGND	Analog Ground

[1] Pin 43 will self-bias to 1.5 V. It can be left floating (as recommended) or tied to AVDD or ground with no ill effects.

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the encode command and the instant the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in a Logic 1 state to achieve rated performance; pulse width low is the minimum time that the clock pulse should be left in a low state. See the timing implications of changing t_{EH} in the Clocking the AD9480 section. At a given clock rate, these specifications define an acceptable clock duty cycle.

Crosstalk
Coupling onto one channel being driven by a low level (−40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically, and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180° and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits
The effective number of bits (ENOB) is calculated by the measured SINAD based on (assuming full-scale input)

$$ENOB = \frac{SINAD_{MEASURED} - 1.76\ \text{dB}}{6.02}$$

Full-Scale Input Power
Expressed in dBm. Computed by

$$Power_{FULLSCALE} = 10 \log \left(\frac{\frac{V^2{}_{FULLSCALE}\ rms}{Z_{INPUT}}}{0.001} \right)$$

Gain Error
The difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of CLK+ and CLK− and the time when all output data bits are within valid logic levels.

Noise (For Any Range Within the ADC)
This value includes both thermal and quantization noise.

$$V_{noise} = \sqrt{Z \times .001 \times 10 \left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10} \right)}$$

where:
Z is the input impedance.
FS is the full scale of the device for the frequency in question.
SNR is the value for the particular input level.
Signal is the signal level within the ADC reported in dB below full scale.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (that is, degrades as signal level is lowered) or dBFS (that is, always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It also may be reported in dBc (that is, degrades as signal level is lowered) or in dBFS (that is, always relates back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic), reported in dBc.

Transient Response Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, DRVDD = 3.3 V, T = 25°C, A_{IN} differential drive, FS = 1, unless otherwise noted.

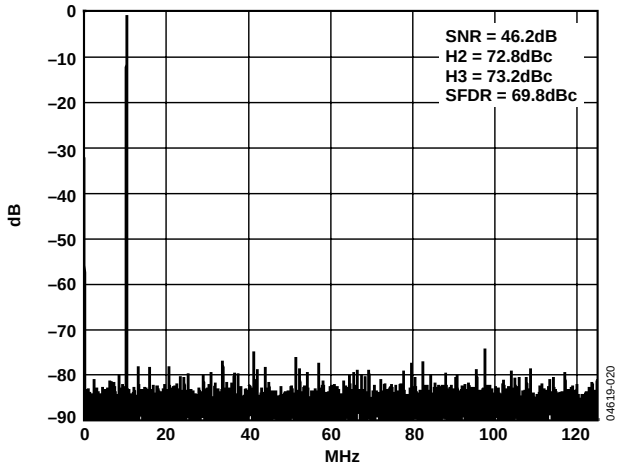


Figure 4. FFT: f_S = 250 MSPS, A_{IN} = 10.3 MHz @ −1 dBFS

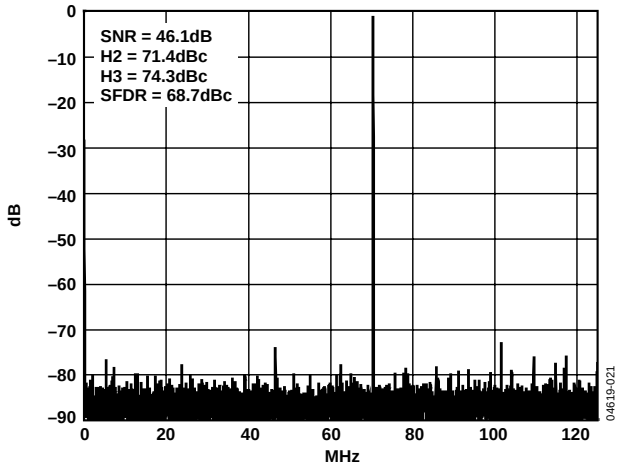


Figure 5. FFT: f_S = 250 MSPS, A_{IN} = 70 MHz @ −1 dBFS

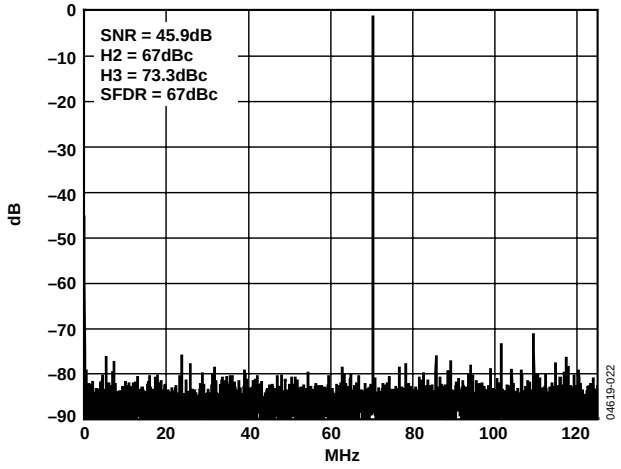


Figure 6. FFT: f_S = 250 MSPS, A_{IN} = 70 MHz @ −1 dBFS, Single-Ended Input

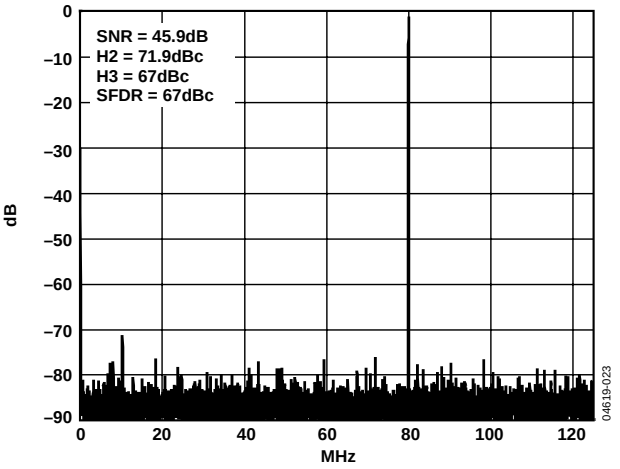


Figure 7. FFT: f_S = 250 MSPS, A_{IN} = 170 MHz @ −1 dBFS

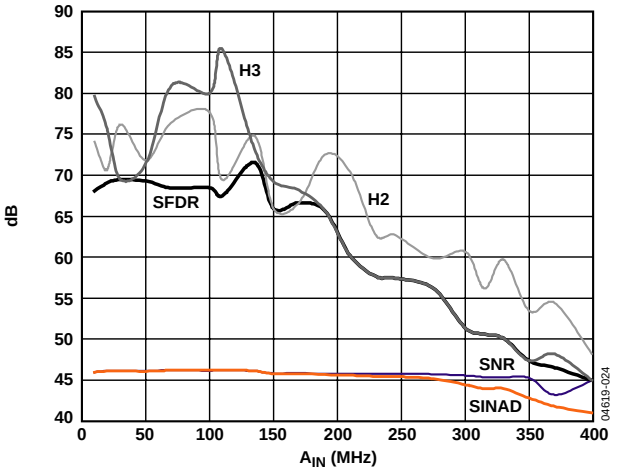


Figure 8. Analog Input Frequency Sweep, A_{IN} = −1 dBFS, FS = 1 V, f_S = 250 MSPS

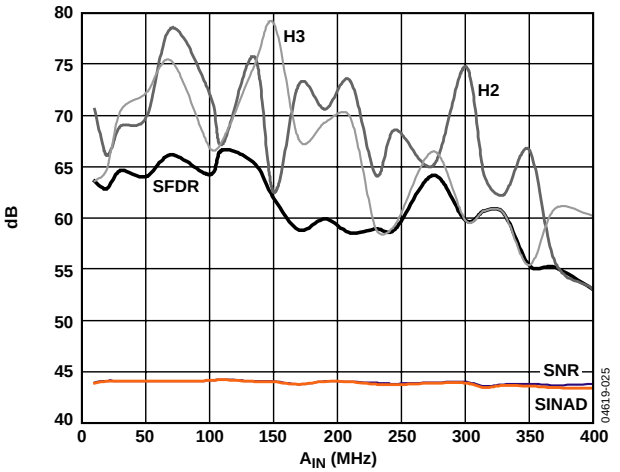


Figure 9. Analog Input Frequency Sweep, A_{IN} = −1 dBFS, FS = 0.75 V, f_S = 250 MSPS

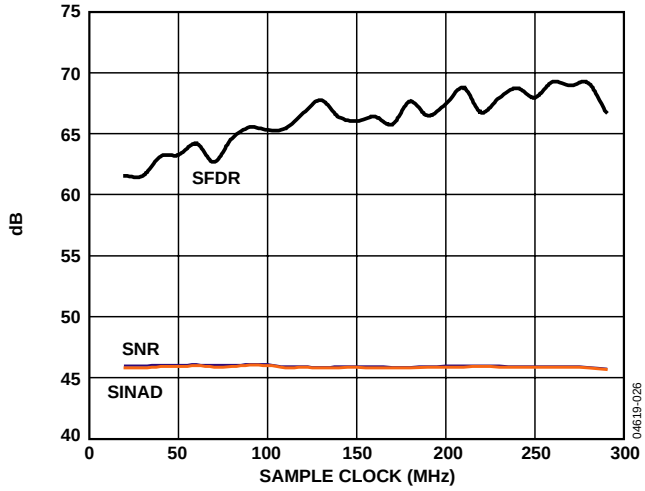


Figure 10. SNR, SINAD, SFDR vs. Sample Clock Frequency, A_{IN} = 70 MHz @ –1 dBFS

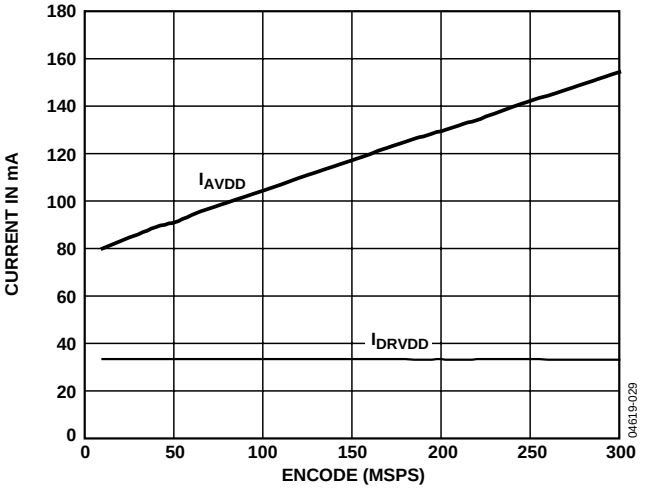


Figure 13. I_{AVDD} and I_{DRVDD} vs. Clock Rate, C_{LOAD} = 5 pF A_{IN} = 70 MHz @ –1 dBFS

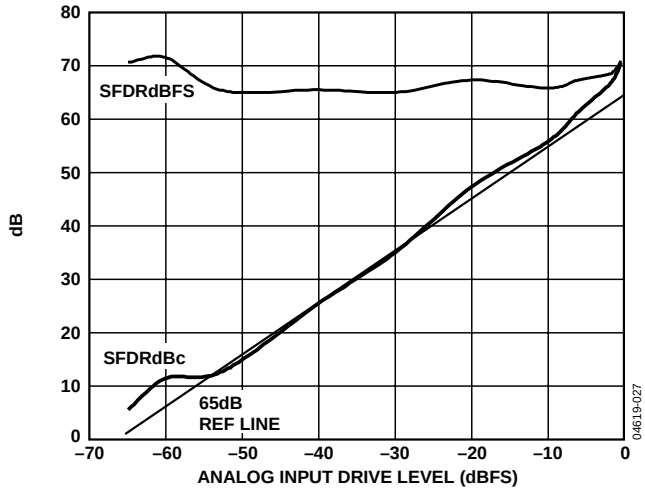


Figure 11. SFDR vs. A_{IN} Input Level; A_{IN} = 70 MHz @ 250 MSPS

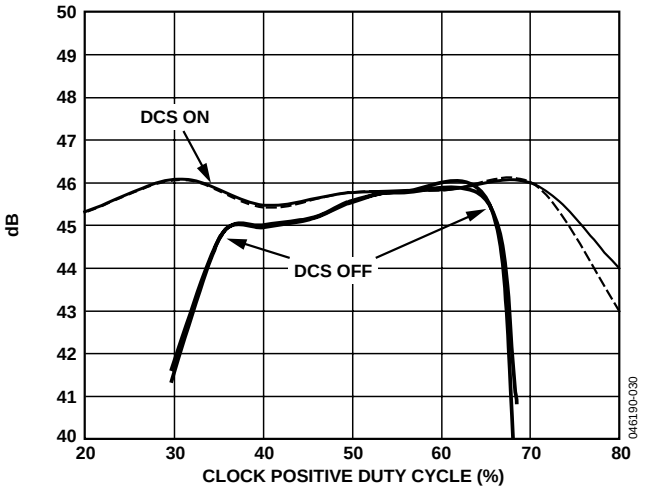


Figure 14. SNR, SINAD vs. Clock Pulse Width High, A_{IN} = 70 MHz @ –1 dBFS, 250 MSPS, DCS On/Off

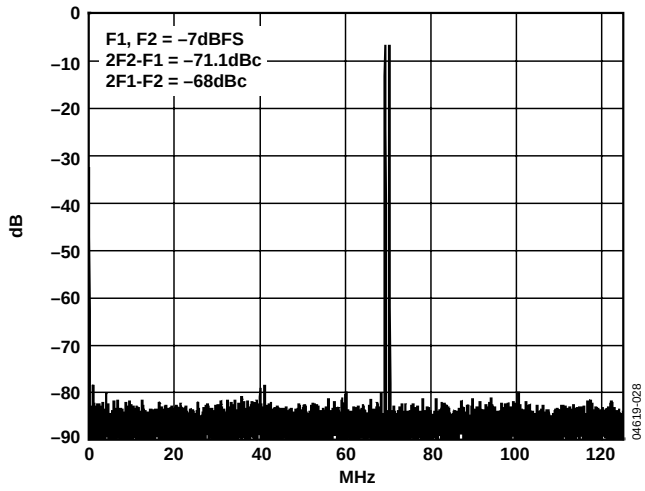


Figure 12. Two-Tone Intermodulation Distortion (69.3 MHz and 70.3 MHz; f_S = 250 MSPS)

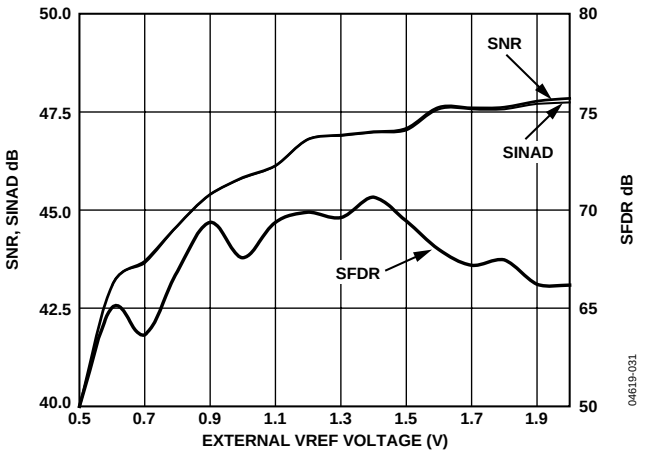


Figure 15. SNR, SINAD, and SFDR vs. VREF in External Reference Mode, A_{IN} = 70 MHz @ –1 dBFS, 250 MSPS

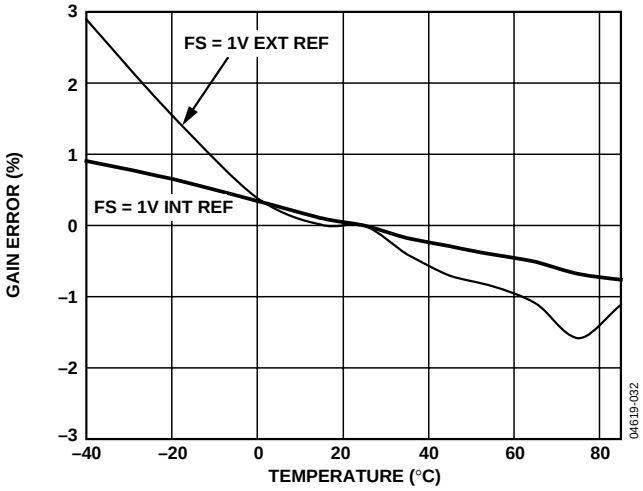


Figure 16. Full-Scale Gain Error vs. Temperature, A_{IN} = 70.3 MHz @ –0.5 dBFS, 250 MSPS, FS = 1

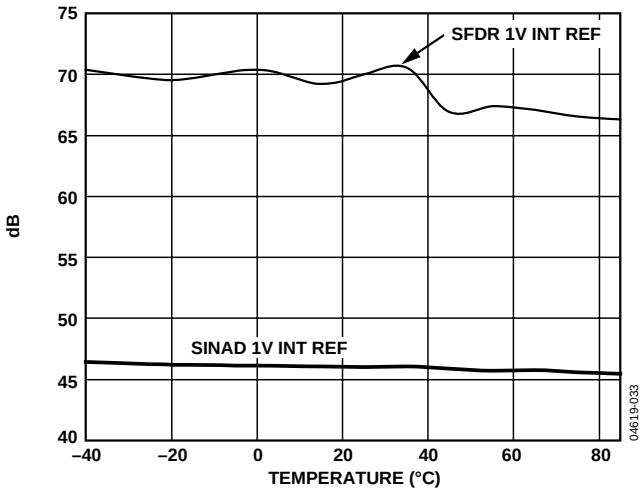


Figure 17. SINAD, SFDR vs. Temperature, A_{IN} = 70 MHz @ –1 dBFS, 250 MSPS

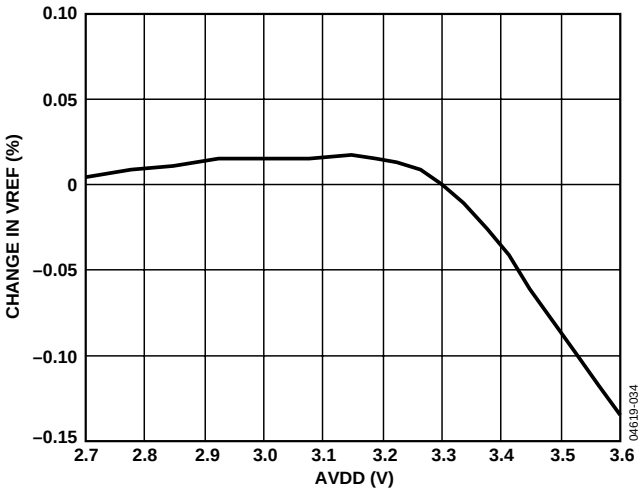


Figure 18. VREF Sensitivity to AVDD

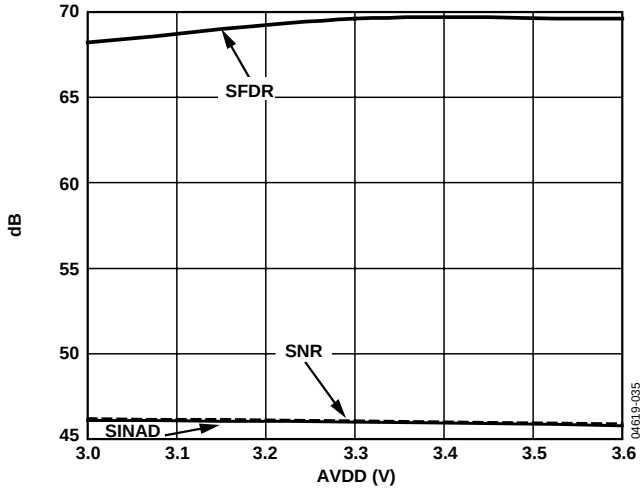


Figure 19. SNR, SINAD, and SFDR vs. Supply Voltage, A_{IN} = 70.3 MHz @ –1 dBFS, 250 MSPS

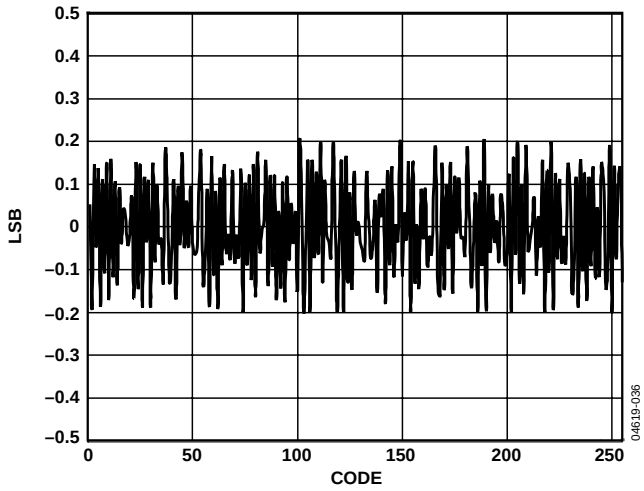


Figure 20. Typical DNL Plot, A_{IN} = 10.3 MHz @ –0.5 dBFS, 250 MSPS

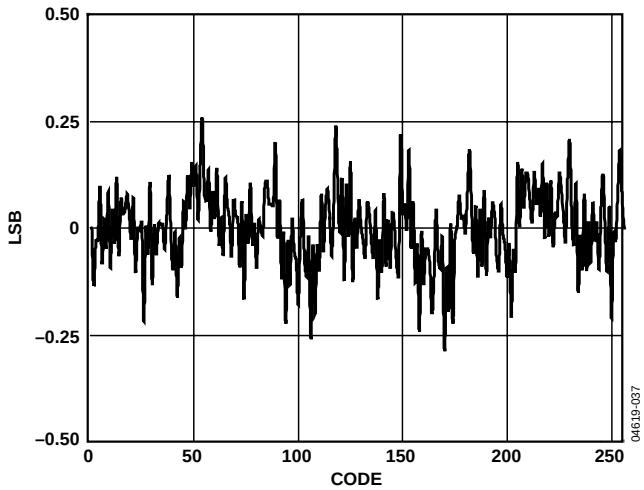


Figure 21. Typical INL Plot, A_{IN} = 10.3 MHz @ –0.5 dBFS, 250 MSPS

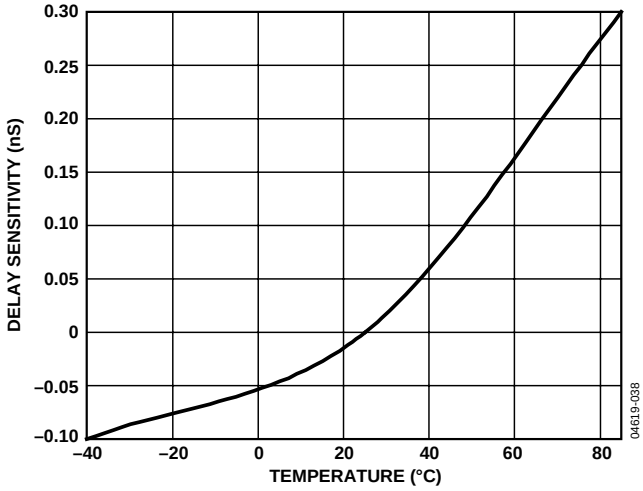


Figure 22. Propagation Delay Adder vs. Temperature

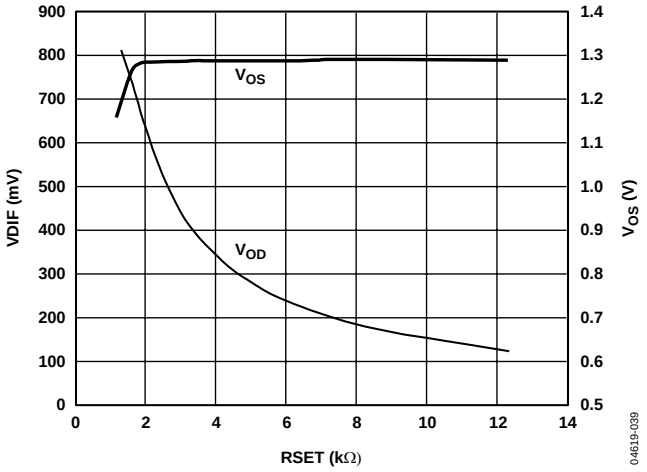


Figure 23. LVDS Output Swing, Common-Mode Voltage vs. RSET, Placed at LVDSBIAS

EQUIVALENT CIRCUITS

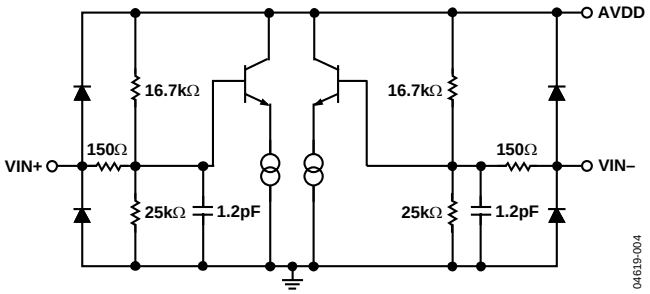


Figure 24. Analog Inputs

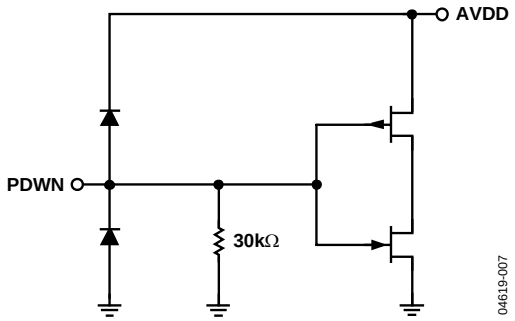


Figure 27. Power-Down Input

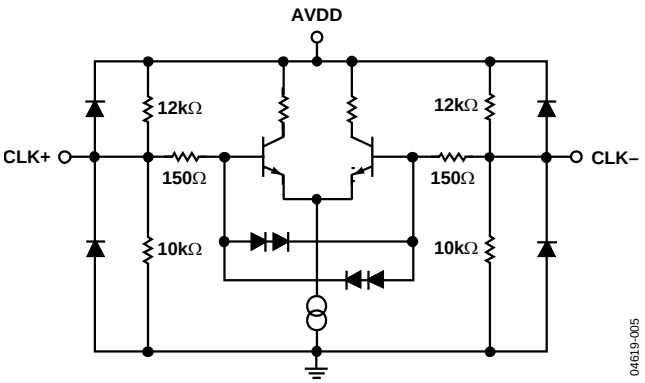


Figure 25. Clock Inputs

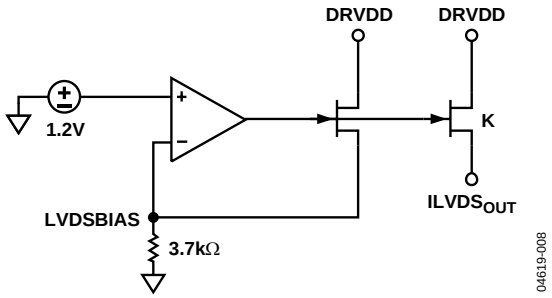


Figure 28. LVDSBIAS Input

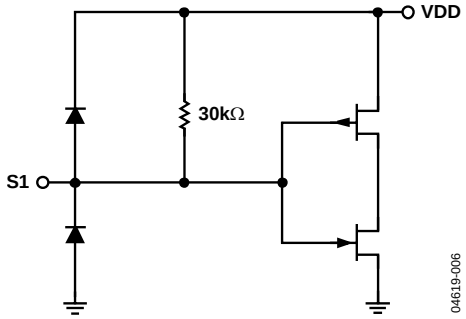


Figure 26. S1 Input

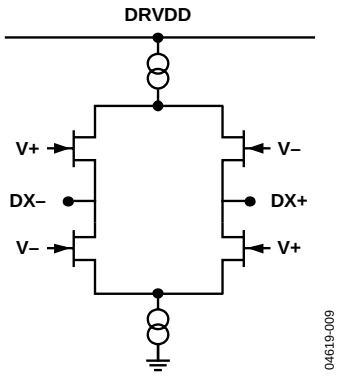


Figure 29. LVDS Data, DCO Outputs

APPLICATION NOTES

The AD9480 uses a 1.5-bit per stage architecture. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the 8-bit core. For ease of use, the part includes an on-board reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output logic levels are LVDS (ANSI 644 compatible).

CLOCKING THE AD9480

Any high speed ADC is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the A/D output. Considerable care has been taken in the design of the CLOCK input of the AD9480, and the user is advised to give commensurate thought to the clock source.

The AD9480 has an internal clock duty-cycle stabilization circuit that locks to the rising edge of CLOCK and optimizes timing internally for sample rates between 100 MSPS and 250 MSPS. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter on the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty-cycle control loop does not function for clock rates less than 70 MHz nominally. The loop is associated with a time constant that needs to be considered in applications where the clock rate can change dynamically, requiring a wait time of 5 µs after a dynamic clock frequency increase before valid data is available. The clock duty-cycle stabilizer can be disabled at Pin 28 (S1).

The clock inputs are internally biased to 1.5 V (nominal) and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. An MC100LVEL16 performs well in the circuit to drive the clock inputs (ac coupling is optional). If the clock buffer is greater than 2 inches from the ADC, a standard LVPECL termination may be required instead of the simple pull-down termination, as shown in Figure 30.

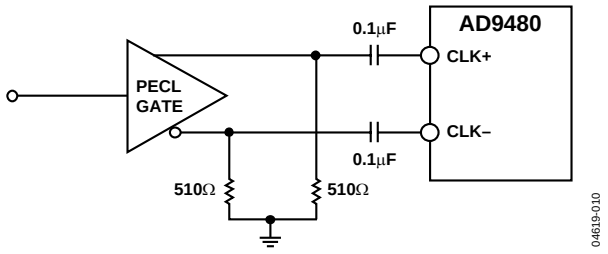


Figure 30. Clocking the AD9480

ANALOG INPUTS

The analog input to the AD9480 is a differential buffer. For best dynamic performance, impedances at VIN+ and VIN− should match. Optimal performance is obtained when the analog inputs are driven differentially. SNR and SINAD performance can degrade if the analog input is driven with a single-ended signal; however, performance can be adequate for some applications (see Figure 6). The analog inputs self-bias to approximately 1.9 V; this common-mode voltage can be externally overdriven by approximately ±300 mV if required.

A wideband transformer, such as the Mini-Circuits® ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Note that the filter and center-tap capacitor on the secondary side is optional and dependent on application requirements. An RC filter at the secondary side helps reduce any wideband noise aliased by the ADC.

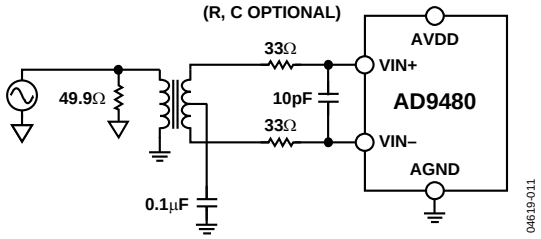


Figure 31. Driving the ADC with an RF Transformer

For dc-coupled applications, the AD8138/AD8139 or AD8351 can serve as a convenient ADC driver, depending on requirements. Figure 32 shows an example with the AD8138. The AD9480 PCB has an optional AD8351 on board, as shown in Figure 41 and Figure 42. The AD8351 typically yields better performance for frequencies greater than 30 MHz to 40 MHz.

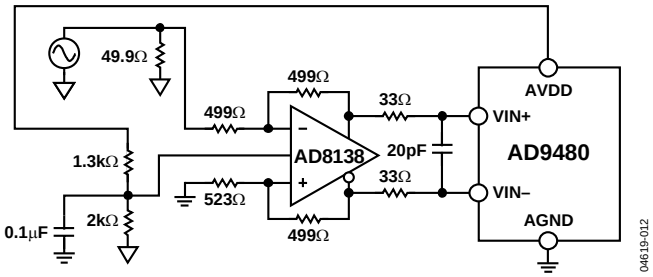


Figure 32. Driving the ADC with the AD8138

Table 8. S1 Voltage Levels

S1 Voltage	Data Format	Duty-Cycle Stabilizer
0.9 × AVDD –> AVDD	Offset binary	Disabled
2/3 AVDD ± (0.1 × AVDD)	Offset binary	Enabled
1/3 AVDD ± (0.1 × AVDD)	Twos complement	Enabled
AGND –> (0.1 × AVDD)	Twos complement	Disabled

The AD9480 can be easily configured for different full-scale ranges. See the Voltage Reference section for more information. Optimal performance is achieved with a 1 V p-p analog input.

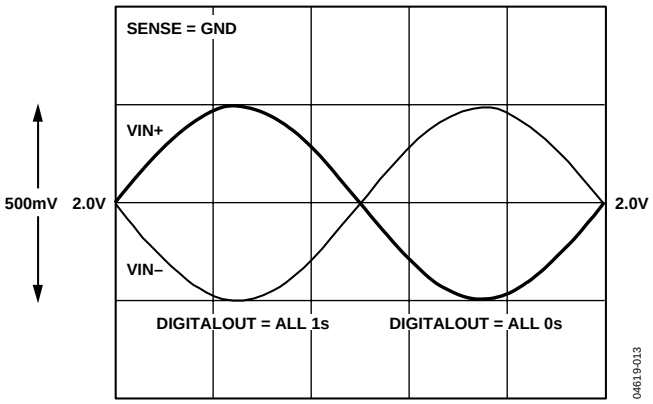


Figure 33. Analog Input Full Scale

VOLTAGE REFERENCE

A stable and accurate 1.0 V reference is built into the AD9480. Users can choose this internal reference or provide an external reference for greater accuracy and flexibility. Figure 35 shows the typical reference variation with temperature. Table 9 summarizes the available reference configurations.

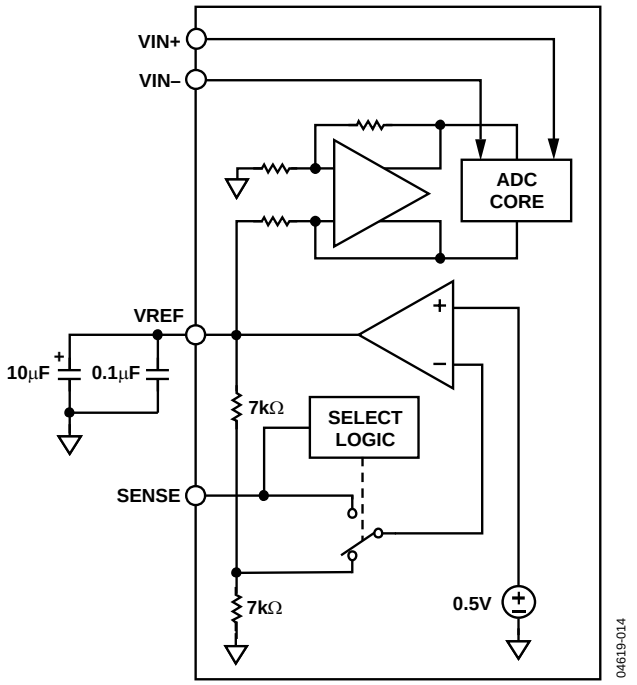


Figure 34. Internal Reference Equivalent Circuit

Fixed Reference

The internal reference can be configured for a differential span of 1 V p-p (see Figure 37). It is recommended to place a 0.1 µF capacitor as close as possible to the VREF pin; a 10 µF capacitor is also required (see the PCB layout for guidance). If the internal reference of the AD9480 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 37 depicts how the internal reference voltage is affected by loading.

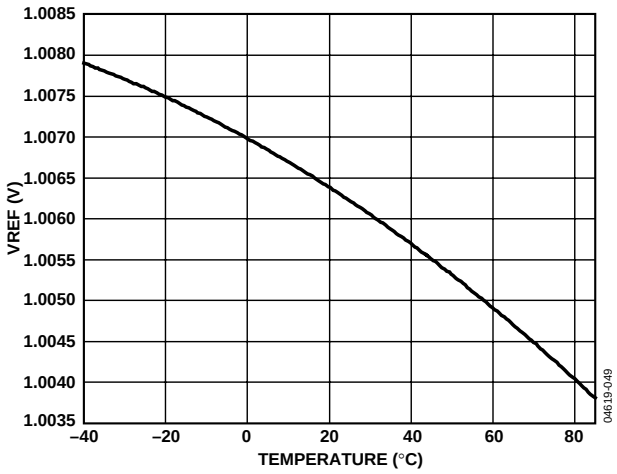


Figure 35. Typical Reference Variation with Temperature

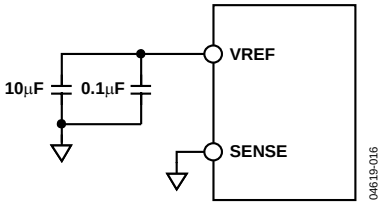


Figure 36. Internal Fixed Reference (1 V p-p)

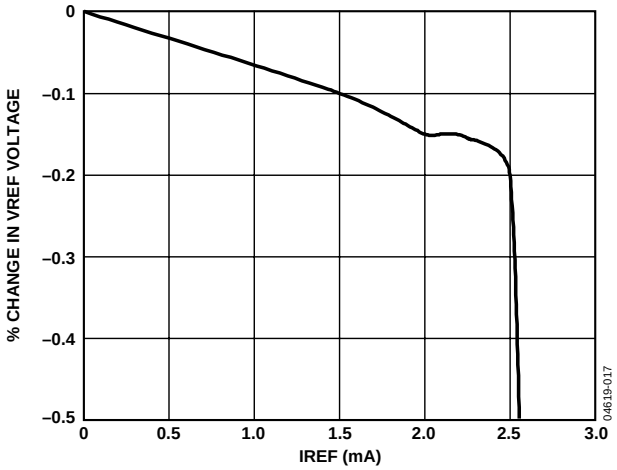


Figure 37. Internal VREF vs. Load Current

Table 9. Reference Configurations

SENSE Voltage	Resulting VREF	Reference	Differential Span
AVDD	N/A (External Reference Input)	External	1 × External Reference Voltage
0.5 V (Self-Biased)	0.5 × (1 + R1/R2) V	Programmable	1 × VREF (0.75 V p-p to 1.5 V p-p)
AGND to 0.2 V	1.0 V	Internal Fixed	1 V p-p

External Reference

An external reference can be used for greater accuracy and temperature stability when required. The gain of the AD9480 can also be varied using this configuration. A voltage output DAC can be used to set VREF, providing for a means to digitally adjust the full-scale voltage. VREF can be externally set to voltages from 0.75 V to 1.5 V; optimum performance is typically obtained at VREF = 1 V. (See the Typical Performance Characteristics section.)

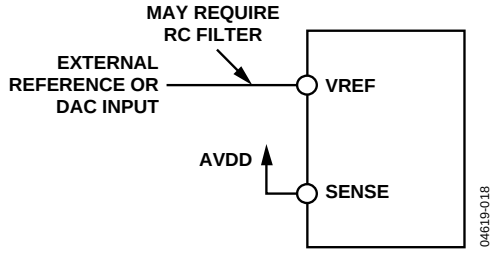


Figure 38. External Reference

Programmable Reference

The programmable reference can be used to set a differential input span anywhere between 0.75 V p-p and 1.5 V p-p by using an external resistor divider. The sense pin will self-bias to 0.5 V, and the resulting VREF is equal to 0.5 × (1 + R1/R2). It is recommended to keep the sum of R1 + R2 ≥ 10 kΩ to limit VREF loading (for VREF = 1.5 V, set R1 equal to 7 kΩ and R2 equal to 3.5 kΩ).

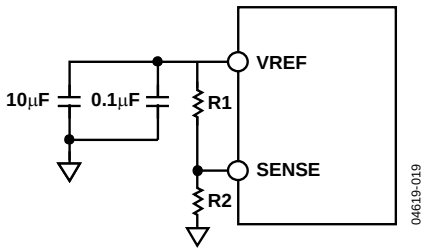


Figure 39. Programmable Reference

DIGITAL OUTPUTS

LVDS outputs are available when a 3.7 kΩ RSET resistor is placed at Pin 42 (LVDSBIAS) to ground. The RSET resistor current (~1.2 V/RSET) is ratioed on-chip, setting the output current at each output equal to a nominal 3.5 mA with an RSET of 3.74 kΩ. Varying the RSET current also linearly changes the LVDS output current, resulting in a variable output swing for a fixed termination resistance.

A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver. LVDS mode facilitates interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor as close to the receiver as possible. Keep the trace length 3 inches to 4 inches maximum and the differential output trace lengths as equal as possible.

OUTPUT CODING

Table 10.

Code	(VIN+) – (VIN–)	Offset Binary	Twos Complement
255	>+0.512 V	1111 1111	0111 1111
255	+0.512 V	1111 1111	0111 1111
254	+0.508 V	1111 1110	0111 1110
•	•	•	•
•	•	•	•
129	+0.004 V	1000 0001	0000 0001
128	+0.0 V	1000 0000	0000 0000
127	–0.004 V	0111 1111	1111 1111
•	•	•	•
•	•	•	•
2	–0.504 V	0000 0010	1000 0010
1	–0.508 V	0000 0001	1000 0001
0	–0.512 V	0000 0000	1000 0000
0	<–0.512 V	0000 0000	1000 0000

INTERLEAVING TWO AD9480s

Instrumentation applications may prefer to interleave or ping-pong two AD9480s to achieve twice the sample rate, or 500 MSPS. In these applications, it is important to match the gain and offset of the two ADCs. Varying the reference voltage allows the gain of the ADCs to be adjusted; external dc offset compensation can be used to reduce offset mismatch between two ADCs. The sampling phase offset between the two ADCs is extremely important as well and requires very low skew between clock signals driving the ADCs (<2 ps clock skew for a 100 MHz analog input frequency).

DATA CLOCK OUT

An LVDS data clock is available at DCO+ and DCO–. These clocks can facilitate latching off-chip, providing a low skew clocking solution. The on-chip delay of the DCO clocks tracks with the on-chip delay of the data bits (under similar loading), such that the variation between T_{PD} and T_{CPD} is minimized. It is recommended to keep the trace lengths on the data and DCO pins matched and to 3 inches to 4 inches maximum. The output and DCO outputs should be designed for a differential characteristic impedance of 100 Ω and terminated differentially at the receiver with 100 Ω.

POWER-DOWN

The chip can be placed in a low power state by driving the PDWN pin to logic high. Typical power-down dissipation is 15 mW. The data outputs and DCO outputs are high impedance in power-down state. The time it takes to go into power-down from assertion of PDWN is one cycle; recovery from power-down is accomplished in three cycles.

AD9480 EVALUATION BOARD

The AD9480 evaluation board offers an easy way to test the device. It requires a clock source, an analog input signal, and a 3.3 V power supply. The clock source is buffered on the board to provide the clocks for the ADC and a data-ready signal. The digital outputs and output clocks are available at a 40-pin connector, P10. The board has several modes of operation and is shipped in the following configuration:

- Offset binary
- Internal voltage reference

POWER CONNECTOR

Power is supplied to the board via two detachable 4-pin power strips.

Table 11. Power Connector

Terminal	Comments
AVDD[1] 3.3 V	Analog supply for ADC ~ 150 mA
DRVDD[1] 3.3 V	Output supply for ADC ~ 40 mA
VCTRL[1, 2] 3.3 V	Supply for support clock circuitry ~ 50 mA
Op Amp, External Reference	Optional supply for op amp and ADR510 reference

[1] AVDD, DRVDD, and VCTRL are the minimum required power connections.
[2] LVEL16 clock buffer can be powered from AVDD or VCTRL LVEL16 buffer jumper.

ANALOG INPUTS

The evaluation board accepts a 700 mV p-p analog input signal centered at ground at SMB Connector J3. This signal is terminated to ground through 50 Ω by R22. The input can be alternatively terminated at the T1 transformer secondary by R21 and R28. T1 is a wideband RF transformer that provides the single-ended-to-differential conversion, allows the ADC to be driven differentially, and minimizes even-order harmonics. An optional transformer, T4, can be placed, if desired (remove T1, as shown in Figure 41 and Figure 42).

The analog signal can be low-pass filtered by R31, C8, and R29, C9 at the ADC input.

GAIN

Full scale is set by the sense jumper. This jumper applies a bias to the SENSE pin to vary the full-scale range; the default position is SENSE = ground, setting the full scale to 1 V p-p.

OPTIONAL OPERATIONAL AMPLIFIER

The PCB has been designed to accommodate an optional AD8351 op amp, which can serve as a convenient solution for dc-coupled applications. To use the AD8351 op amp, remove R29, R31, and C3. Populate R40, R43, and R47 with 25 Ω resistors, and populate C24, C28, C29, C30, C31, and C32 with 0.1 µF capacitors. Populate R38, R39, and R51 with a 10 Ω resistor, and R44 and R45 with a 1 kΩ resistor. Populate R41 with a 1.2 kΩ resistor and R42 with a 100 Ω resistor. Populate R52 with a 10 kΩ resistor.

CLOCK

The clock input is terminated to ground through 50 Ω at SMA Connector J1. The input is ac-coupled to a high speed differential receiver (LVEL16) that provides the required low jitter and fast edge rates needed for best performance. J1 input should be >0.5 V p-p. Power to the LVEL16 is set to VCTRL (default) or AVDD by jumper placement at the device.

OPTIONAL CLOCK BUFFER

The PCB has been designed to accommodate the SNLVDS1 line driver. The SNLVDS1 is used as a high speed LVDS-level optional encode clock. To use this clock, remove C2, C5, and C6. Place a 0.1 µF capacitor on C34, C35, and C26. Place a 10 Ω resistor on R48, a 100 Ω resistor on R6, and a 0 Ω resistor on R49 and R53. For best results using the LVDS line driver, J1 input should be >2.5 V p-p.

OPTIONAL XTAL

The PCB has been designed to accommodate an optional crystal oscillator that can serve as a convenient clock source. The footprint can accept both through-hole and surface-mount devices, including Vectron XO-400 and Vectron VCC6 family oscillators.

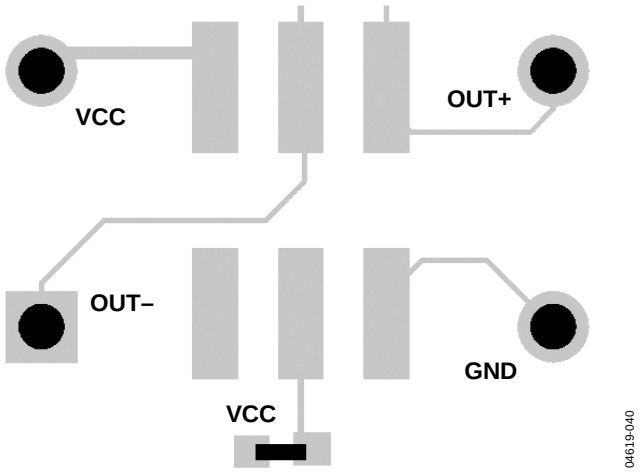


Figure 40. XTAL Footprint

To use either crystal, populate C26 and C27 with 0.1 µF capacitors. Populate R49 and R53 with 0 Ω resistors. Place 1 kΩ resistors on R54, R55, R56, and R57 and remove C6 and C5. If the Vectron VCC6 family crystal is being used, populate R48 with a 10 Ω resistor. If using the XO-400 crystal, place Jumper E21 or Jumper E22 to Jumper E23.

VOLTAGE REFERENCE

The AD9480 has an internal 1 V reference mode. The ADC uses the internal 1 V reference as the default when SENSE is set to ground. An optional on-board external 1.0 V reference (ADR510) can be used by setting the SENSE jumper to AVDD, by placing a jumper on E20 to E3, and by placing a 0 Ω resistor on R36. When using an external programmable reference (R20, R30), the SENSE jumper must be removed.

DATA OUTPUTS

The off-chip drivers provide LVDS-compatible output levels with an LVDS RSET resistor of 3.74 kΩ.

The ADC digital outputs can be terminated on the board by 100 Ω resistors at the connector if receiving logic does not have the required termination resistance. (The on-chip LVDS output drivers require a far-end, 100 Ω differential termination.)

EVALUATION BOARD BILL OF MATERIALS (BOM)

Table 12.

No.	Quantity	Reference Designator	Device	Package	Value
1	23	C1 to C6, C10 to C12, C17 to C23, C26 to C28, C31 to C33, C35	Capacitors	0402	0.1 µF
2	1	C13	Capacitor	Tantalum (3528)	10 µF
3	4	C7, C14 to C16	Capacitors	Tantalum (6032)	10 µF
4	2	J1, J3	SMAs		
5	2	P12, P13	4-pin power connector posts	Z5.531.3425.0	Wieland
6	2	P12, P13	4-pin power detachable connectors	25.602.5453.0	Wieland
7	2	R22, R27	Resistors	0603	50 Ω
8	10	R2 to R5, R7 to R10, R15, R42 (All not placed)	Resistors	0603	100 Ω
9	6	R1, R44, R45, R50, R58, R59	Resistors	0603	1000 Ω
10	1	R41	Resistors	0603	1200 Ω
11	3	R40, R43, R47	Resistors	0603	25 Ω
12	3	R38, R39, R51	Resistors	0603	10 Ω
13	2	R25, R26	Resistors	0603	82 Ω
14	2	R23, R24	Resistors	0603	510 Ω
15	2	R32, R34	Resistors	0603	130 Ω
16	2	R29, R31	Resistors	0603	0 Ω
17	2	R33, R52	Resistors	0603	10 kΩ
18	1	R63	Resistor	0603	3.74 kΩ
19	1	T1	Transformer	CD542	Mini-Circuits T1-1WT
20	1	U13	AD8351	MSOP-10	
21	1	U2	SN65LVDS1	SN65LVDS1 DBV	Not placed
22	1	U14	ADR510	SOT-23	Not placed
23	1	U15	VCC6PECL6	VCC6-QAB-250M000	Not placed
24	1	U1	XO-400	Dip4(14)	Not placed
25	1	U12	AD9480	TQFP-44	
26	1	U11	MC100LVEL16D	S08NB	
27	1	T2	ETC1-1-13	1-1 TX	Not placed
28	7	C8, C9, C24, C25, C29, C30, and C34 (All not placed)	Capacitors	0402	Not placed
29	12	R6, R20, R21, R28, R30, R36, R46, R48, R49, and R55 to R57 (All not placed)	Resistors	0603	User-determined
30	18	E5 to E8, E17, E35, E73 to E84	Jumpers		
31	1	P10	Output Data Connector	40-pin right angle	Digi-Key S2131-20-ND

PCB SCHEMATICS

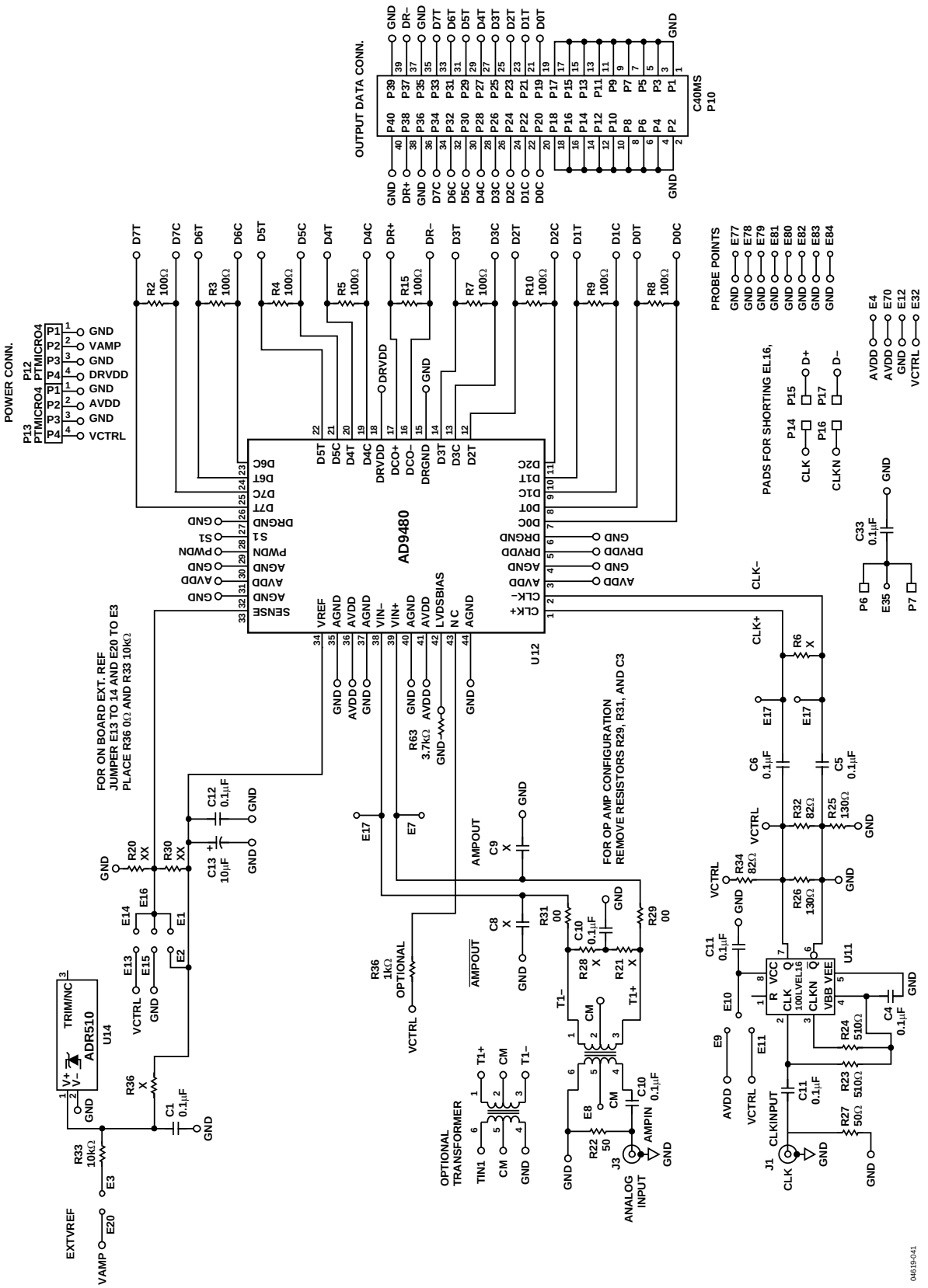


Figure 41. PCB Schematic (1 of 2)

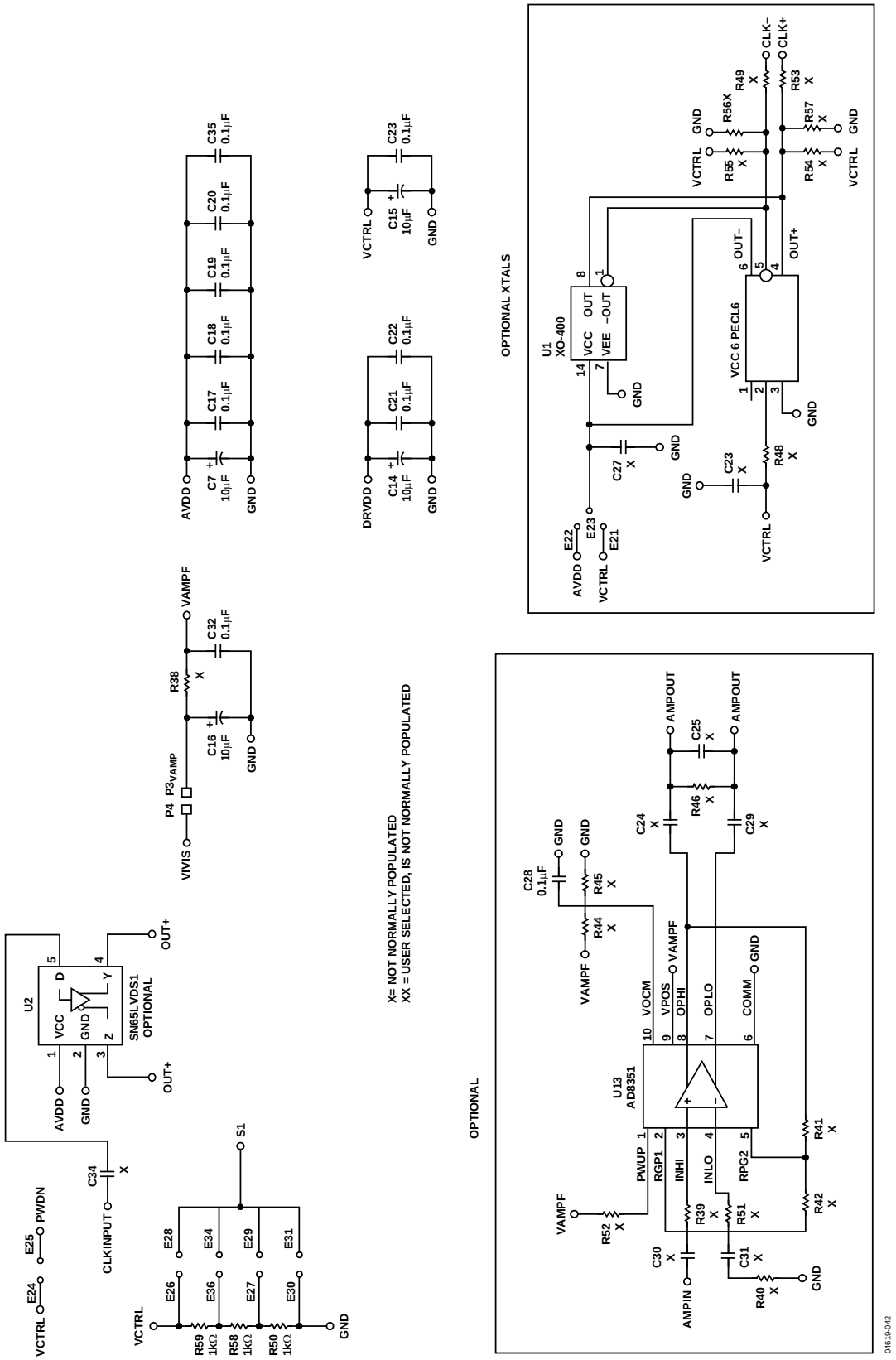


Figure 42. PCB Schematic (2 of 2)

PCB LAYERS

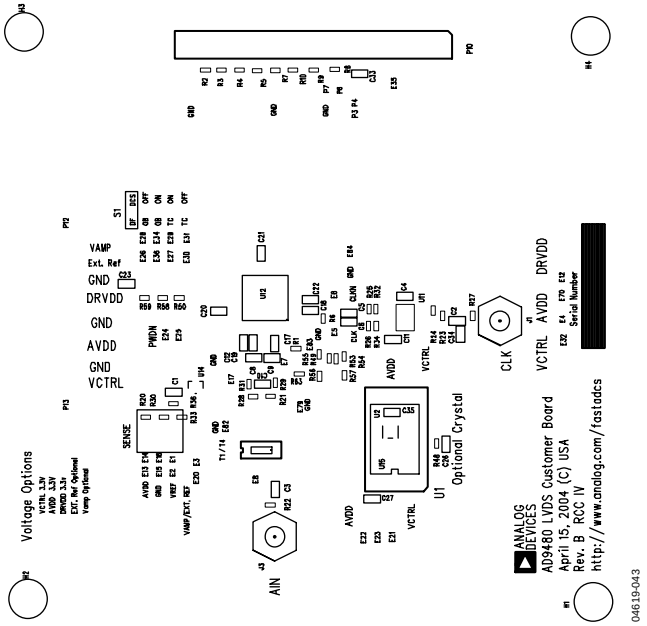


Figure 43. PCB Top-Side Silkscreen

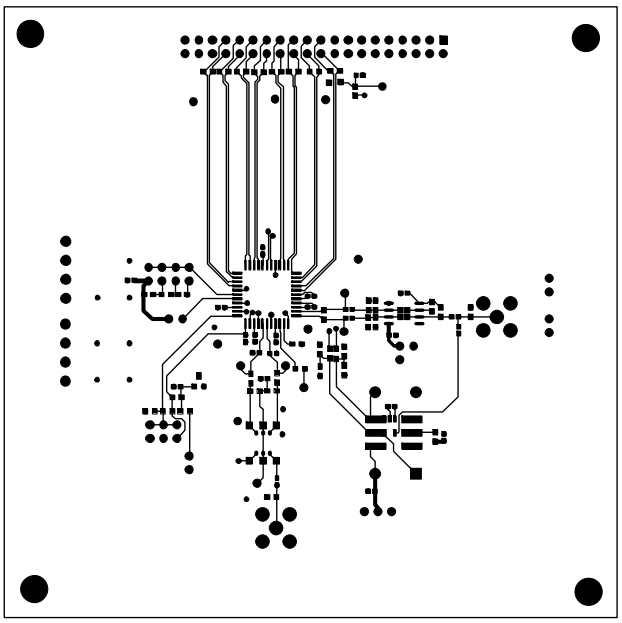


Figure 44. PCB Top-Side Copper Routing

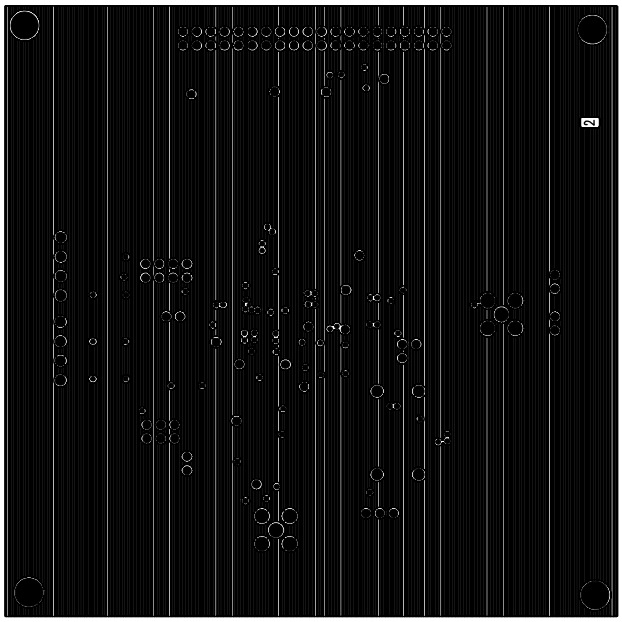


Figure 45. PCB Ground Layer

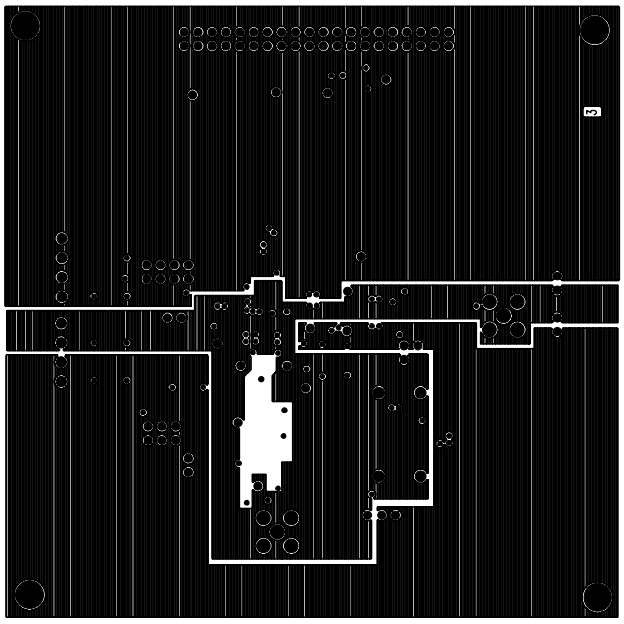


Figure 46. PCB Split Power Plane

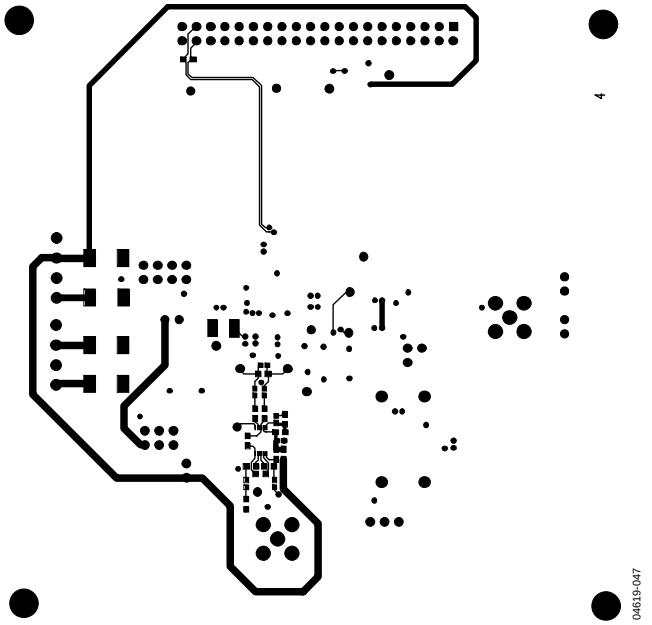


Figure 47. PCB Bottom-Side Copper Routing

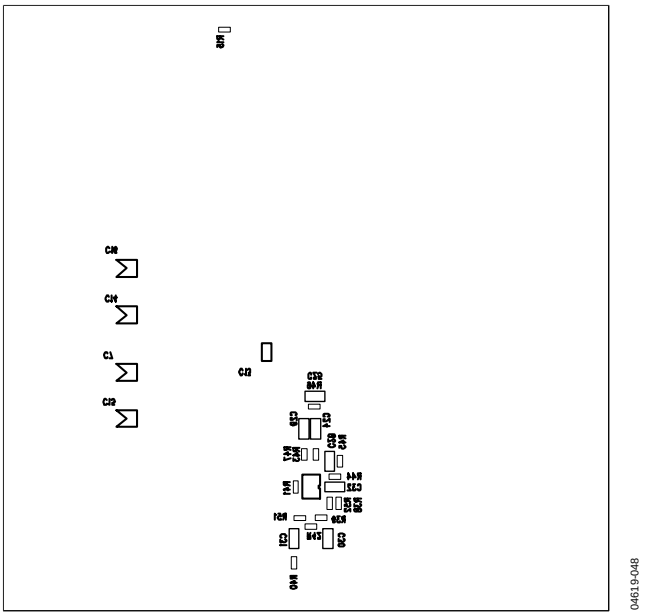
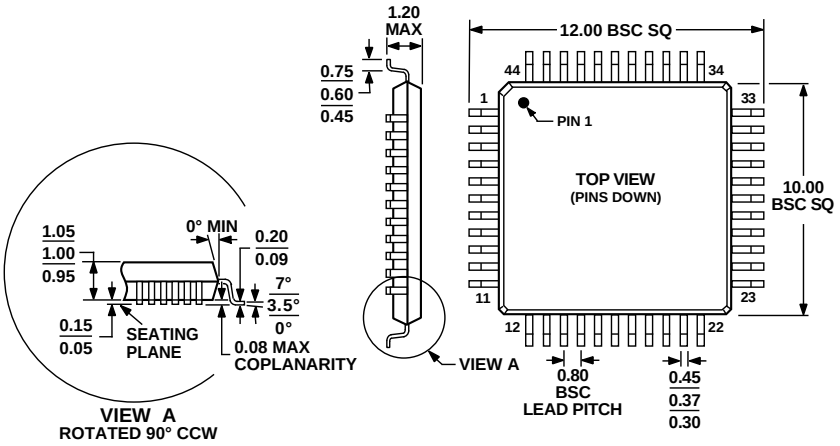


Figure 48. PCB Bottom-Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026ACB

Figure 49. 44-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-44)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Description	Package Option
AD9480BSUZ-250[1, 2]	−40°C to +85°C	44-Lead Thin Plastic Quad Flat Package (TQFP)	SU-44
AD9480ASUZ-250[1]	−40°C to +85°C	44-Lead Thin Plastic Quad Flat Package (TQFP)	SU-44
AD9480-LVDS/PCB[3]		Evaluation Board	

[1] Z = Pb-free part.
[2] Optimized differential nonlinearity.
[3] Evaluation board shipped with AD9480BSUZ-250 installed.

NOTES

NOTES

D04619–0–4/05(A)