

# AD521 — SPECIFICATIONS (typical @ $V_S = \pm 15V$ , $R_L = 2k\Omega$ and $T_A = +25^\circ C$ unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (AD521SD/883B)
<b>GAIN</b>				
Range (For Specified Operation, Note 1)	1 to 1000	*	*	*
Equation	$G = R_S/R_G V/V$	*	*	*
Error from Equation	( $\pm 0.25 - 0.004G$ )%	*	*	*
Nonlinearity (Note 2)				
$1 \leq G \leq 1000$	0.2% max	*	0.1% max	*
Gain Temperature Coefficient	$\pm (3 \pm 0.05G) \text{ppm}/^\circ C$	*	*	$\pm (15 \pm 0.4G) \text{ppm}/^\circ C$
<b>OUTPUT CHARACTERISTICS</b>				
Rated Output	$\pm 10V, \pm 10mA$ min	*	*	*
Output at Maximum Operating Temperature	$\pm 10V @ 5mA$ min	*	*	*
Impedance	0.1 $\Omega$	*	*	*
<b>DYNAMIC RESPONSE</b>				
Small Signal Bandwidth ( $\pm 3dB$ )				
$G = 1$	$> 2MHz$	*	*	*
$G = 10$	300kHz	*	*	*
$G = 100$	200kHz	*	*	*
$G = 1000$	40kHz	*	*	*
Small Signal, $\pm 1.0\%$ Flatness				
$G = 1$	75kHz	*	*	*
$G = 10$	26kHz	*	*	*
$G = 100$	24kHz	*	*	*
$G = 1000$	6kHz	*	*	*
Full Peak Response (Note 3)	100kHz	*	*	*
Slew Rate, $1 \leq G \leq 1000$	10V/ $\mu s$	*	*	*
Settling Time (any 10V step to within 10mV of Final Value)				
$G = 1$	7 $\mu s$	*	*	*
$G = 10$	5 $\mu s$	*	*	*
$G = 100$	10 $\mu s$	*	*	*
$G = 1000$	35 $\mu s$	*	*	*
Differential Overload Recovery ( $\pm 30V$ Input to within 10mV of Final Value) (Note 4)				
$G = 1000$	50 $\mu s$	*	*	*
Common Mode Overload Recovery ( $\pm 30V$ Input to within 10mV of Final Value) (Note 5)				
$G = 1000$	10 $\mu s$	*	*	*
<b>VOLTAGE OFFSET (may be nulled)</b>				
Input Offset Voltage ( $V_{OS1}$ )	1.5mV max (0.5mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15 $\mu V/^\circ C$ max (5 $\mu V/^\circ C$ typ)	5 $\mu V/^\circ C$ max (1.5 $\mu V/^\circ C$ typ)	2 $\mu V/^\circ C$ max	**
vs. Supply	3 $\mu V/\%$	*	*	*
Output Offset Voltage ( $V_{OS0}$ )	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400 $\mu V/^\circ C$ max (150 $\mu V/^\circ C$ typ)	200 $\mu V/^\circ C$ max (50 $\mu V/^\circ C$ typ)	75 $\mu V/^\circ C$ max	**
vs. Supply (Note 6)	0.005 $V_{OS0}/\%$	*	*	*
<b>INPUT CURRENTS</b>				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/ $^\circ C$ max	500pA/ $^\circ C$ max	**	**
vs. Supply	2%/V	*	*	*
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/ $^\circ C$ max	125pA/ $^\circ C$ max	**	**
<b>INPUT</b>				
Differential Input Impedance (Note 7)	$3 \times 10^9 \Omega    1.8pF$	*	*	*
Common Mode Input Impedance (Note 8)	$6 \times 10^{10} \Omega    3.0pF$	*	*	*
Input Voltage Range for Specified Performance (with respect to ground)	$\pm 10V$	*	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*	*
Voltage at either input (Note 9)	$V_S \pm 15V$	*	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1k $\Omega$ source unbalance				
$G = 1$	70dB min (74dB typ)	74dB min (80dB typ)	**	**
$G = 10$	90dB min (94dB typ)	94dB min (100dB typ)	**	**
$G = 100$	100dB min (104dB typ)	104dB min (114dB typ)	**	**
$G = 1000$	100dB min (110dB typ)	110dB min (120dB typ)	**	**
<b>NOISE</b>				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2} \mu V$	*	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2} \mu V$	*	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*	*
<b>REFERENCE TERMINAL</b>				
Bias Current	3 $\mu A$	*	*	*
Input Resistance	10M $\Omega$	*	*	*
Voltage Range	$\pm 10V$	*	*	*
Gain to Output	1	*	*	*
<b>POWER SUPPLY</b>				
Operating Voltage Range	$\pm 5V$ to $\pm 18V$	*	*	*
Quiescent Supply Current	5mA max	*	*	*
<b>TEMPERATURE RANGE</b>				
Specified Performance	0 to $+70^\circ C$	*	*	$-55^\circ C$ to $+125^\circ C$
Operating	$-25^\circ C$ to $+85^\circ C$	*	*	$-55^\circ C$ to $+125^\circ C$
Storage	$-65^\circ C$ to $+150^\circ C$	*	*	*

\*Specifications same as AD521JD.

\*\*Specifications same as AD521KD.

Specifications subject to change without notice.

## NOTES:

1. Gains below 1 and above 1000 are obtained by simply adjusting the gain setting resistors. (Input voltage should be restricted to  $\pm 10V$  for gains equal to or less than 1.)
2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of  $\pm 9$  volts. With a combination of high gain and  $\pm 10$  volt output swing, distortion may increase to as much as 0.3%.
3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.
4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10 $\mu$ s pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)
5. Common Mode Size Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10 $\mu$ s pulse at a 1kHz rate. (When a common mode signal greater than  $V_S - 0.5V$  is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

mon mode signal greater than  $V_S - 0.5V$  is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply includes a constant 0.005 times the unnullled output offset per percent change in either power supply. If the output offset is nullled, the output offset change versus supply change is substantially reduced.
7. Differential Input Impedance is the impedance between the two inputs.
8. Common Mode Input Impedance is the impedance from either input to the power supplies.
9. Maximum Input Voltage (differential or at either input) is 30V when using  $\pm 15V$  supplies. A more general specification is that neither input may exceed either supply (even when  $V_S = 0$ ) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)
10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 8.

## ORDERING GUIDE

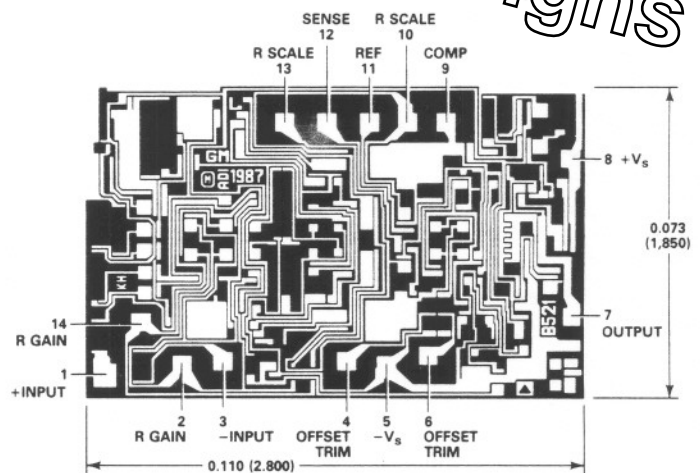
Model	Temperature Range	Description	Package Option <sup>1</sup>
AD521JD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521KD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521LD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521SD	-55°C to +125°C	14-Pin Ceramic DIP	D-14
AD521SD/883B <sup>2</sup>	-55°C to +125°C	14-Pin Ceramic DIP	D-14
AD521J Chips	0°C to +70°C	Die	
AD521K Chips	0°C to +70°C	Die	
AD521S Chips	-55°C to +125°C	Die	

## NOTES

- <sup>1</sup>For outline information see Package Information section.  
<sup>2</sup>Standard military drawing available.

## METALLIZATION PHOTOGRAPH

Dimensions shown in inches and millimeters.  
 Contact factory for latest dimensions.





# AD521

## DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage,  $V_{IN}$ , appears across  $R_G$  causing an imbalance in the currents through  $Q_1$  and  $Q_2$ ,  $\Delta I = V_{IN}/R_G$ . That imbalance is forced to flow in  $R_S$  because the collector currents of  $Q_3$  and  $Q_4$  are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across  $R_S$  (and hence the output voltage of the AD521) is equal to  $\Delta I \times R_S$ . The feedback amplifier,  $A_{FB}$

performs that function. Therefore,  $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$  or  $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$

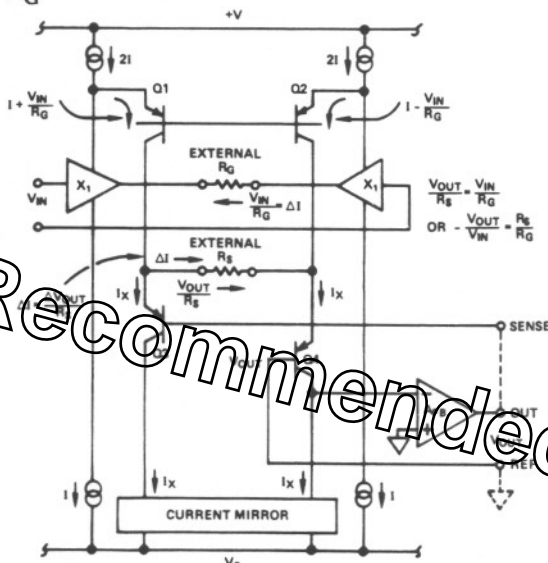


Figure 1. Simplified AD521 Schematic

## APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor,  $R_S$  between pins 10 and 13 should remain  $100k\Omega \pm 15\%$ , see application note 3). For best results, the input voltage should be restricted to  $\pm 10V$  even though the gain may be less than 1. See Figure 6 for gains above 1000.
2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.
3. The resistors between pins 10 and 13, ( $R_{SCALE}$ ) must equal  $100k\Omega \pm 15\%$  (Figure 2). If  $R_{SCALE}$  is too low (below  $85k\Omega$ ) the output swing of the AD521 is reduced. At values below  $80k\Omega$  and above  $120k\Omega$  the stability of the AD521 may be impaired.

4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor  $R/2$  matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce  $680\Omega$  to  $24\Omega$
2. Reduce  $330\Omega$  to  $7.5\Omega$
3. Increase  $1000pF$  to  $0.1\mu F$
4. Set  $C_X$  to  $1000pF$  if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to  $1000pF$ , but limits the slew rate to approximately  $0.16V/\mu s$ .

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from  $V_-$  to the output with little or no attenuation. Therefore, it is advisable to decouple the  $V_-$  supply line to the output common or to pin 11.

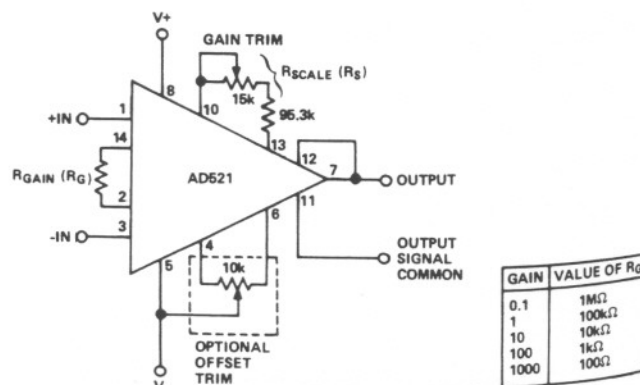
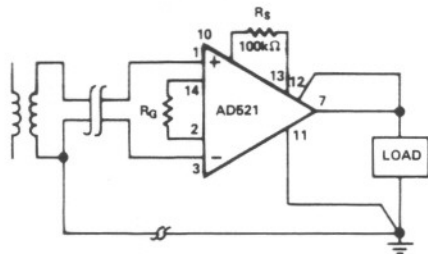
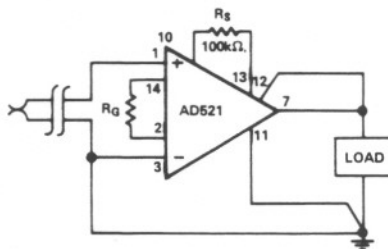


Figure 2. Operating Connections for AD521

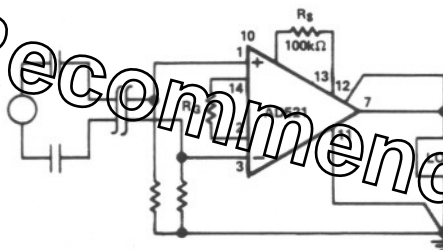
<sup>1</sup> For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.



a). Transformer Coupled, Direct Return

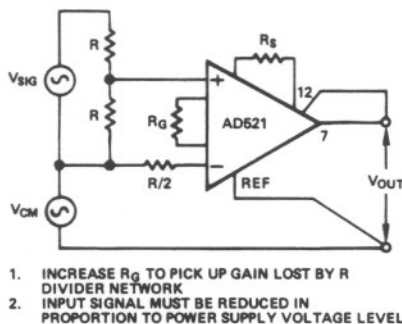


b). Thermocouple, Direct Return

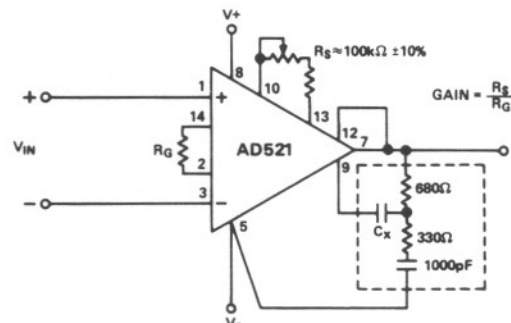


c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE  $R_G$  TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for  $V_{IN} \approx V_S = 10V$ 

$$C_X = \frac{1}{100\pi f_t} \text{ when } f_t \text{ is the desired bandwidth.}$$

( $f_t$  in kHz,  $C_X$  in  $\mu F$ )

Figure 5. Optional Compensation Circuit

### INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the total output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or:  $30mV + 100(-0.7mV) = -40mV$ .

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

$$\text{Total Error R.T.I.} = \text{input error} + (\text{output error}/\text{gain})$$

$$\text{Total Error R.T.O.} = (\text{Gain} \times \text{input error}) + \text{output error}$$

The offset trim adjustment (pins 4 and 5, Figure 2) is associated primarily with the output offset. A unity gain can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio,  $R_S/R_G$ ). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by  $R_1$  and  $R_2$ . This gain factor is  $1 + R_2/R_1$ .

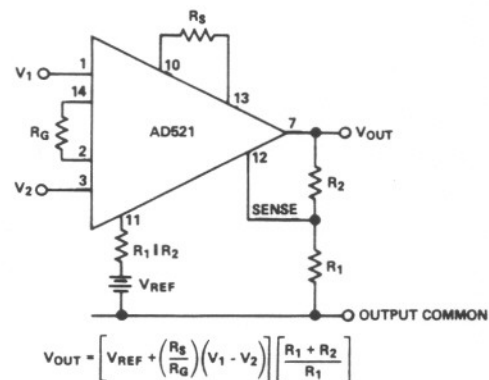


Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing  $R_1$  and  $R_2$  will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

Not Recommended for new Designs



## AD521

Where offset errors are critical, a resistor equal to the parallel combination of  $R_1$  and  $R_2$  should be placed between pin 11 and  $V_{REF}$ . This minimizes the offset errors resulting from the input current flowing in  $R_1$  and  $R_2$  at the sense terminal. Note that gain changes introduced by changing the  $R_1/R_2$  attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired,  $V_{REF}$  can be placed in series with pin 11. This offset is then multiplied by the gain factor  $1 + R_2/R_1$  as shown in the equation of Figure 6.

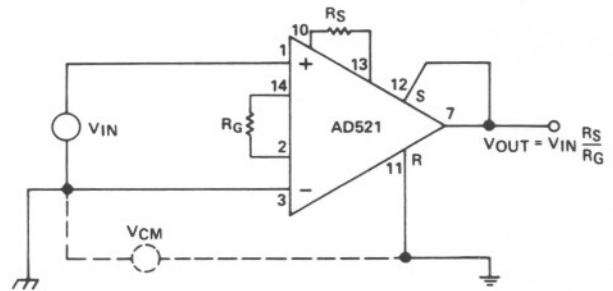


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

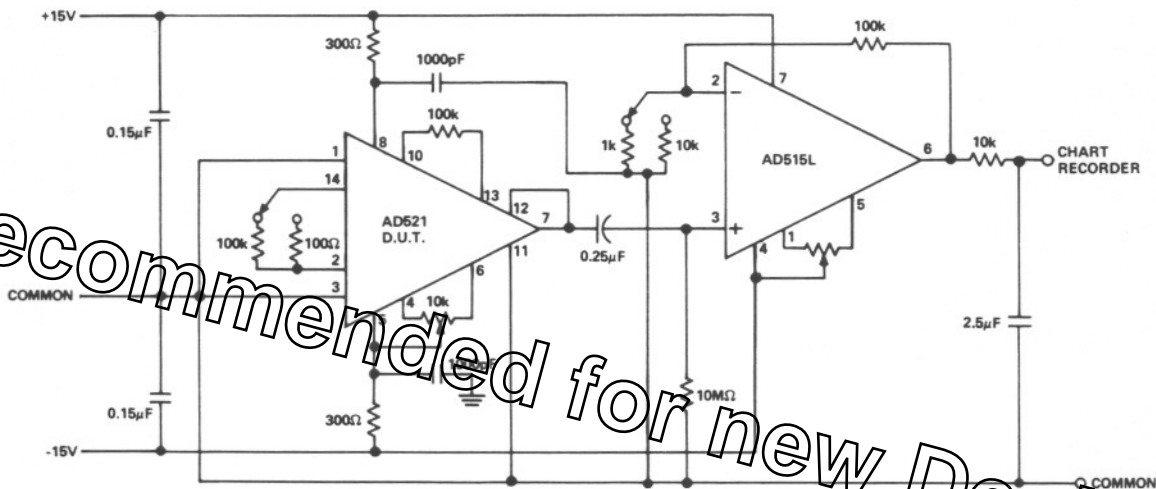


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.