2. Pin Configuration

Figure 2-1. Pinning DIP18

Note: The DIP18 package is no longer available and has end-of-life status. For new developments please use the SO16 package.

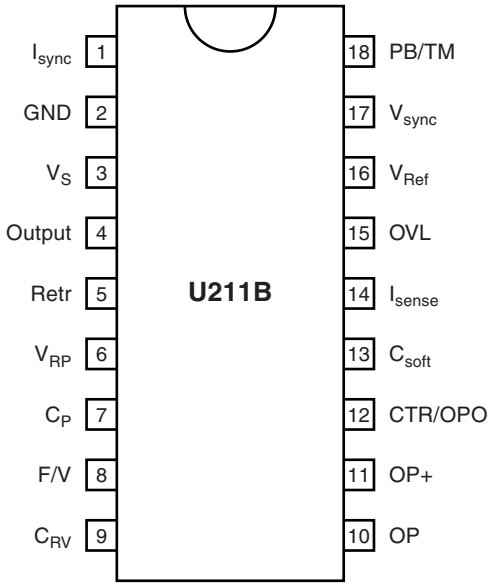


Table 2-1. Pin Description

Pin	Symbol	Function
1	I_{sync}	Current synchronization
2	GND	Ground
3	V_S	Supply voltage
4	Output	Trigger pulse output
5	Retr	Retrigger programming
6	V_{RP}	Ramp current adjust
7	C_P	Ramp voltage
8	F/V	Frequency-to-voltage converter
9	C_{RV}	Charge pump
10	OP-	OP inverting input
11	OP+	OP non-inverting input
12	CTR/OPO	Control input/OP output
13	C_{soft}	Soft start
14	I_{sense}	Load-current sensing
15	OVL	Overload adjust
16	V_{Ref}	Reference voltage
17	V_{sync}	Voltage synchronization
18	PB/TM	Pulse blocking/tacho monitoring

Figure 2-2. Pinning SO16

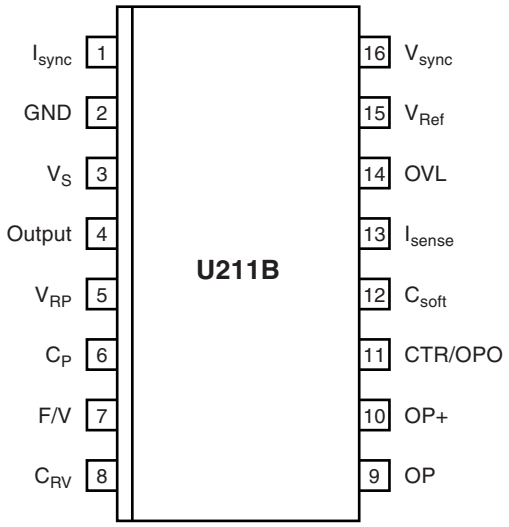


Table 2-2. Pin Description

Pin	Symbol	Function
1	I_{sync}	Current synchronization
2	GND	Ground
3	V_S	Supply voltage
4	Output	Trigger pulse output
5	V_{RP}	Ramp current adjust
6	C_P	Ramp voltage
7	F/V	Frequency-to-voltage converter
8	C_{RV}	Charge pump
9	OP-	OP inverting input
10	OP+	OP non-inverting input
11	CTR/OPO	Control input/OP output
12	C_{soft}	Soft start
13	I_{sense}	Load-current sensing
14	OVL	Overload adjust
15	V_{Ref}	Reference voltage
16	V_{sync}	Voltage synchronization

3. Mains Supply [1)]

The Atmel® U211B is equipped with voltage limiting and can therefore be supplied directly from the mains. The supply voltage between pin 2 (+ pol/_|_) and pin 3 builds up across D_1 and R_1 and is smoothed by C_1. The value of the series resistance can be approximated using:

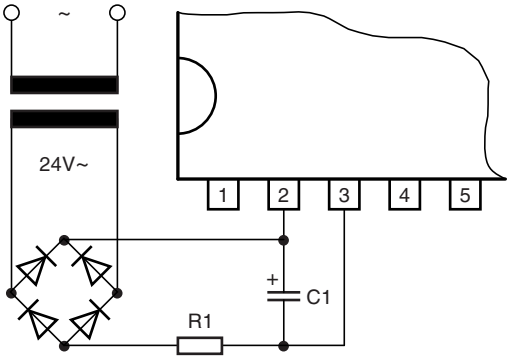
$$R_1 = \frac{V_M - V_S}{2\, I_S}$$

Further information regarding the design of the mains supply can be found in the section “Design Hints 1)” on page 10. The reference voltage source on pin 16 of typically –8.9V is derived from the supply voltage and is used for regulation.

Operation using an externally stabilized DC voltage is not recommended.

If the supply cannot be taken directly from the mains because the power dissipation in R_1 would be too large, the circuit as shown in Figure 3-1 should be used.

Figure 3-1. Supply Voltage for High Current Requirements



Note: 1. The descripten refers to the DIP18 package version which is no longer available.

4. Phase Control [1)]

The phase angle of the trigger pulse is derived by comparing the ramp voltage (which is mains synchronized by the voltage detector) with the set value on the control input pin 12. The slope of the ramp is determined by C_2 and its charging current. The charging current can be varied using R_2 on pin 6. The maximum phase angle α_{max} can also be adjusted by using R_2.

When the potential on pin 7 reaches the nominal value predetermined at pin 12, a trigger pulse is generated whose width t_p is determined by the value of C_2 (the value of C_2 and hence the pulse width can be evaluated by assuming 8µs/nF). At the same time, a latch is set, so that as long as the automatic retriggering has not been activated, no more pulses can be generated in that half cycle.

The current sensor on pin 1 ensures that, for operations with inductive loads, no pulse will be generated in a new half cycle as long as a current from the previous half cycle is still flowing in the opposite direction to the supply voltage at that instant. This makes sure that “gaps” in the load current are prevented.

The control signal on pin 12 can be in the range of 0V to –7V (reference point pin 2).

If $V_{12} = –7V$, the phase angle is at maximum (α_{max}), i.e., the current flow angle, is at minimum. The phase angle is minimum (α_{min}) when $V_{12} = V_2$.

5. Voltage Monitoring [1)]

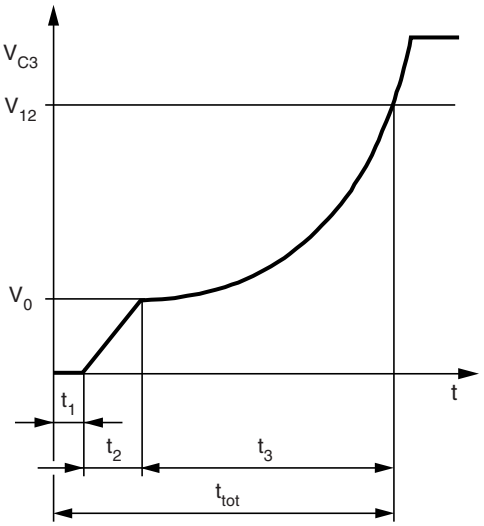
As the voltage is built up, uncontrolled output pulses are avoided by internal voltage surveillance. At the same time, all latches in the circuit (phase control, load limit regulation, soft start) are reset and the soft-start capacitor is short circuited. Used with a switching hysteresis of 300mV, this system guarantees defined start-up behavior each time the supply voltage is switched on or after short interruptions of the mains supply.

Note: 1. The descripten refers to the DIP18 package version which is no longer available.

6. Soft Start [1)]

As soon as the supply voltage builds up (t_1), the integrated soft start is initiated. Figure 6-1 shows the behavior of the voltage across the soft-start capacitor, which is identical with the voltage on the phase-control input on pin 12. This behavior guarantees a gentle start-up for the motor and automatically ensures the optimum run-up time.

Figure 6-1. Soft Start



t_1 = Build-up of supply voltage
t_2 = Charging of C_3 to starting voltage
$t_1 + t_2$ Dead time
t_3 = Run-up time
t_{tot} = Total start-up time to required speed

C_3 is first charged up to the starting voltage V_0 with a current of typically 45µA (t_2). By reducing the charging current to approximately 4µA, the slope of the charging function is also substantially reduced, so that the rotational speed of the motor only slowly increases. The charging current then increases as the voltage across C_3 increases, resulting in a progressively rising charging function which accelerates the motor more and more with increasing rotational speed. The charging function determines the acceleration up to the set point. The charging current can have a maximum value of 55µA.

Note: 1. The descripten refers to the DIP18 package version which is no longer available.

7. Frequency-to-voltage Converter [1)]

The internal frequency-to-voltage converter (f/V converter) generates a DC signal on pin 10 which is proportional to the rotational speed, using an AC signal from a tacho generator or a light beam whose frequency is in turn dependent on the rotational speed. The high-impedance input pin 8 compares the tacho voltage to a switch-on threshold of typically –100mV. The switch-off threshold is –50mV. The hysteresis guarantees very reliable operation even when relatively simple tacho generators are used.

The tacho frequency is given by:

$$f = \frac{n}{60} \times p \text{ (Hz)}$$

where: n = Revolutions per minute
p = Number of pulses per revolution

The converter is based on the charge pumping principle. With each negative half-wave of the input signal, a quantity of charge determined by C_5 is internally amplified and then integrated by C_6 at the converter output on pin 10. The conversion constant is determined by C_5, its charge transfer voltage of V_{ch}, R_6 (pin 10) and the internally adjusted charge transfer gain.

$$G_i\left[\frac{I_{10}}{I_9}\right] = 8.3$$

$$k = G_i \times C_5 \times R_6 \times V_{ch}$$

The analog output voltage is given by

$$V_O = k \times f$$

The values of C_5 and C_6 must be such that for the highest possible input frequency, the maximum output voltage V_O does not exceed 6V. While C_5 is charging up, the R_i on pin 9 is approximately 6.7kΩ. To obtain good linearity of the f/V converter, the time constant resulting from R_i and C_5 should be considerably less (1/5) than the time span of the negative half-cycle for the highest possible input frequency. The amount of remaining ripple on the output voltage on pin 10 is dependent on C_5, C_6 and the internal charge amplification.

$$\Delta V_O = \frac{G_i \times V_{ch} \times C_5}{C_6}$$

The ripple ΔV_O can be reduced by using larger values of C_6. However, the increasing speed will then also be reduced.

The value of this capacitor should be chosen to fit the particular control loop where it is going to be used.

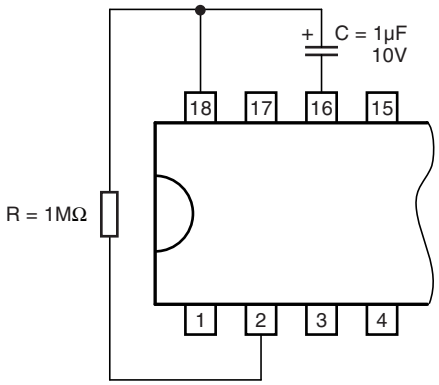
Note: 1. The descripten refers to the DIP18 package version which is no longer available.

7.1 Pulse Blocking [1)]

The output of pulses can be blocked by using pin 18 (standby operation) and the system reset via the voltage monitor if $V_{18} \geq -1.25V$. After cycling through the switching point hysteresis, the output is released when $V_{18} \leq -1.5V$, followed by a soft start such as after turn-on.

Monitoring of the rotation can be carried out by connecting an RC network to pin 18. In the event of a short or open circuit, the triac triggering pulses are cut off by the time delay which is determined by R and C. The capacitor C is discharged via an internal resistance $R_i = 2k\Omega$ with each charge transfer process of the f/V converter. If there are no more charge transfer processes, C is charged up via R until the switch-off threshold is exceeded and the triac triggering pulses are cut off. For operation without trigger pulse blocking or monitoring of the rotation, pin 18 and pin 16 must be connected together.

Figure 7-1. Operation Delay



7.2 Control Amplifier [1)]

The integrated control amplifier (see Figure 10-17 on page 22) with differential input compares the set value (pin 11) with the instantaneous value on pin 10, and generates a regulating voltage on the output pin 12 (together with the external circuitry on pin 12). This pin always tries to keep the actual voltage at the value of the set voltages. The amplifier has a transmittance of typically 1000µA/V and a bipolar current source output on pin 12 which operates with typically ±110µA. The amplification and frequency response are determined by R_7, C_7, C_8 and R_{11} (can be left out). For open-loop operation, C_4, C_5, R_6, R_7, C_7, C_8 and R_{11} can be omitted. Pin 10 should be connected with pin 12 and pin 8 with pin 2. The phase angle of the triggering pulse can be adjusted by using the voltage on pin 11. An internal limitation circuit prevents the voltage on pin 12 from becoming more negative than $V_{16} + 1V$.

7.3 Load Limitation [1)]

The load limitation, with standard circuitry, provides full protection against overloading of the motor. The function of load limiting takes account of the fact that motors operating at higher speeds can safely withstand larger power dissipations than at lower speeds due to the increased action of the cooling fan. Similarly, considerations have been made for short-term overloads for the motor which are, in practice, often required. These behaviors are not damaging and can be tolerated.

Note: 1. The descripten refers to the DIP18 package version which is no longer available.

In each positive half-cycle, the circuit measures, via R_{10}, the load current on pin 14 as a potential drop across R_8 and produces a current proportional to the voltage on pin 14. This current is available on pin 15 and is integrated by C_9. If, following high-current amplitudes or a large phase angle for current flow, the voltage on C_9 exceeds an internally set threshold of approximately 7.3V (reference voltage pin 16), a latch is set and load limiting is turned on. A current source (sink) controlled by the control voltage on pin 15 now draws current from pin 12 and lowers the control voltage on pin 12 so that the phase angle α is increased to α_{max}.

The simultaneous reduction of the phase angle during which current flows causes firstly a reduction of the rotational speed of the motor which can even drop to zero if the angular momentum of the motor is excessively large, and secondly a reduction of the potential on C_9 which in turn reduces the influence of the current sink on pin 12. The control voltage can then increase again and bring down the phase angle. This cycle of action sets up a “balanced condition” between the “current integral” on pin 15 and the control voltage on pin 12.

Apart from the amplitude of the load current and the time during which current flows, the potential on pin 12 and hence the rotational speed also affects the function of load limiting. A current proportional to the potential on pin 10 gives rise to a voltage drop across R_{10}, via pin 14, so that the current measured on pin 14 is smaller than the actual current through R_8.

This means that higher rotational speeds and higher current amplitudes lead to the same current integral. Therefore, at higher speeds, the power dissipation must be greater than that at lower speeds before the internal threshold voltage on pin 15 is exceeded. The effect of speed on the maximum power is determined by the resistor R_{10} and can therefore be adjusted to suit each individual application.

If, after load limiting has been turned on, the momentum of the load sinks below the “o-momentum” set using R_{10}, V_{15} will be reduced. V_{12} can then increase again so that the phase angle is reduced. A smaller phase angel corresponds to a larger momentum of the motor and hence the motor runs up, as long as this is allowed by the load momentum. For an already rotating machine, the effect of rotation on the measured “current integral” ensures that the power dissipation is able to increase with the rotational speed. The result is a current-controlled acceleration run-up which ends in a small peak of acceleration when the set point is reached. The load limiting latch is simultaneously reset. Then the speed of the motor is under control again and is capable of carrying its full load. The above mentioned peak of acceleration depends upon the ripple of actual speed voltage. A large amount of ripple also leads to a large peak of acceleration.

The measuring resistor R_8 should have a value which ensures that the amplitude of the voltage across it does not exceed 600mV.

Note: 1. The descripten refers to the DIP18 package version which is no longer available.

7.4 Design Hints [1)]

Practical trials are normally needed for the exact determination of the values of the relevant components for load limiting. To make this evaluation easier, the following table shows the effect of the circuitry on the important parameters for load limiting and summarizes the general tendencies.

Table 7-1. Load Limiting Parameters

Parameters	Component R_{10} Increasing	Component R_9 Increasing	Component C_9 Increasing
P_{max}	Increases	Decreases	n.e.
P_{min}	Increases	Decreases	n.e.
$P_{max/min}$	Increases	n.e.	n.e.
t_d	n.e.	Increases	Increases
t_r	n.e.	Increases	Increases

P_{max} - Maximum continuous power dissipation $P_1 = f_{(n)}\ n \neq 0$
P_{min} - Power dissipation with no rotation $P_1 = f_{(n)}\ n = 0$
t_d - Operation delay time
t_r - Recovery time
n.e. - No effect

7.5 Pulse-output Stage [1)]

The pulse-output stage is short-circuit protected and can typically deliver currents of 125mA. For the design of smaller triggering currents, the function $I_{GT} = f(R_{GT})$ can be taken from Figure 10-12 on page 19.

7.6 Automatic Retriggering [1)]

The variable automatic retriggering prevents half cycles without current flow, even if the triac has been turned off earlier, e.g., due to a collector which is not exactly centered (brush lifter) or in the event of unsuccessful triggering. If necessary, another triggering pulse is generated after a time lapse which is determined by the repetition rate set by resistance between pin 5 and pin 3 (R_{5-3}). With the maximum repetition rate (pin 5 directly connected to pin 3), the next attempt to trigger comes after a pause of 4.5 t_p and this is repeated until either the triac fires or the half cycle finishes. If pin 5 is not connected, only one trigger pulse per half cycle is generated. Since the value of R_{5-3} determines the charging current of C_2, any repetition rate set using R_{5-3} is only valid for a fixed value of C_2.

Note: 1. The descripten refers to the DIP18 package version which is no longer available.

7.7 General Hints and Explanation of Terms [1)]

To ensure safe and trouble-free operation, the following points should be taken into consideration when circuits are being constructed or in the design of printed circuit boards.

- The connecting lines from C_2 to pin 7 and pin 2 should be as short as possible. The connection to pin 2 should not carry any additional high current such as the load current. When selecting C_2, a low temperature coefficient is desirable.
- The common (earth) connections of the set-point generator, the tacho generator and the final interference suppression capacitor C_4 of the f/V converter should not carry load current.
- The tacho generator should be mounted without influence by strong stray fields from the motor.
- The connections from R_{10} and C_5 should be as short as possible.

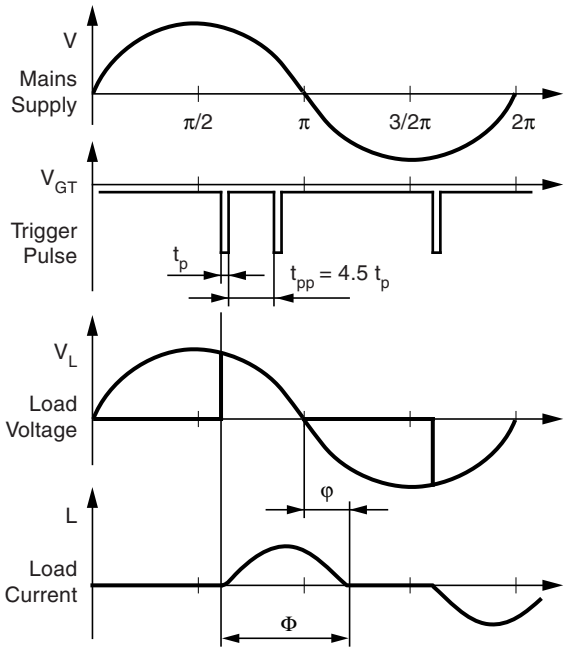
To achieve a high noise immunity, a maximum ramp voltage of 6V should be used. The typical resistance R_φ can be calculated from I_φ as follows:

$$R_\varphi(k\Omega) = \frac{T(ms) \times 1.13(V) \times 10^3}{C(nF) \times 6(V)}$$

T = Period duration for mains frequency (10ms at 50Hz)
C_φ = Ramp capacitor, maximum ramp voltage 6V and constant voltage drop at R_φ = 1.13V

A 10% lower value of R_φ (under worst case conditions) is recommended.

Figure 7-2. Explanation of Terms in Phase Relationship



Note: 1. The descripten refers to the DIP18 package version which is no longer available.

7.8 Design Calculations for Main Supply [1)]

The following equations can be used for the evaluation of the series resistor R_1 for worst case conditions:

$$R_{1max} = 0.85 \frac{V_{Mmin} - V_{Smax}}{2\, I_{tot}} \qquad R_{1min} = \frac{V_M - V_{Smin}}{2\, I_{Smax}}$$

$$P_{(R1max)} = \frac{(V_{Mmax} - V_{Smin})^2}{2\, R_1}$$

where:

V_M = Mains voltage
V_S = Supply voltage on pin 3
I_{tot} = Total DC current requirement of the circuit
= $I_S + I_p + I_x$
I_{Smax} = Current requirement of the IC in mA
I_p = Average current requirement of the triggering pulse
I_x = Current requirement of other peripheral components

R_1 can be easily evaluated from the Figure 10-14 on page 20, Figure 10-15 on page 20 and Figure 10-16 on page 21.

Note: 1. The descripten refers to the DIP18 package version which is no longer available.

8. Absolute Maximum Ratings

Reference point pin 2, unless otherwise specified.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pins [1]	Symbol	Value	Unit
Current requirement	3	$-I_S$	30	mA
$t \leq 10\mu s$	3	$-i_s$	100	mA
Synchronization current	1	I_{syncI}	5	mA
	17	I_{syncV}	5	mA
$t < 10\mu s$	1	$\pm i_I$	35	mA
$t < 10\mu s$	17	$\pm i_I$	35	mA
f/V Converter				
Input current	8	I_I	3	mA
$t < 10\mu s$	8	$\pm i_I$	13	mA
Load Limiting				
Limiting current, negative half wave	14	I_I	5	mA
$t < 10\mu s$	14	I_I	35	mA
Input voltage	14	$\pm V_i$	1	V
	15	$-V_I$	$\lvert V_{16}\rvert$ to 0	V
Phase Control				
Input voltage	12	$-V_I$	0 to 7	V
Input current	12	$\pm I_I$	500	µA
	6	$-I_I$	1	mA
Soft Start				
Input voltage	13	$-V_I$	$\lvert V_{16}\rvert$ to 0	V
Pulse Output				
Reverse voltage	4	V_R	V_S to 5	V
Pulse Blocking				
Input voltage	18	$-V_I$	$\lvert V_{16}\rvert$ to 0	V
Amplifier				
Input voltage	11	V_I	0 to V_S	V
Pin 9 open	10	$-V_I$	$\lvert V_{16}\rvert$ to 0	V
Reference Voltage Source				
Output current	16	I_o	7.5	mA
Storage temperature range		T_{stg}	–40 to +125	°C
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	–10 to +100	°C

Note: 1. The pins refer to the DIP18 package version which is no longer available.

9. Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	SO16 on p.c. SO16 on ceramic	R_{thJA} R_{thJA}	180 100	K/W K/W

10. Electrical Characteristics

$-V_S$ = 13.0V, T_{amb} = 25°C, reference point pin 2, unless otherwise specified

Parameters	Test Conditions	Pins [1]	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for mains operation		3	$-V_S$	13.0		V_{Limit}	V
Supply voltage limitation	$-I_S$ = 4mA $-I_S$ = 30mA	3	$-V_S$	14.6 14.7		16.6 16.8	V V
DC current requirement	$-V_S$ = 13.0V	3	I_S	1.2	2.5	3.0	mA
Reference voltage source	$-I_L$ = 10µA $-I_L$ = 5mA	16	$-V_{Ref}$	8.6 8.3	8.9	9.2 9.1	V V
Temperature coefficient		16	$-TC_{VRef}$		0.5		mV/K
Voltage Monitoring							
Turn-on threshold		3	$-V_{SON}$	11.2	13.0		V
Turn-off threshold		3	$-V_{SOFF}$	9.9	10.9		V
Phase-control Currents							
Synchronization current		1 17	$\pm I_{syncI}$ $\pm I_{syncV}$	0.35		2.0	mA
Voltage limitation	$\pm I_L$ = 5mA	1, 17	$\pm V_I$	1.4	1.6	1.8	V
Reference Ramp (see Figure 10-1 on page 16)							
Charge current	$I_7 = f(R_6)$ R_6 = 50kΩ to 1MΩ	7	I_7	1	20		µA
R_φ-reference voltage	$\alpha \geq 180°$	6, 3	$V_{\varphi Ref}$	1.06	1.13	1.18	V
Temperature coefficient		6	$TC_{V\varphi Ref}$		0.5		mV/K
Pulse Output (see Figure 10-12 on page 19, Pin 4)							
Output pulse current	R_{GT} = 0, V_{GT} = 1.2V		I_o	100	155	190	mA
Reverse current			I_{or}		0.01	3.0	µA
Output pulse width	Cφ = 10nF		t_p		80		µs
Amplifier							
Common-mode signal range		10, 11	V_{10}, V_{11}	V_{16}		–1	V
Input bias current		11	I_{IO}		0.01	1	µA
Input offset voltage		10, 11	V_{10}		10		mV
Output current		12	$-I_O$ $+I_O$	75 88	110 120	145 165	µA µA
Short circuit forward, transmittance	$I_{12} = f(V_{10-11})$, (see Figure 10-7 on page 18)	12	Y_f		1000		µA/V

Note: 1. The pins refer to the DIP18 package version which is no longer available.

10. Electrical Characteristics (Continued)

$-V_S$ = 13.0V, T_{amb} = 25°C, reference point pin 2, unless otherwise specified

Parameters	Test Conditions	Pins [1]	Symbol	Min.	Typ.	Max.	Unit
Pulse Blocking, Tacho Monitoring							
Logic-on		18	$-V_{TON}$	3.7	1.5		V
Logic-off		18	$-V_{TOFF}$		1.25	1.0	V
Input current	$V_{18} = V_{TOFF} = 1.25V$ $V_{18} = V_{16}$	18	I_I	 14.5	0.3	1	µA µA
Output resistance		18	R_O	1.5	6	10	kΩ
Frequency-to-voltage Converter							
Input bias current		8	I_{IB}		0.6	2	µA
Input voltage limitation	$I_I = -1mA$ $I_I = +1mA$ (see Figure 10-7 on page 18)	8	$-V_I$ $+V_I$	660 7.25		750 8.05	mV V
Turn-on threshold		8	$-V_{TON}$		100	150	mV
Turn-off threshold		8	$-V_{TOFF}$	20	50		mV
Charge Amplifier							
Discharge current	C_5 = 1nF, (see Figure 10-17 on page 22)	9	I_{dis}		0.5		mA
Charge transfer voltage		9 to 16	V_{ch}	6.50	6.70	6.90	V
Charge transfer gain	I_{10}/I_9	9, 10	G_i	7.5	8.3	9.0	
Conversion factor	C_5 = 1nF, R_6 = 100kΩ (see Figure 10-17 on page 22)		K		5.5		mV/Hz
Output operating range		10 to 16	V_O		0-6		V
Linearity					±1		%
Soft Start, f/V Converter Non-active (see Figure 10-2 on page 16 and Figure 10-4 on page 17)							
Starting current	$V_{13} = V_{16}$, $V_8 = V_2$	13	I_O	20	45	55	µA
Final current	V_{13} = 0.5	13	I_O	50	85	130	µA
f/V Converter Active (see Figure 10-3 on page 16, Figure 10-5 on page 17 and Figure 10-6 on page 17)							
Starting current	$V_{13} = V_{16}$	13	I_O	2	4	7	µA
Final current	V_{13} = 0.5		I_O	30	55	80	µA
Discharge current	Restart pulse	13	I_O	0.5	3	10	mA
Automatic Retriggering (see Figure 10-13 on page 20, Pin 5)							
Repetition rate	R_{5-3} = 0		t_{pp}	3	4.5	6	t_p
	R_{5-3} = 15kΩ		t_{pp}		20		t_p
Load Limiting (see Figure 10-9 on page 18, Figure 10-10 on page 19 and Figure 10-11 on page 19)							
Operating voltage range		14	V_I	–1.0		+1.0	V
Offset current	$V_{10} = V_{16}$ $V_{14} = V_2$ via 1kΩ	14 15-16	I_O I_O	5	 0.1	12 1.0	µA µA
Input current	V_{10} = 4.5V	14	I_I	60	90	120	µA
Output current	V_{14} = 300mV	15-16	I_O	110		140	µA
Overload ON		15-16	V_{TON}	7.05	7.4	7.7	V

Note: 1. The pins refer to the DIP18 package version which is no longer available.

Figure 10-1. Ramp Control

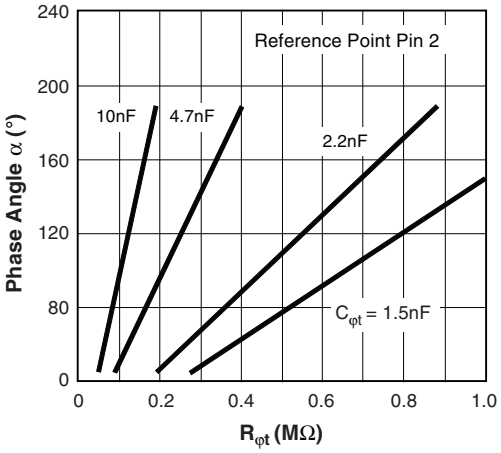


Figure 10-2. Soft-start Charge Current (f/V Converter Non-active)

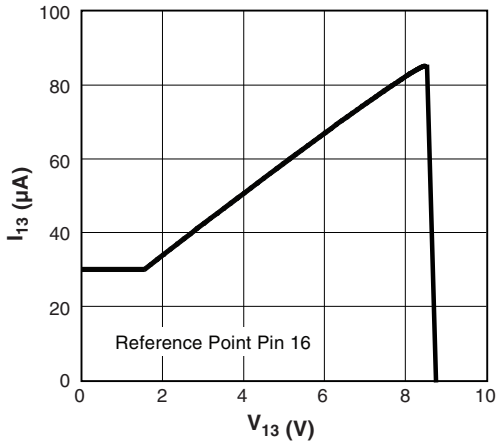


Figure 10-3. Soft-start Charge Current (f/V Converter Active)

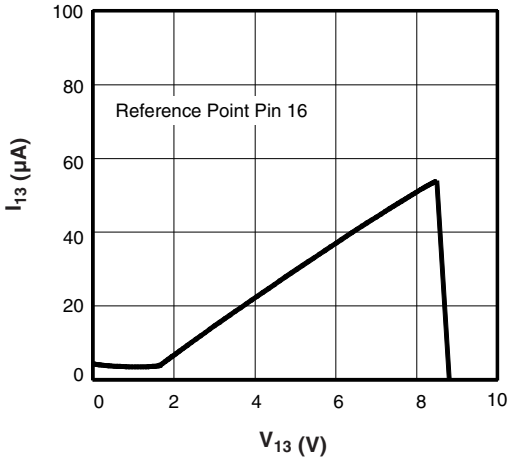


Figure 10-4. Soft-start Voltage (f/V Converter Non-active)

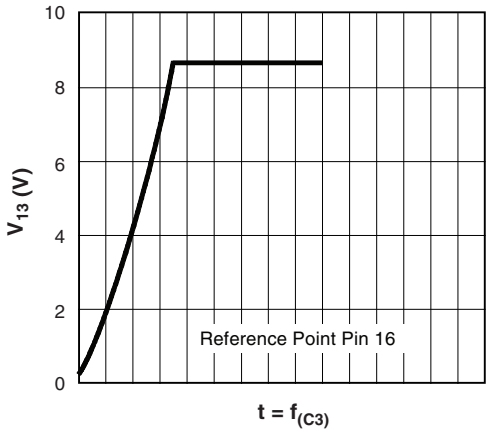


Figure 10-5. Soft-start Voltage (f/V Converter Active)

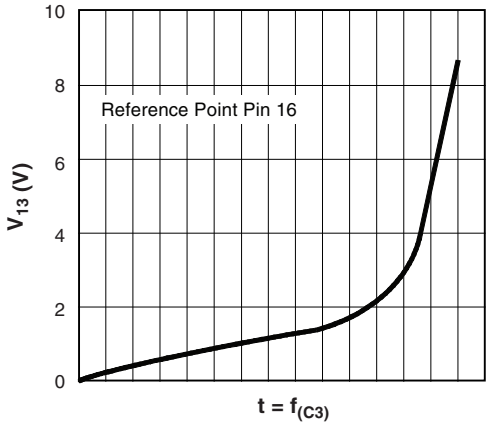


Figure 10-6. Soft-start Function

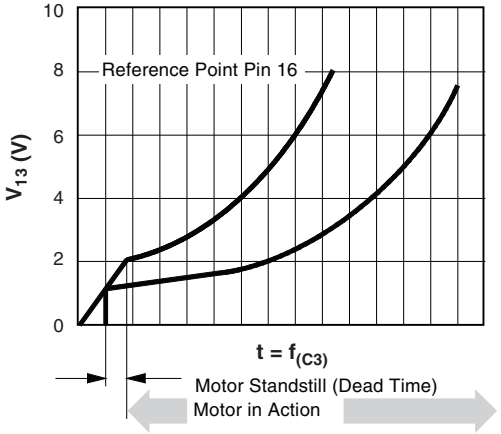


Figure 10-7. f/V Converter Voltage Limitation

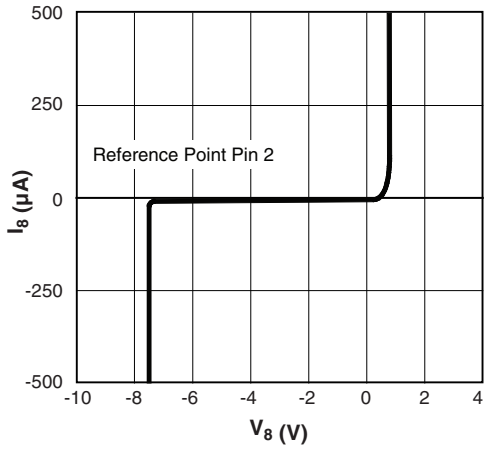


Figure 10-8. Amplifier Output Characteristics

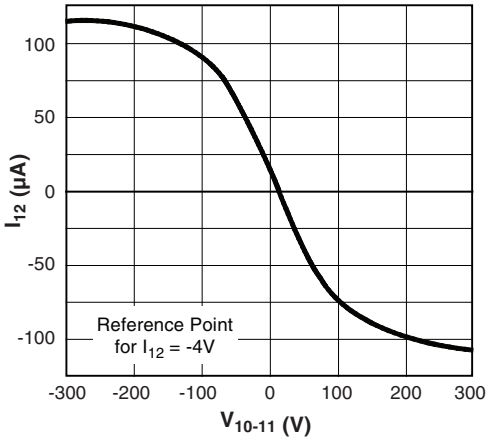


Figure 10-9. Load Limit Control

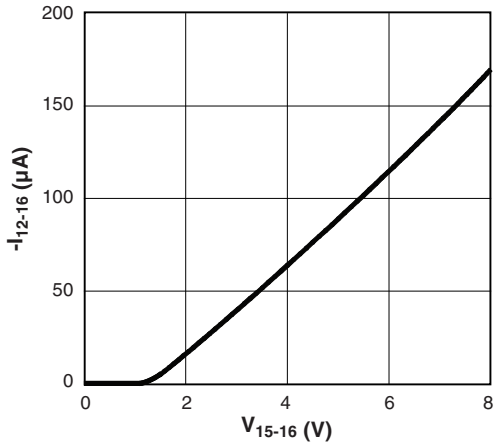


Figure 10-10. Load Limit Control f/V Dependency

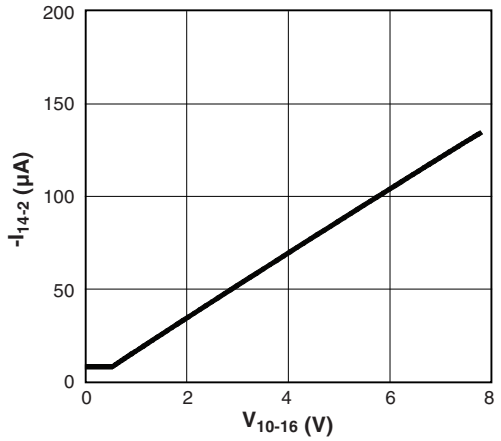


Figure 10-11. Load Current Detection

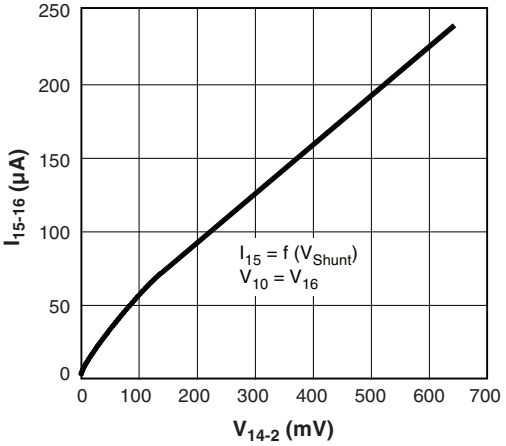


Figure 10-12. Pulse Output

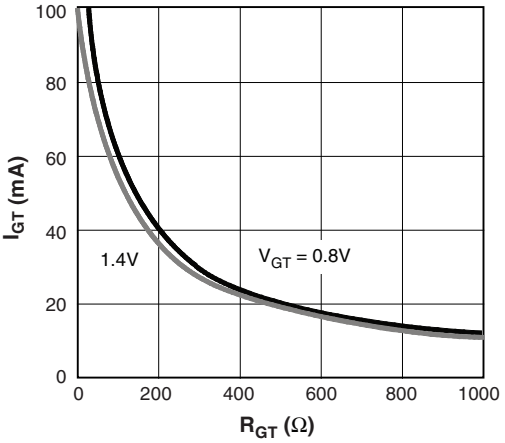


Figure 10-13. Automatic Retriggering Repetition Rate

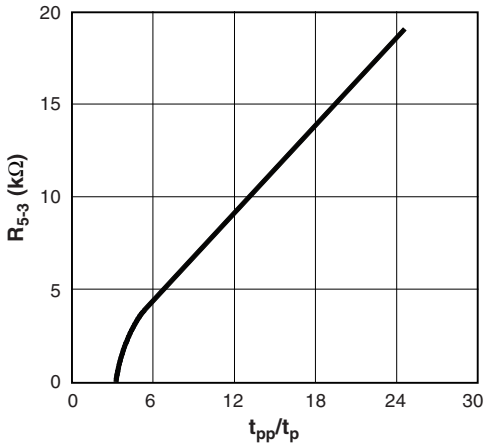


Figure 10-14. Determination of R_1

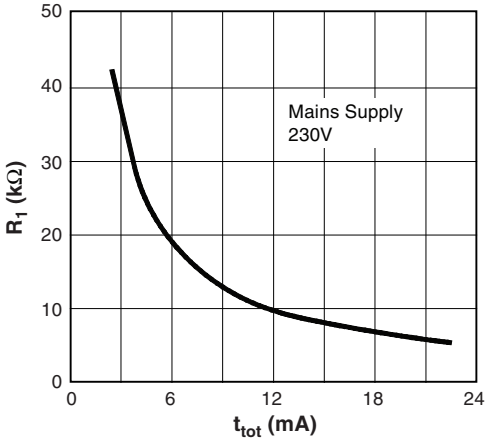


Figure 10-15. Power Dissipation of R_1

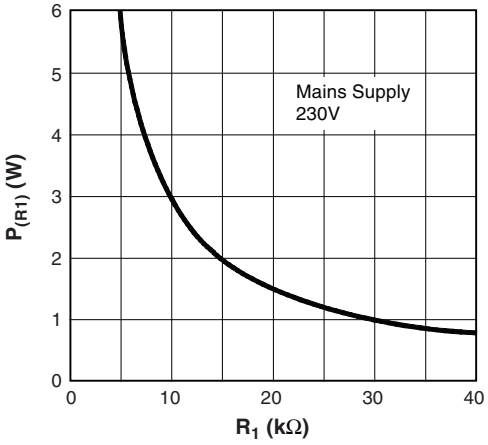


Figure 10-16. Power Dissipation of R_1 According to Current Consumption

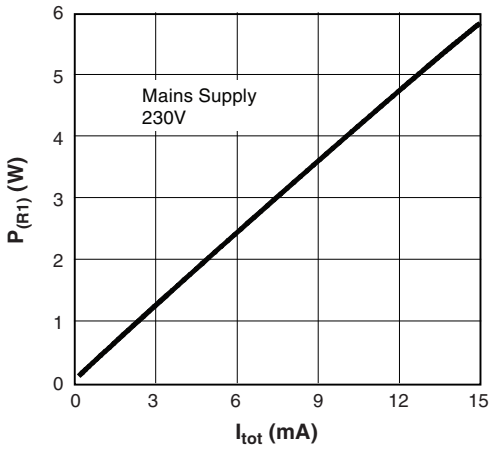
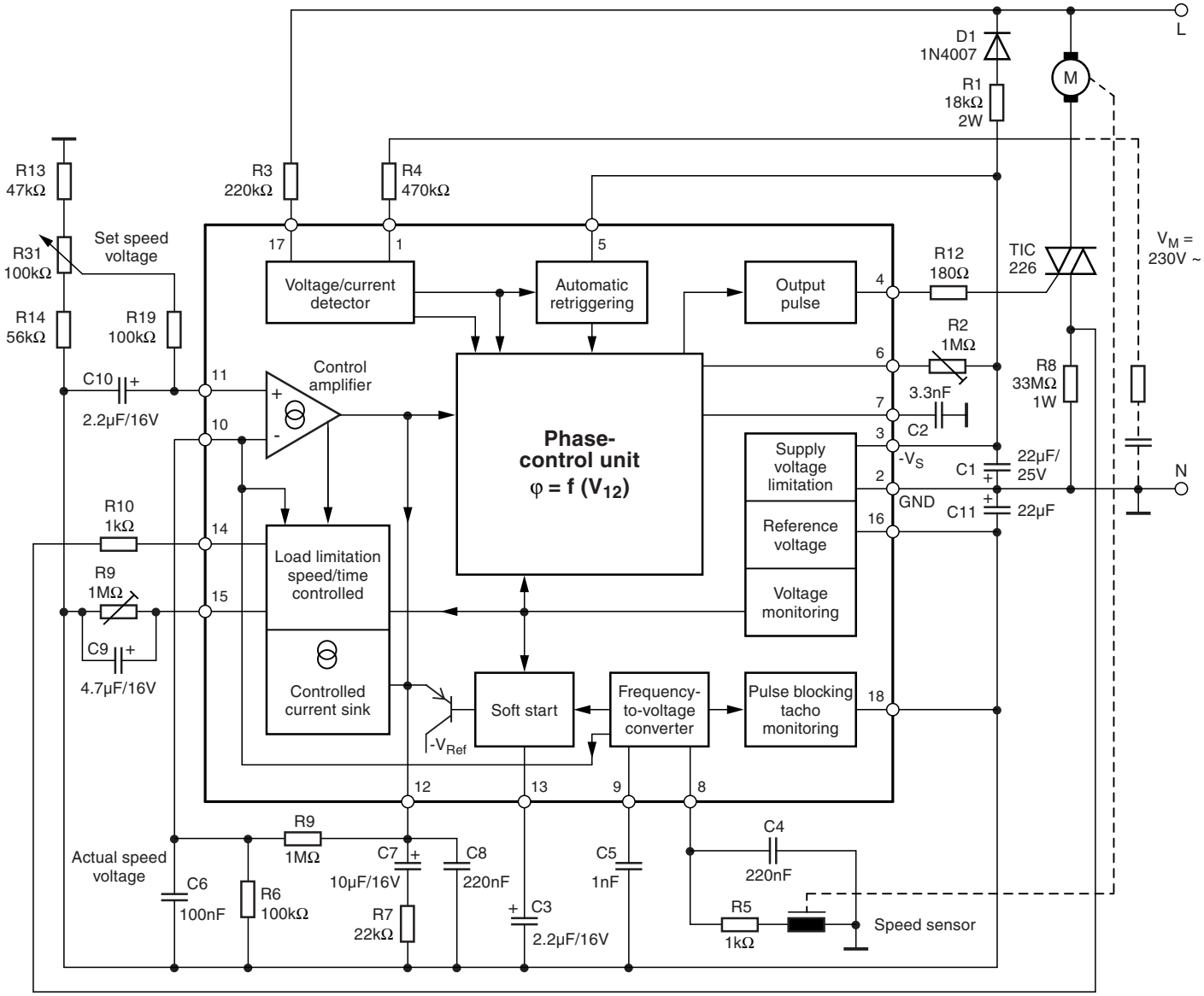
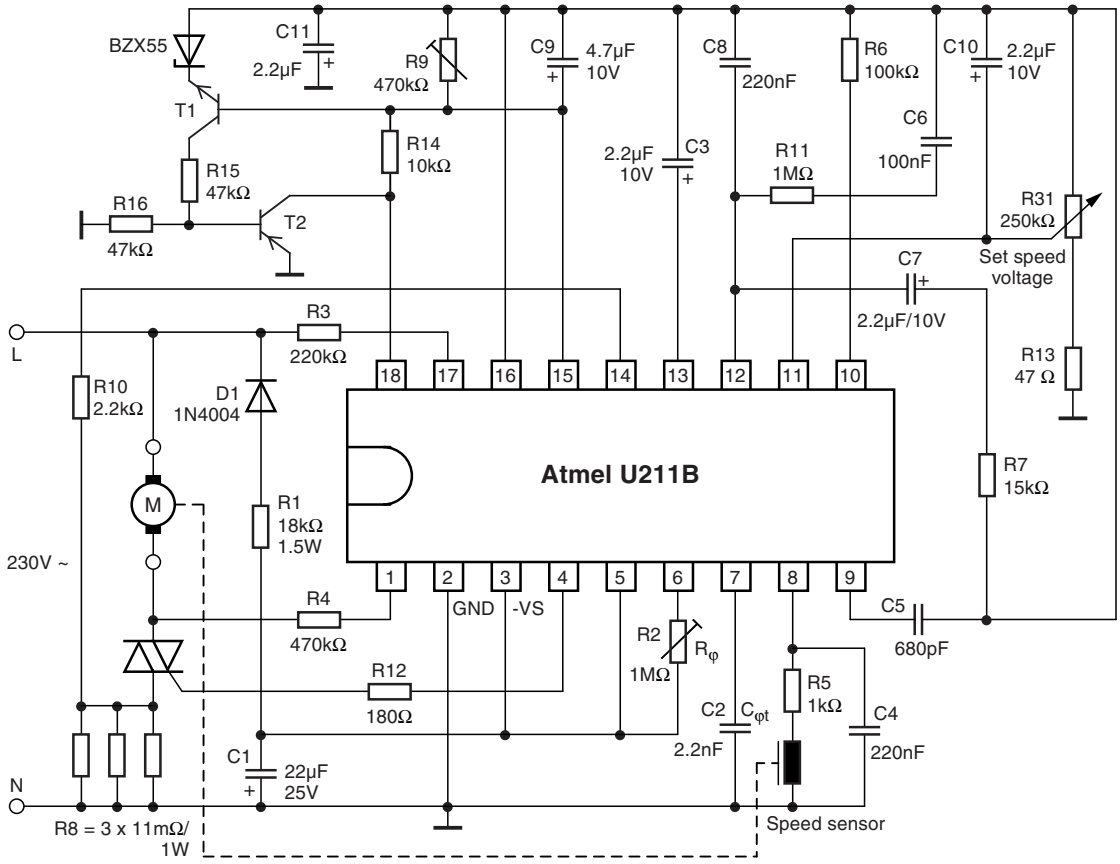


Figure 10-17. Speed Control, Automatic Retriggering, Load Limiting, Soft Start



Note: 1. The schematic refers to the DIP18 package version which is no longer available.

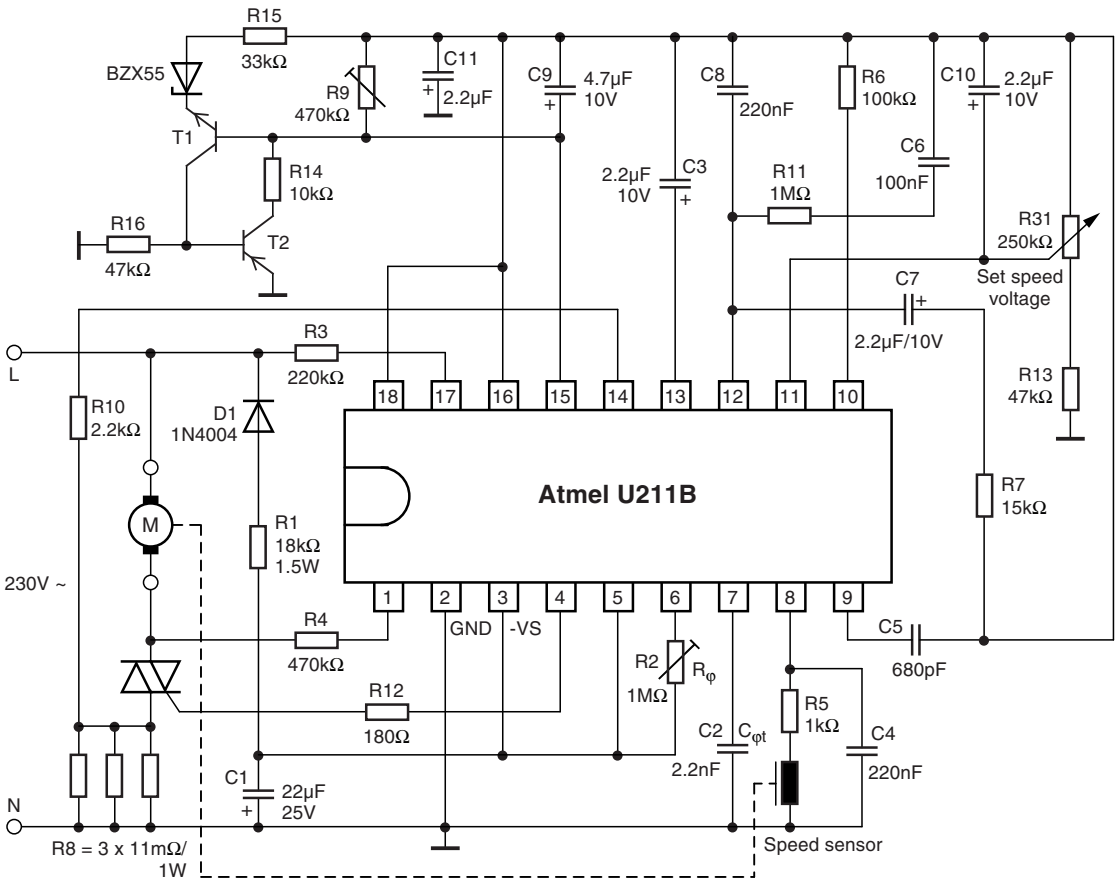
Figure 10-18. Speed Control, Automatic Retriggering, Load Switch-off, Soft Start



The switch-off level at maximum load shows in principle the same speed dependency as the original version (see Figure 10-17 on page 22), but when reaching the maximum load, the motor is switched off completely. This function is effected by the thyristor (formed by T_1 and T_2) which ignites when the voltage at pin 15 reaches typically 7.4V (reference point pin 16). The circuit is thereby switched to standby mode over the release Pin 18.

Note: 1. The schematic refers to the DIP18 package version which is no longer available.

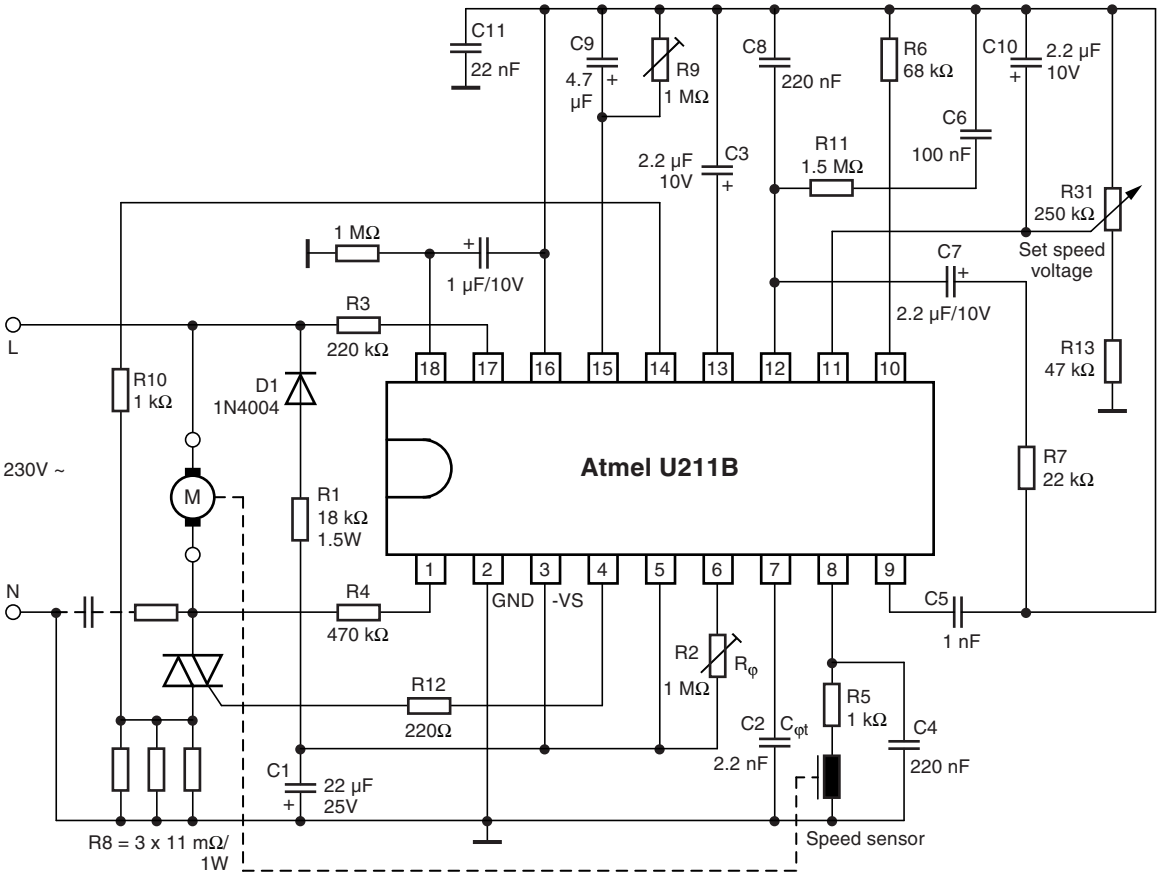
Figure 10-19. Speed Control, Automatic Retriggering, Load Switch-down, Soft Start



The maximum load regulation shows in principle the same speed dependency as the original version (see Figure 10-17 on page 22). When reaching the maximum load, the control unit is turned to α_{max}, adjustable with R_2. Then, only I_O flows. This function is effected by the thyristor, formed by T_1 and T_2 which ignites as soon as the voltage at pin 15 reaches approximately 6.8V (reference point pin 16). The potential at pin 15 is lifted and kept by R_{14} over the internal operating threshold whereby the maximum load regulation starts and adjusts the control unit constantly to α_{max} (I_O), inspite of a reduced load current. The motor shows that the circuit is still in operation by produceing a buzzing sound.

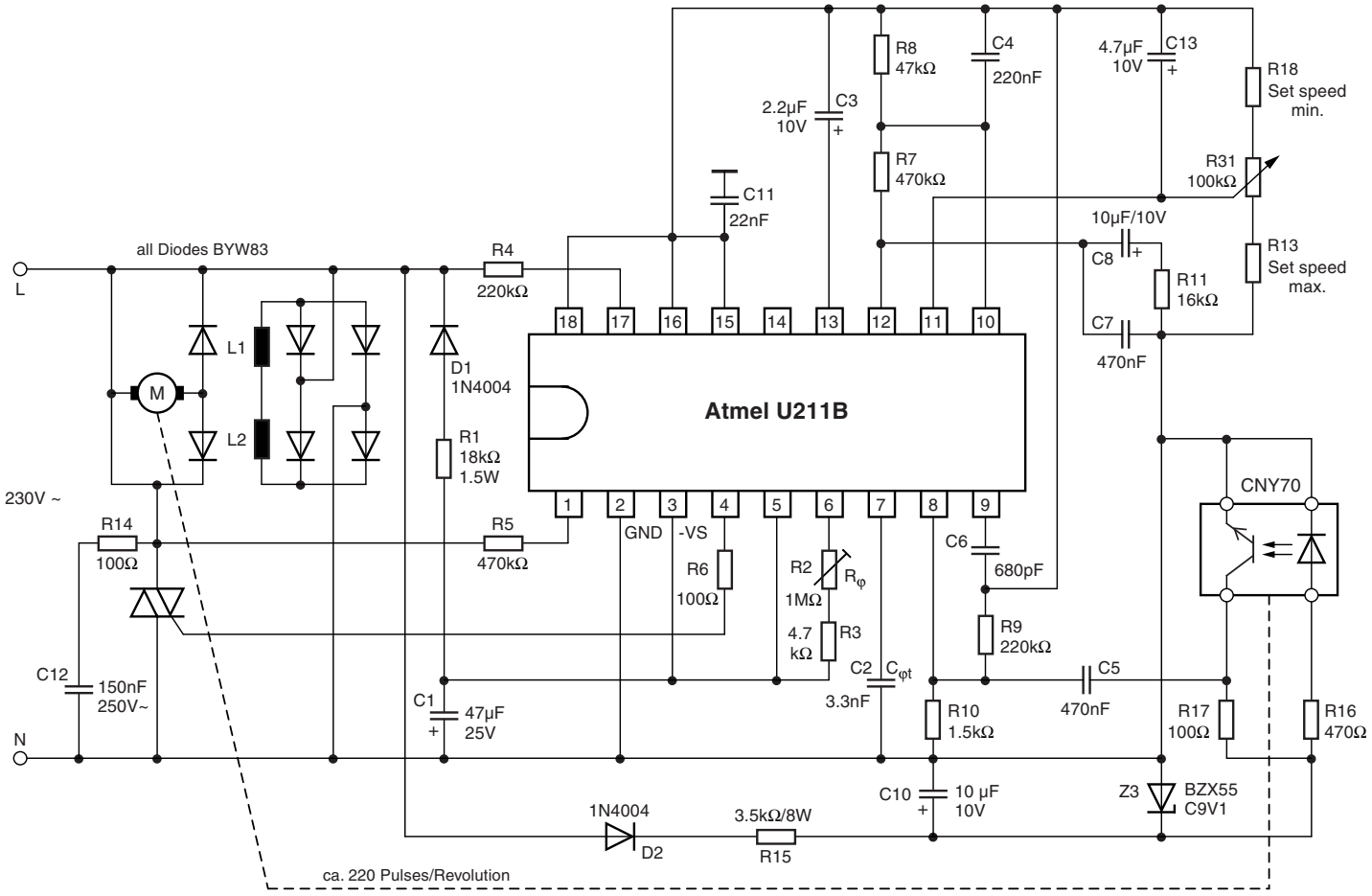
Note: 1. The schematic refers to the DIP18 package version which is no longer available.

Figure 10-20. Speed Control, Automatic Retriggering, Load Limiting, Soft Start, Tacho Control



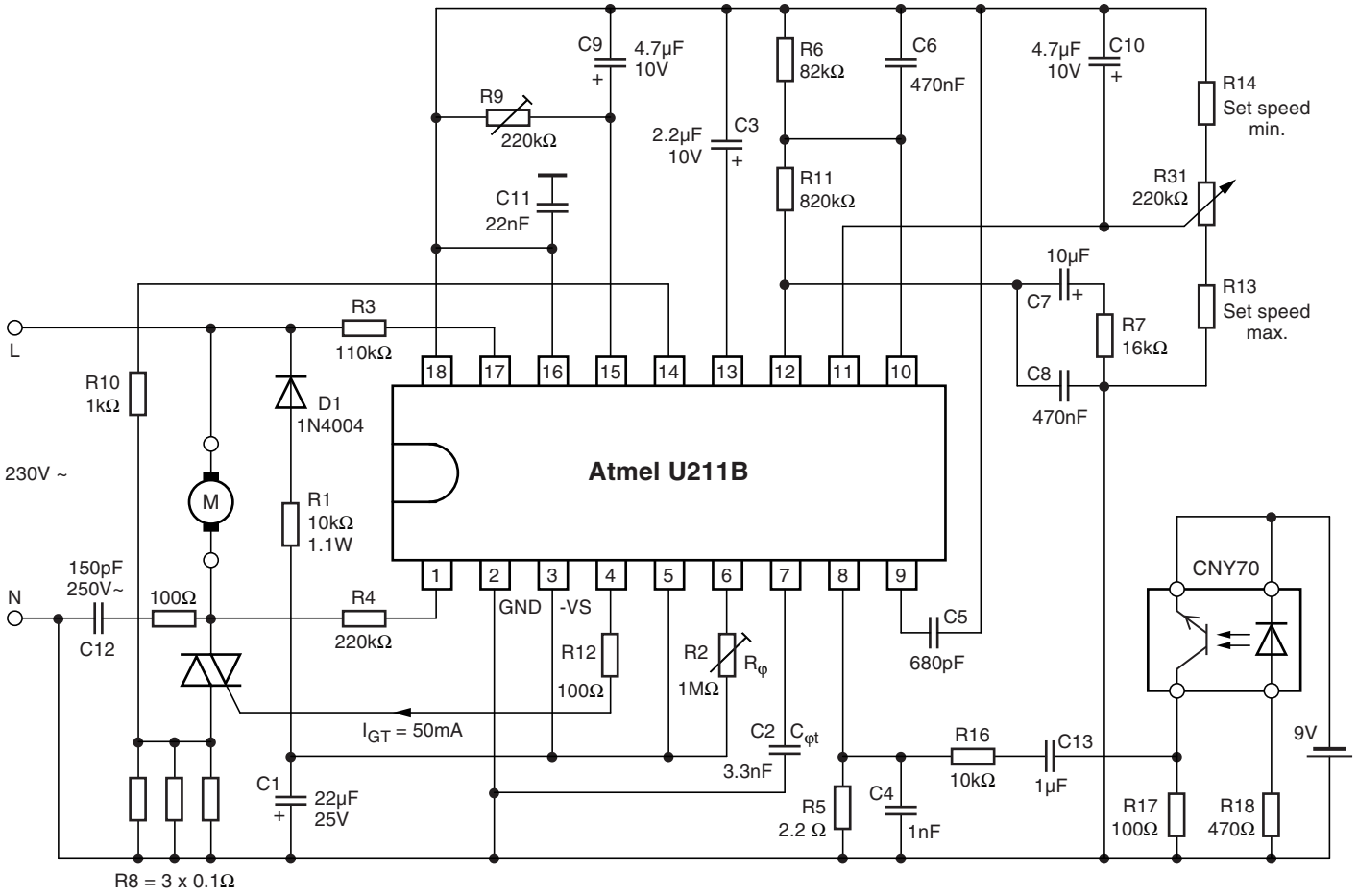
Note: 1. The schematic refers to the DIP18 package version which is no longer available.

Figure 10-21. Speed Control with Reflective Opto Coupler CNY70 as Emitter



Note: 1. The schematic refers to the DIP18 package version which is no longer available.

Figure 10-22. Speed Control, Maximum Load Control with Reflective Opto Coupler CNY70 as Emitter



The schematic diagram (see Figure 10-22 on page 27) is designed as a speed control IC based on the reflection-coupled principle with 4 periods per revolution and a maximum speed of 30000rpm. The separation of the coupler from the rotating aperture should be about approximately 1mm. In the schematic diagram, the power supply for the coupler was provided externally because of the relatively high current consumption.

Instructions for adjusting:

1. In the initial adjustment of the phase-control circuit, R_2 should be adjusted so that when $R_{14} = 0$ and R_{31} are in minimum position, the motor just turns.
2. The speed can now be adjusted as desired by means of R_{31} between the limits determined by R_{13} and R_{14}.
3. The switch-off power of the limiting-load control can be set by R_9. The lower R_9, the higher the switch-off power.

Note: 1. The schematic refers to the DIP18 package version which is no longer available.

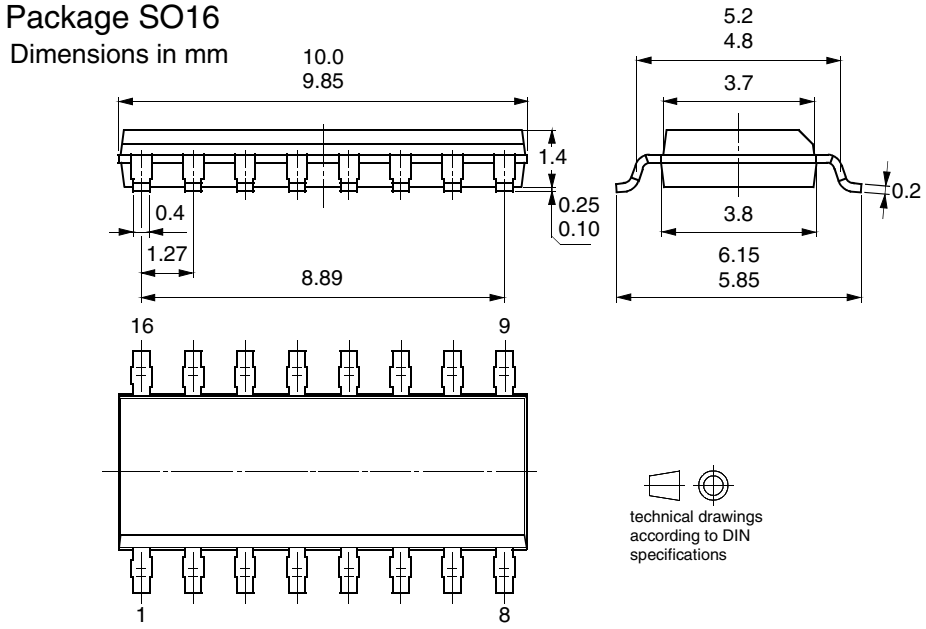
11. Ordering Information

Extended Type Number	Package	Remarks
U211B-xFPY	SO16	Tube
U211B-xFPG3Y	SO16	Taped and reeled

12. Package Information

Package SO16

Dimensions in mm



13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4752C-INDCO-10/11	• Put datasheet in newest template • DIP18 package is no longer available: Comments added and some changes made
4752B-INDCO-09/05	• Put datasheet in a new template • First page: Pb-free logo added • Page 27: Ordering Information changed

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1)(408) 441-0311
Fax: (+1)(408) 487-2600

Atmel Asia Limited
Unit 01-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
JAPAN
Tel: (+81) (3) 3523-3551
Fax: (+81) (3) 3523-7581