

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS -H)

TK100E10NE

■ E-Bike/UPS/Inverter

Note : This product is designed for E-Bike / UPS / Inverter in China / India market.

- Low drain-source on-resistance : $R_{DS(ON)} = 4.3 \text{ m}\Omega$ (typ.)
- Low leakage current : $I_{DSS} = 10 \text{ }\mu\text{A}$ (max) ($V_{DS} = 100 \text{ V}$)
- Enhancement mode : $V_{th} = 2.0 \sim 4.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

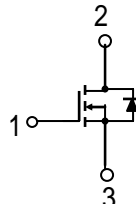
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	100	A
	DC (Note 1,4)	I_D	90	A
	Pulse (Note 1)	I_{DP}	670	A
Drain power dissipation ($T_c = 25^\circ\text{C}$)		P_D	230	W
Single pulse avalanche energy (Note 2)		E_{AS}	65	mJ
Avalanche current		I_{AR}	50	A
Repetitive avalanche energy (Note 3)		E_{AR}	23	mJ
Peak diode recovery dv/dt (Note 5)		dv/dt	12	V/ns
Channel temperature (Note 4)		T_{ch}	175	$^\circ\text{C}$
Storage temperature range (Note 4)		T_{stg}	$-55 \sim 175$	$^\circ\text{C}$

Thermal Characteristics

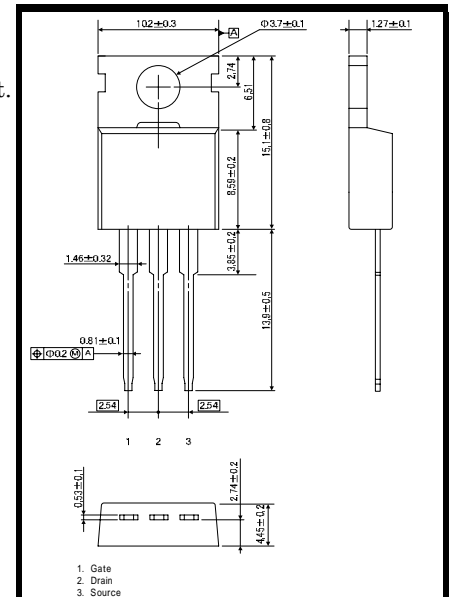
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	0.65	$^\circ\text{C/W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	$^\circ\text{C/W}$

Note 1: Ensure that the channel temperature does not exceed 175°C .Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 42 \text{ }\mu\text{H}$, $R_G = 25 \text{ }\Omega$, $I_{AR} = 50 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: $T_c = 100^\circ\text{C}$ Note 5: $I_{DR} = 80 \text{ A}$, $di/dt = 160 \text{ A}/\mu\text{s}$, $T_{ch} = T_{ch \text{ max.}}$,
 $V_{DS \text{ peak}} < V_{DSS}$ This transistor is an electrostatic-sensitive device.
Please handle with caution.

Unit: mm



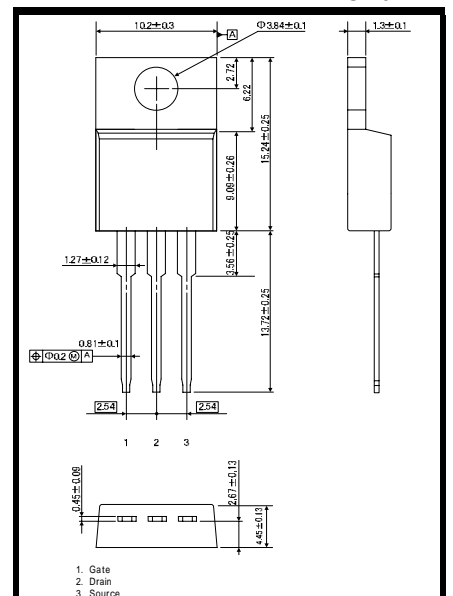
JEDEC TO-220AB

JEITA SC-46

TOSHIBA -

Weight: 1.9 g (typ.)

Unit: mm



JEDEC TO-220AB

JEITA SC-46

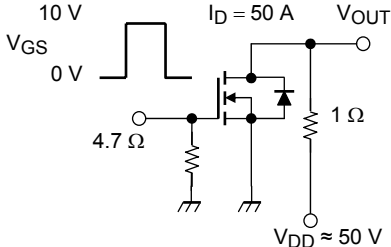
TOSHIBA -

Weight: 1.9 g (typ.)

Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.). Thermal Characteristics

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V	—	—	±0.1	μA
Drain cut-off current		I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage	V _(BR) DSS	I _D = 10 mA, V _{GS} = 0 V		100	—	—	V
	V _(BR) DSX	I _D = 10 mA, V _{GS} = -20 V(Note 5)		65	—	—	V
Gate threshold voltage		V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance		R _{DS (ON)}	V _{GS} = 10 V, I _D = 50 A	—	4.3	5.1	mΩ
Input capacitance		C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	—	5590	—	pF
Reverse transfer capacitance		C _{rss}		—	350	—	
Output capacitance		C _{oss}		—	2680	—	
Switching time	Rise time	t _r		—	18	—	ns
	Turn-on time	t _{on}		—	44	—	
	Fall time	t _f		—	27	—	
	Turn-off time	t _{off}		—	86	—	
Total gate charge (Gate-source plus gate-drain)		Q _g	V _{DD} ≈ 80 V, V _{GS} = 10 V, I _D = 100 A	—	83	—	nC
Gate-source charge		Q _{gs}		—	63	—	
Gate-drain (“miller”) charge		Q _{gd}		—	20	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

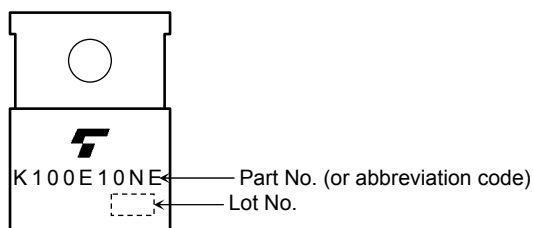
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	—	—	—	100	A
Pulse drain reverse current (Note 1)	I _{DRP}	—	—	—	670	A
Forward voltage (diode)	V _{DSF}	I _{DR} = 100 A, V _{GS} = 0 V	—	—	-1.5	V
Reverse recovery time (Note 6)	t _{rr}	I _{DR} = 100 A, V _{GS} = 0 V	—	88	—	ns
Reverse recovery charge (Note 6)	Q _{rr}	dI _{DR} /dt = 50 A/μs	—	93	—	nC

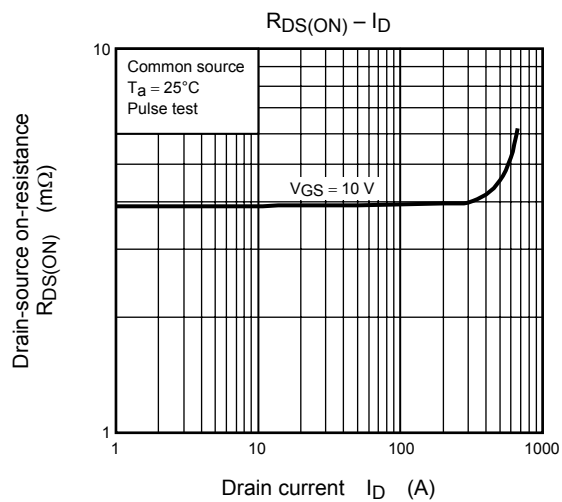
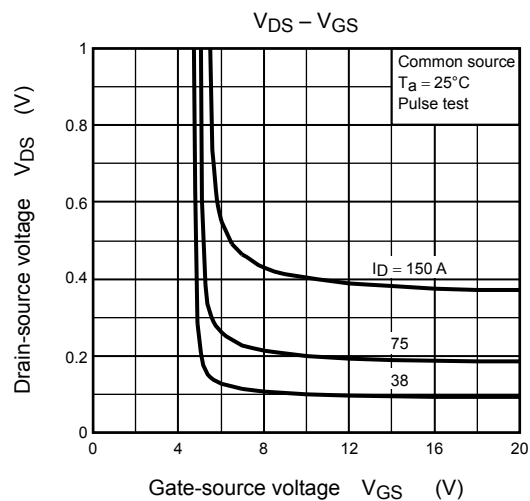
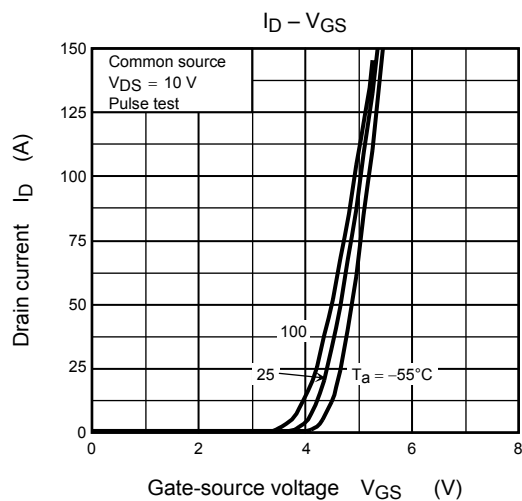
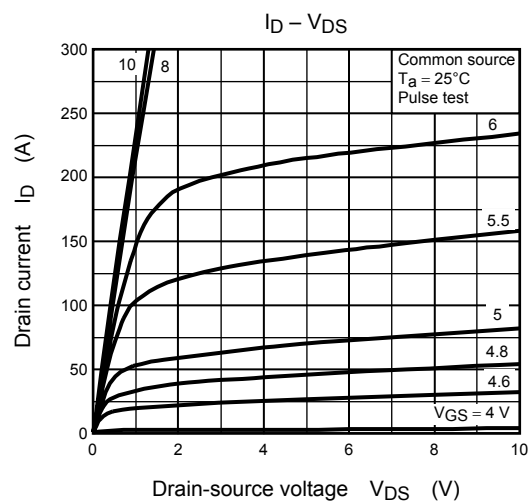
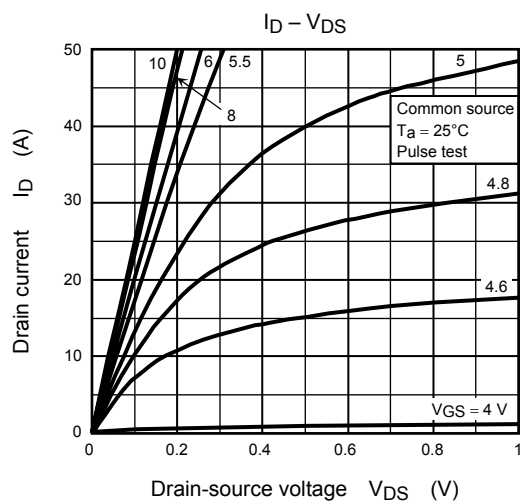
Note 5: If a reverse bias is applied between gate and source, this device enters V_(BR)DSX mode.

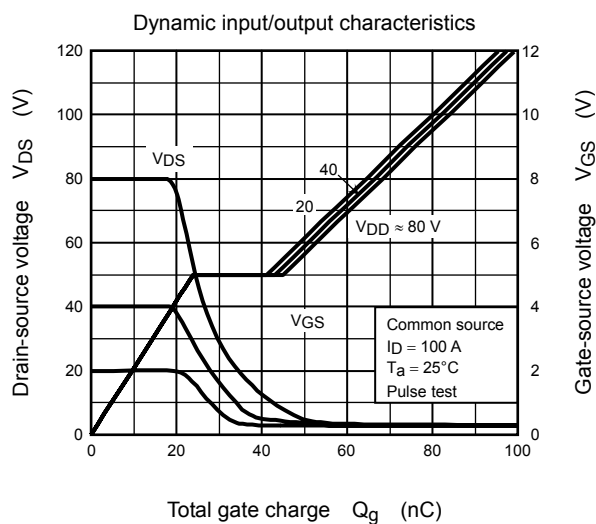
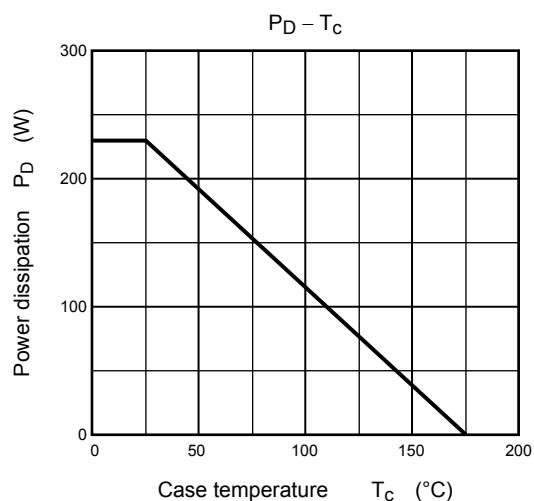
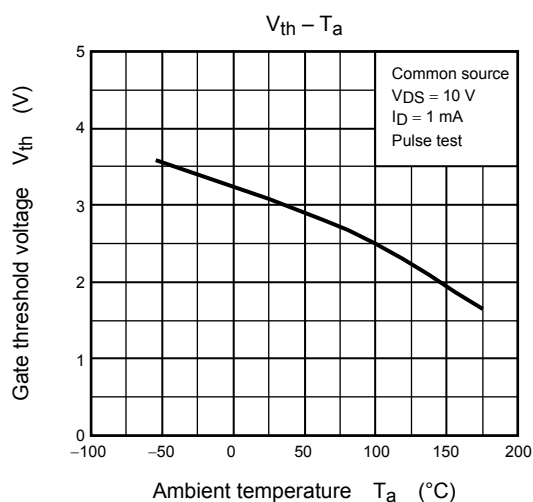
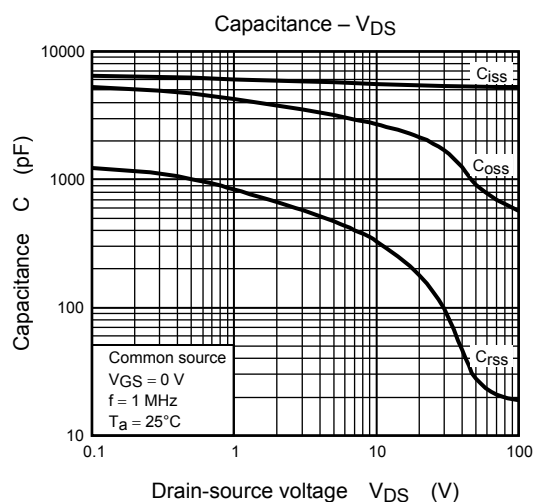
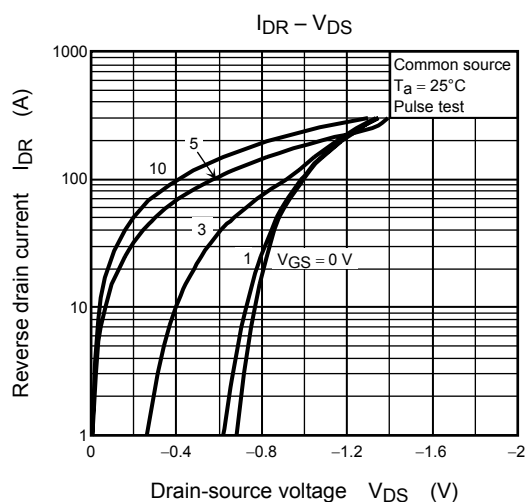
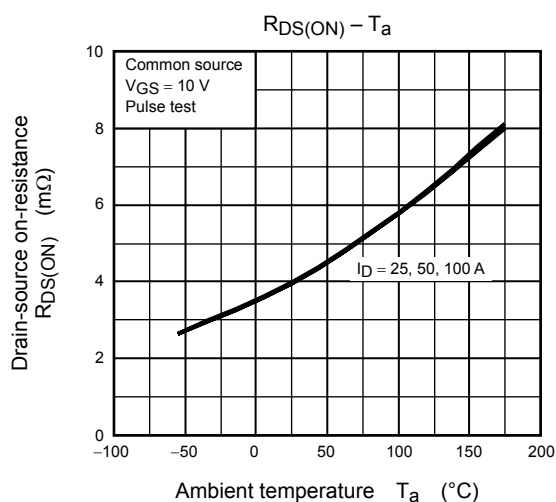
Note that the drain-source breakdown voltage is lowered in this mode.

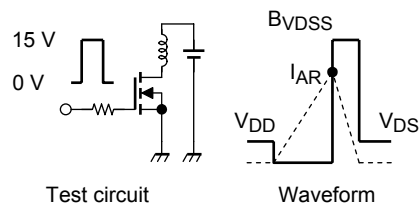
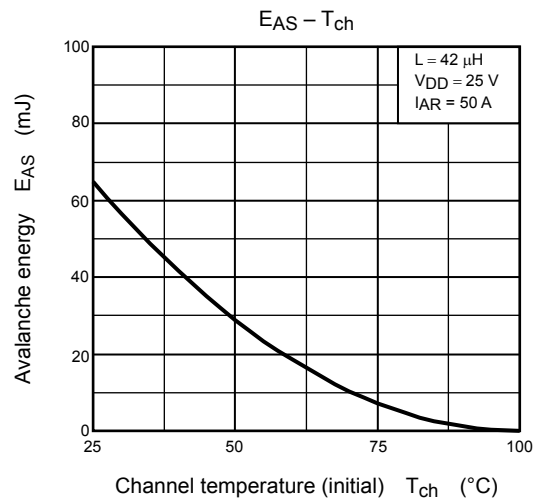
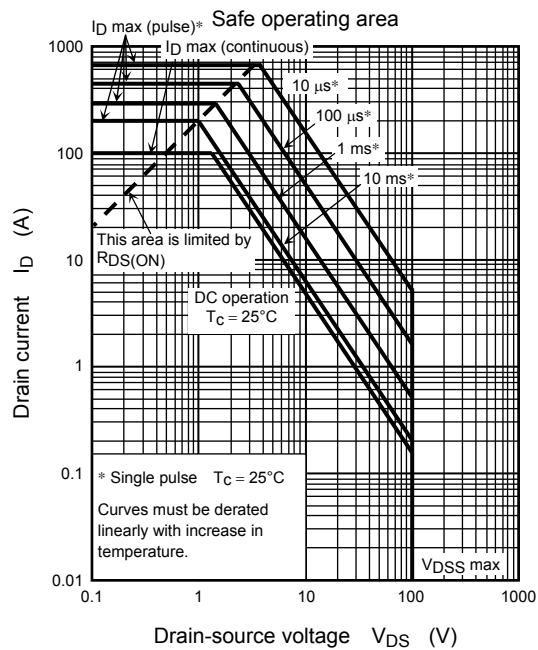
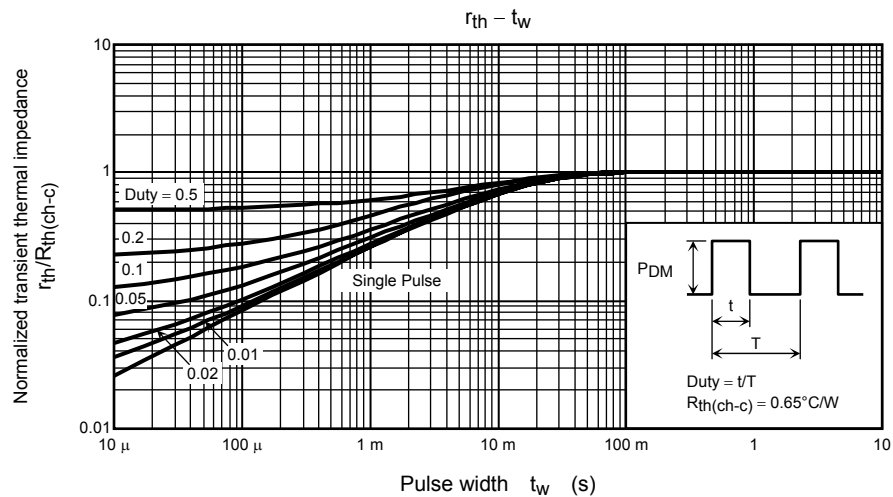
Note 6: Ensure that V_{DS} peak does not exceed V_{DSS}.

Marking









$$R_G = 25 \Omega$$

$$V_{DD} = 25 \text{ V}, L = 42 \mu\text{H}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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