Pin Out (top view)

TOP VIEW

	1	2	3	4	5	6	7	8	9	
A	TA1+	TB1+	TC1+	TCLK1+	TD1+	TA2+	TB2+	TC2+	TCLK2+	A
B	TA1-	TB1-	TC1-	TCLK1-	TD1-	TA2-	TB2-	TC2-	TCLK2-	B
C	PRBS	N/C	Reserved1	GND	LVDS VCC	GND	PLL VCC	TD2-	TD2+	C
D	R11	R10	LVDS VCC				GND	/PDWN	O/E	D
E	R13	R12	GND				MODE	MAP	DDRN	E
F	R15	R14	GND				6B/8B	RS	CLKIN	F
G	R17	R16	VCC	GND	VCC	GND	IOVCC	R/F	DE	G
H	G10	G12	G14	G16	B10	B12	B14	B16	VSYNC	H
J	G11	G13	G15	G17	B11	B13	B15	B17	HSYNC	J
	1	2	3	4	5	6	7	8	9	

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>TA1+, TA1-</td><td>A1,B1</td><td rowspan="4">LVDS OUT</td><td rowspan="4">The 1st Link.
The 1st pixel output data when Dual out.
Output data when Single out.</td></tr>
<tr><td>TB1+, TB1-</td><td>A2,B2</td></tr>
<tr><td>TC1+, TC1-</td><td>A3,B3</td></tr>
<tr><td>TD1+, TD1-</td><td>A5,B5</td></tr>
<tr><td>TCLK1+, TCLK1-</td><td>A4,B4</td><td>LVDS OUT</td><td>LVDS Clock Out for 1st Link.</td></tr>
<tr><td>TA2+, TA2-</td><td>A6,B6</td><td rowspan="4">LVDS OUT</td><td rowspan="4">The 2nd Link.
The 2nd pixel output data when Dual out.</td></tr>
<tr><td>TB2+, TB2-</td><td>A7,B7</td></tr>
<tr><td>TC2+, TC2-</td><td>A8,B8</td></tr>
<tr><td>TD2+, TD2-</td><td>C9,C8</td></tr>
<tr><td>TCLK2+, TCLK2-</td><td>A9,B9</td><td>LVDS OUT</td><td>LVDS Clock Out for 2nd Link.</td></tr>
<tr><td>R17 ~ R10</td><td>G1,G2,F1,F2
E1,E2,D1,D2</td><td rowspan="3">IN</td><td rowspan="3">Pixel Data Inputs.</td></tr>
<tr><td>G17 ~ G10</td><td>J4,H4,J3,H3
J2,H2,J1,H1</td></tr>
<tr><td>B17 ~ B10</td><td>J8,H8,J7,H7
J6,H6,J5,H5</td></tr>
<tr><td>DE</td><td>G9</td><td>IN</td><td>Data Enable Input.</td></tr>
<tr><td>VSYNC</td><td>H9</td><td>IN</td><td>Vsync Input.</td></tr>
<tr><td>HSYNC</td><td>J9</td><td>IN</td><td>Hsync Input.</td></tr>
<tr><td>CLKIN</td><td>F9</td><td>IN</td><td>Clock Input.</td></tr>
<tr><td>R/F</td><td>G8</td><td>IN</td><td>Input Clock Triggering Edge Select.
H: Rising edge, L: Falling edge</td></tr>
<tr><td>RS</td><td>F8</td><td>IN</td><td>LVDS swing mode select.
<table>
<tr><th>RS</th><th>LVDS Swing (VOD, see Fig4 and Fig5)</th></tr>
<tr><td>H</td><td>350mV</td></tr>
<tr><td>L</td><td>200mV</td></tr>
</table></td></tr>
<tr><td>MAP</td><td>E8</td><td>IN</td><td>LVDS mapping table select. See Fig9 and Fig10.
<table>
<tr><th>MAP</th><th>Mapping Mode</th></tr>
<tr><td>H</td><td>Mapping MODE1</td></tr>
<tr><td>L</td><td>Mapping MODE2</td></tr>
</table></td></tr>
<tr><td>MODE</td><td>E7</td><td>IN</td><td>Pixel data mode. See Fig7 and Fig8.
<table>
<tr><th>MODE</th><th>Modes</th></tr>
<tr><td>H</td><td>Single out (Single-in/Single-out)</td></tr>
<tr><td>L</td><td>Dual out (Single-in/Dual-out)</td></tr>
</table></td></tr>
<tr><td>O/E</td><td>D9</td><td>IN</td><td>Output enable.
H: Output enable,
L: Output disable (all outputs are Hi-Z).</td></tr>
<tr><td>/PDWN</td><td>D8</td><td>IN</td><td>H: Normal operation,
L: Power down (all outputs are Hi-Z and all circuits are stand-by mode with minimum current (ITCCS)).</td></tr>
<tr><td>PRBS [a]</td><td>C1</td><td>IN</td><td>Must be tied to GND.</td></tr>
</table>

Pin Description (Continued)

Pin Name	Pin #	Type	Description
Reserved1	C3	IN	Must be tied to GND.
6B/8B	F7	IN	6bit / 8bit mode select. H: 6bit mode (21bit mode), L: 8bit mode (27bit mode).
DDRN	E9	IN	DDR function is active when MODE = L (Dual-out mode). H: DDR (Double Edge input) function disable (Fig4). L: DDR (Double Edge input) function enable (Fig5).
N/C	C2		Must be Open.
VCC	G3,G5	Power	Power Supply Pins for digital circuitry.
IOVCC	G7	Power	Power Supply Pin for IO inputs circuitry.
LVDSVCC	C5,D3	Power	Power Supply Pins for LVDS Outputs.
PLLVCC	C7	Power	Power Supply Pin for PLL circuitry.
GND	F3,G4,G6,C4, E3,C6,D7	Ground	Ground Pins.

a: Setting the PRBS pin high enables the internal test pattern generator. It generates Pseudo-Random Bit Sequence of 2^{23}-1.
The generated PRBS is fed into input data latches, encoded and serialized into LVDS OUT.
This function is normally to be used for analyzing the signal integrity of the transmission channel including PCB traces, connectors, and cables.

Absolute Maximum Ratings

Supply Voltage (IOVCC)	-0.3V ~ +4.0V
Supply Voltage (VCC, PLLVCC, LVDSVCC)	-0.3V ~ +2.1V
CMOS/TTL Input Voltage	-0.3V ~ (IOVCC+ 0.3V)
LVDS Transmitter Output Voltage	-0.3V ~ (LVDSVCC + 0.3V)
Output Current	-50mA ~ 50mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	1.3W

Recommended Operating Conditions

Parameter				**Min**	**Typ**	**Max**	**Units**
Supply Voltage (IOVCC)				1.62	1.8 / 2.5 / 3.3	3.6	V
Supply Voltage (PLLVCC / LVDSVCC / VCC)				1.62	1.8	1.98	V
Operating Ambient Temperature (Ta)				-40		85	°C
Clock Frequency	MODE=L Dual-out	Single Edge Input (DDRN=H)	Input	20		174	MHz
			LVDS Output	10		87	MHz
		Double Edge Input (DDRN=L)	Input	10		174	MHz
			LVDS Output	10		174	MHz
	MODE=H Single-out		Input	10		174	MHz
			LVDS Output	10		174	MHz

Electrical Characteristics

CMOS/TTL (Pin type “**IN**”) DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH18}	High Level Data Input Voltage	IOVCC=1.62V~1.98V	0.65 IOVCC		IOVCC+0.3	V
V_{IL18}	Low Level Data Input Voltage		-0.3		0.35 IOVCC	V
V_{IH25}	High Level Data Input Voltage	IOVCC=2.3V~2.7V	1.7		IOVCC+0.3	V
V_{IL25}	Low Level Data Input Voltage		-0.3		0.7	V
V_{IH33}	High Level Data Input Voltage	IOVCC=3.0V~3.6V	2.0		IOVCC+0.3	V
V_{IL33}	Low Level Data Input Voltage		-0.3		0.8	V
I_{INC}	Input Current	VIN=GND~IOVCC	-10		10	μA

LVDS Transmitter (Pin type “**LVDS OUT**”) DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS= H	250	350	450	mV
			Reduced swing RS= L	140	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=GND, RL=100Ω				100	mA
I_{OZ}	Output TRI-State current	/PDWN=L, VOUT=GND~LVDSVCC		-20		20	μA

Electrical Characteristics (Continued)

Supply Current

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions			Typ.[a]	Max.[b]	Units
I_{TCCW}	Transmitter Supply Current	RL=100Ω CL=5pF RS = H (RS = L)	MODE=H Single-out	CLKIN=37MHz	24 (18)	33 (26)	mA
				CLKIN=65MHz	29 (23)	43 (37)	mA
				CLKIN=72MHz	30 (24)	46 (40)	mA
			MODE=L Dual-out DDRN=H DDR Input Off	CLKIN=89MHz	48 (36)	65 (53)	mA
				CLKIN=119MHz	53 (41)	75 (63)	mA
				CLKIN=139MHz	56 (44)	82 (70)	mA
				CLKIN=154MHz	58 (46)	88 (76)	mA
			MODE=L Dual-out DDRN=L DDR Input On	CLKIN=44.5MHz	47 (35)	64 (52)	mA
				CLKIN=59.5MHz	51 (39)	74 (62)	mA
				CLKIN=69MHz	54 (42)	80 (68)	mA
				CLKIN=77MHz	56 (44)	85 (73)	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L, All Inputs = Fixed L or H			1	50	uA

(a) All Typ. values are at Vcc=1.8V, Ta=25°C . The 256 Grayscale Test Pattern inputs test for a typical display pattern.

(b) All Max. values are at Vcc=1.98V, Ta=85°C . Worst Case Test Pattern produces maximum switching frequency for all the LVDS outputs (Fig.1).

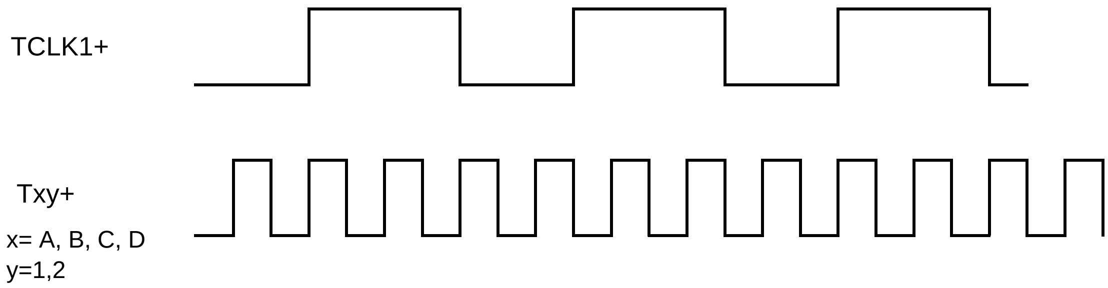


Fig1. Test Pattern
(LVDS Output Full Toggle Pattern)

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{TCIP}	CLK IN Period(Fig4,5)		5.75		100	ns
t_{TCH}	CLK IN High Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLK IN Low Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLK IN(Fig4,5)		0.8			ns
t_{TH}	TTL Data Hold from CKL IN(Fig4,5)		0.8			ns
t_{TCD}	CLK IN to TCLK+/- Delay (Fig4,5)	MODE=L,DDR=H	$9t_{TCIP}+3.1$		$9t_{TCIP}+8.0$	ns
		Others	$5t_{TCIP}+3.1$		$5t_{TCIP}+8.0$	ns
t_{TCOP}	CLK OUT Period(Fig6)		5.75		100	ns
t_{LVT}	LVDS Transition Time(Fig2)			0.6	1.5	ns
t_{TOP1}	Output Data Position0 (Fig6)	t_{TCOP} = 5.75ns~15ns	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (Fig6)		$\frac{t_{TCOP}}{7}-0.15$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7}+0.15$	ns
t_{TOP6}	Output Data Position2 (Fig6)		$2\frac{t_{TCOP}}{7}-0.15$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7}+0.15$	ns
t_{TOP5}	Output Data Position3 (Fig6)		$3\frac{t_{TCOP}}{7}-0.15$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7}+0.15$	ns
t_{TOP4}	Output Data Position4 (Fig6)		$4\frac{t_{TCOP}}{7}-0.15$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7}+0.15$	ns
t_{TOP3}	Output Data Position5 (Fig6)		$5\frac{t_{TCOP}}{7}-0.15$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7}+0.15$	ns
t_{TOP2}	Output Data Position6 (Fig6)		$6\frac{t_{TCOP}}{7}-0.15$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7}+0.15$	ns
t_{TPLL}	Phase Lock Time(Fig3)				10.0	ms
t_{DEINT}	DE input period (Fig3-1) Dual out mode only (MODE=L)		$4t_{TCIP}$	tTCIP*(2n)(a)		ns
t_{DEH}	DE High time (Fig3-1) Dual-out mode only (MODE=L)		$2t_{TCIP}$	tTCIP*(2m)(a)		ns
t_{DEL}	DE Low time(Fig3-1) Dual-out mode only (MODE=L)		$2t_{TCIP}$			ns

(a) Refer to Fig3-1 for details.

AC Timing Diagrams

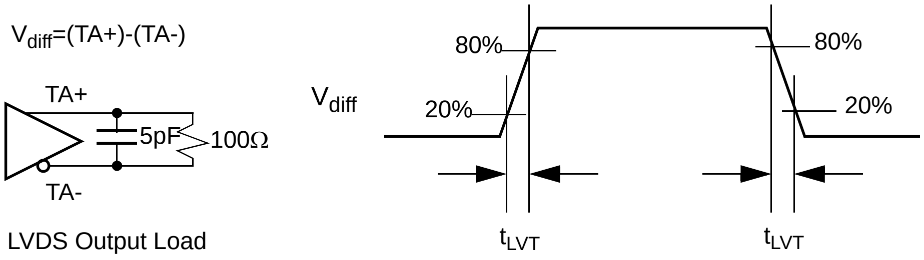


Fig2. LVDS Output Load and Transition Time

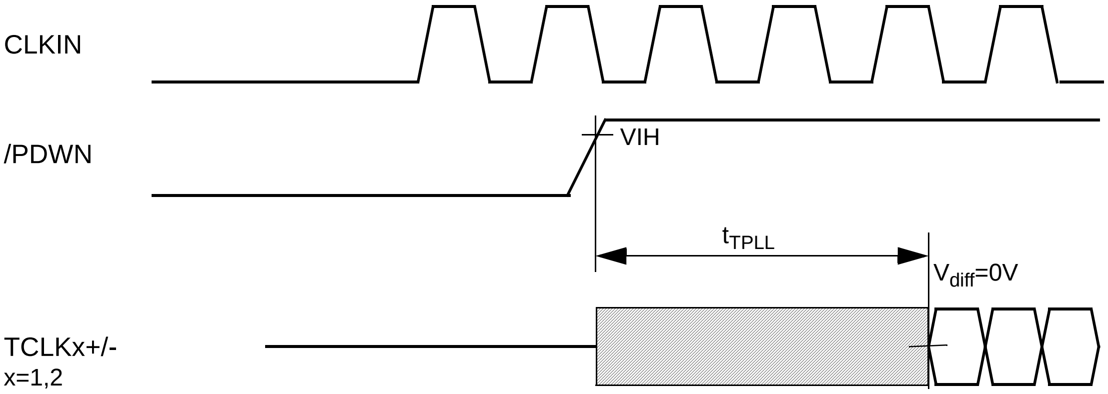
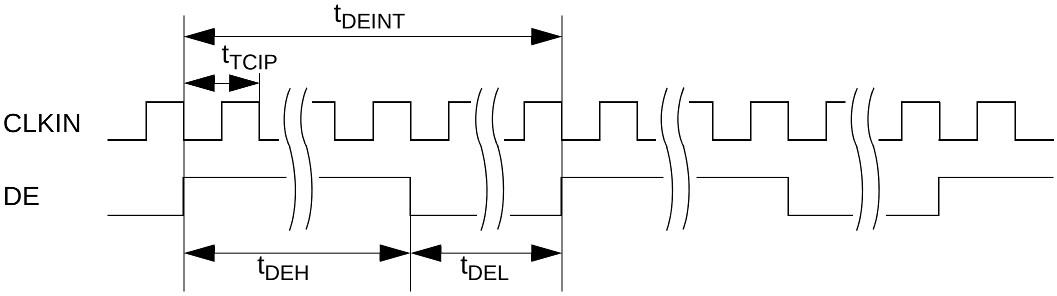


Fig3. PLL Lock Time



Note: In dual-out mode (MODE=L),
the period between rising edges of DE (t_{DEINT}), high time of DE (t_{DEH})
should always satisfy following equations.

$$t_{DEH} = tTCIP * (2m)$$
$$t_{DEINT} = tTCIP * (2n)$$
m, n =integer

Fig3-1. Dual OUT mode DE input timing

AC Timing Diagrams (Continued)

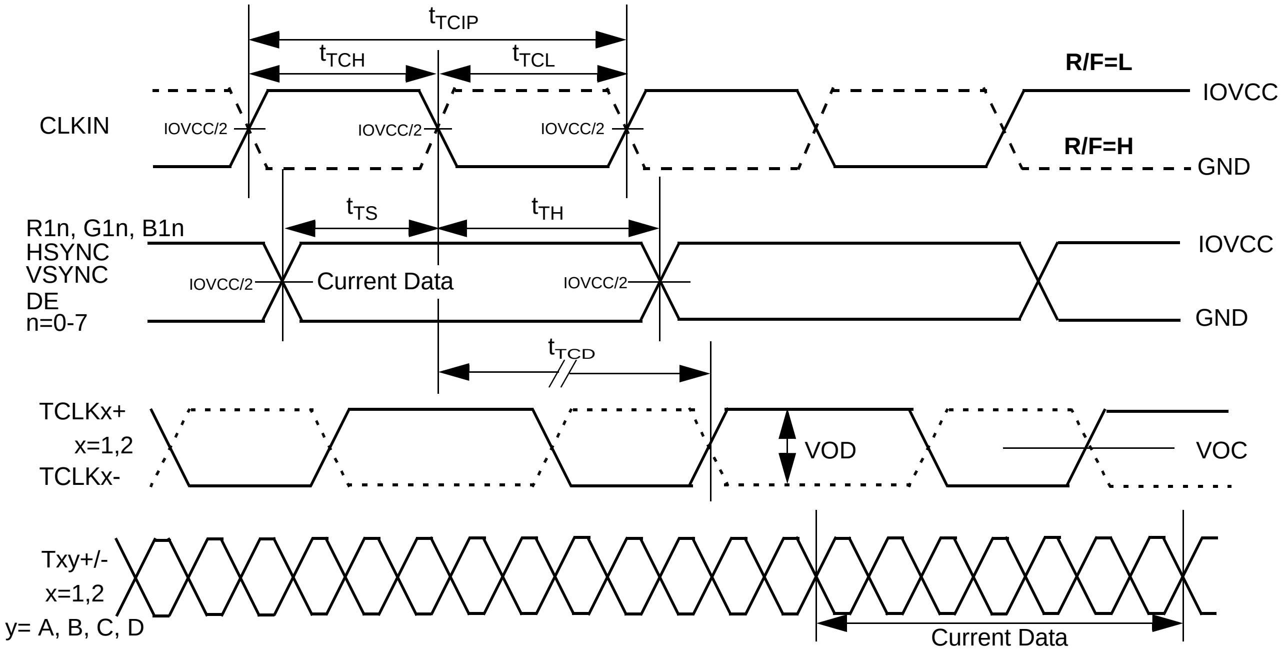
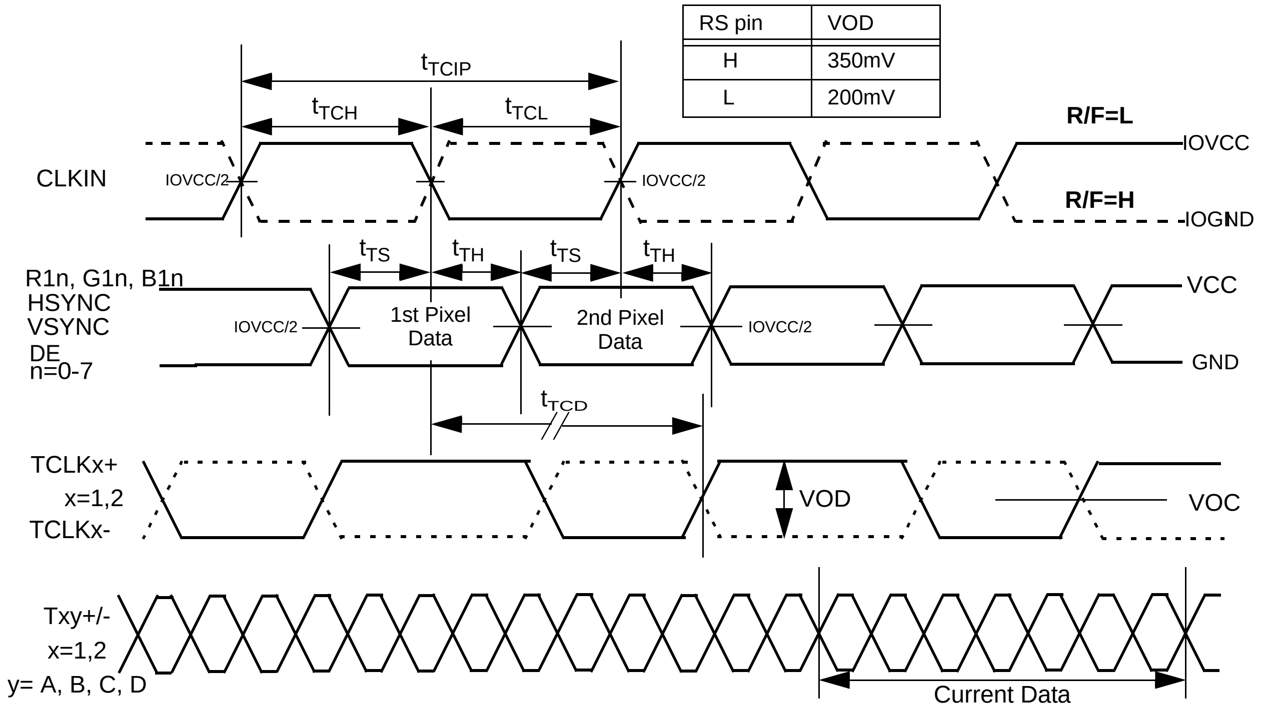


Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing for Single Edge Input Mode

MODE=H or MODE=L,DDR=H

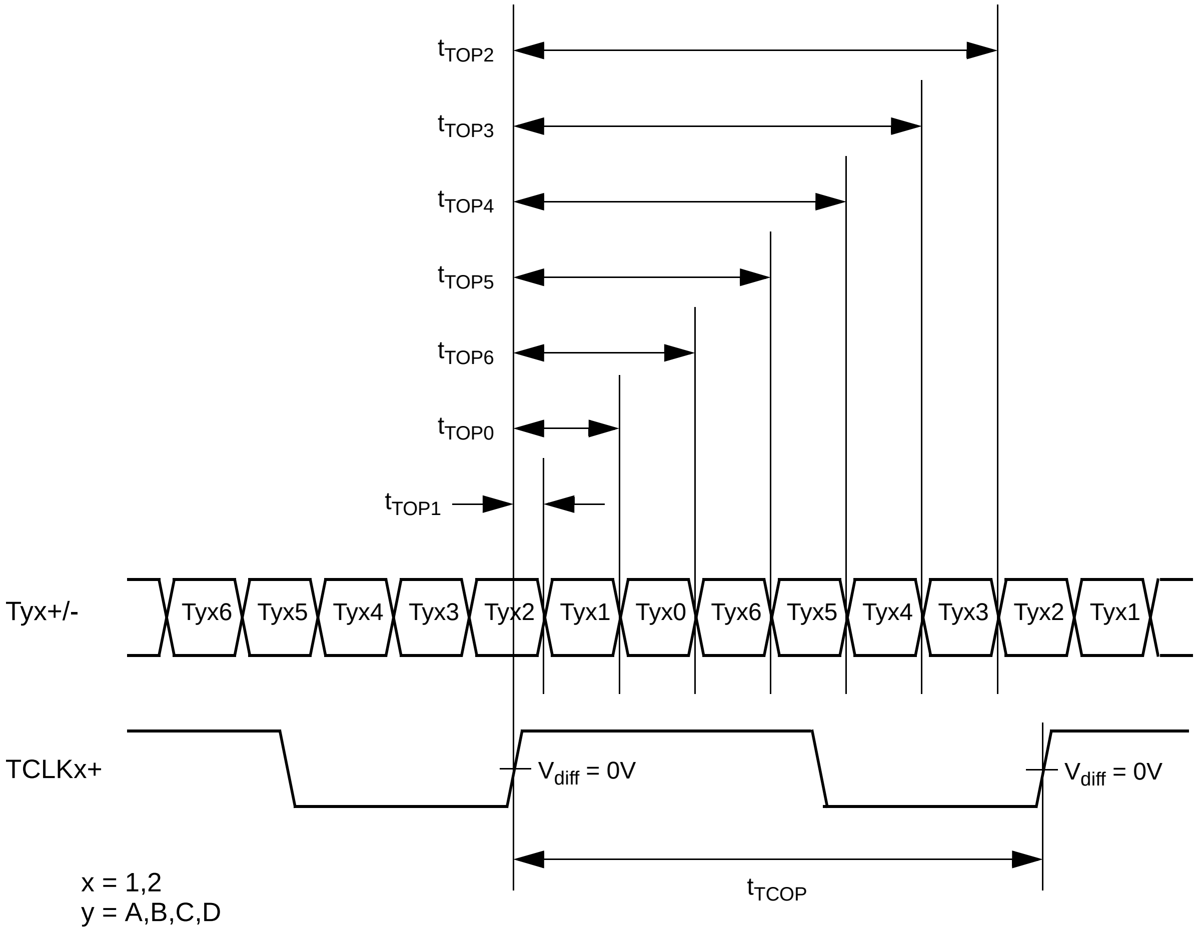


RS pin	VOD
H	350mV
L	200mV

Fig5. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode (DDR)

MODE=L,DDRN=L

AC Timing Diagrams (Continued)



Note:
V_{diff} = (Tyx+) - (Tyx-), (TCLKx+) - (TCLKx-)

Fig6. LVDS Output Data Position

Single-In / Dual-Out Mode (MODE = L)

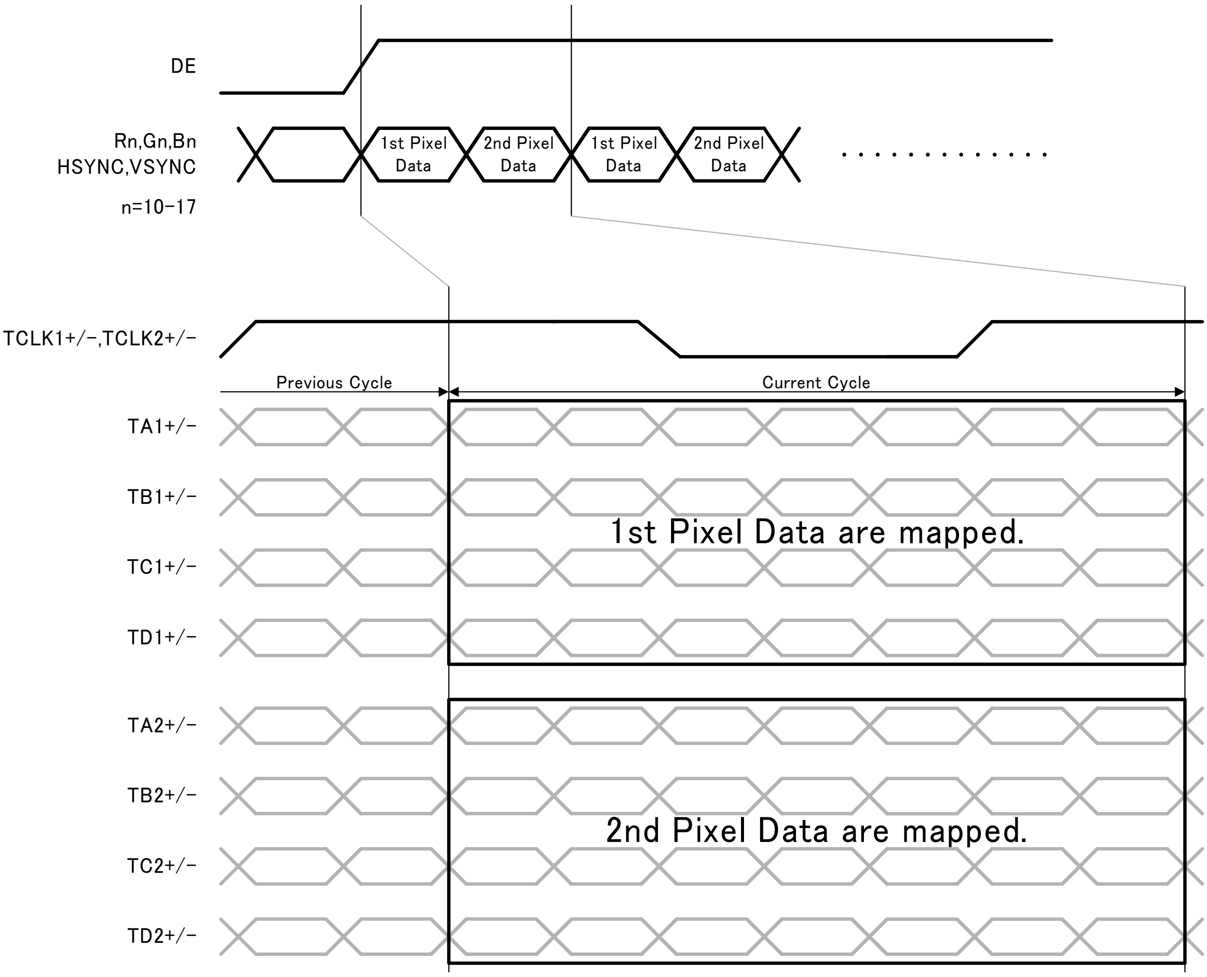


Fig7. Single-In / Dual-Out Mode (MODE=L)

Single-In / Single-Out Mode (MODE=H)

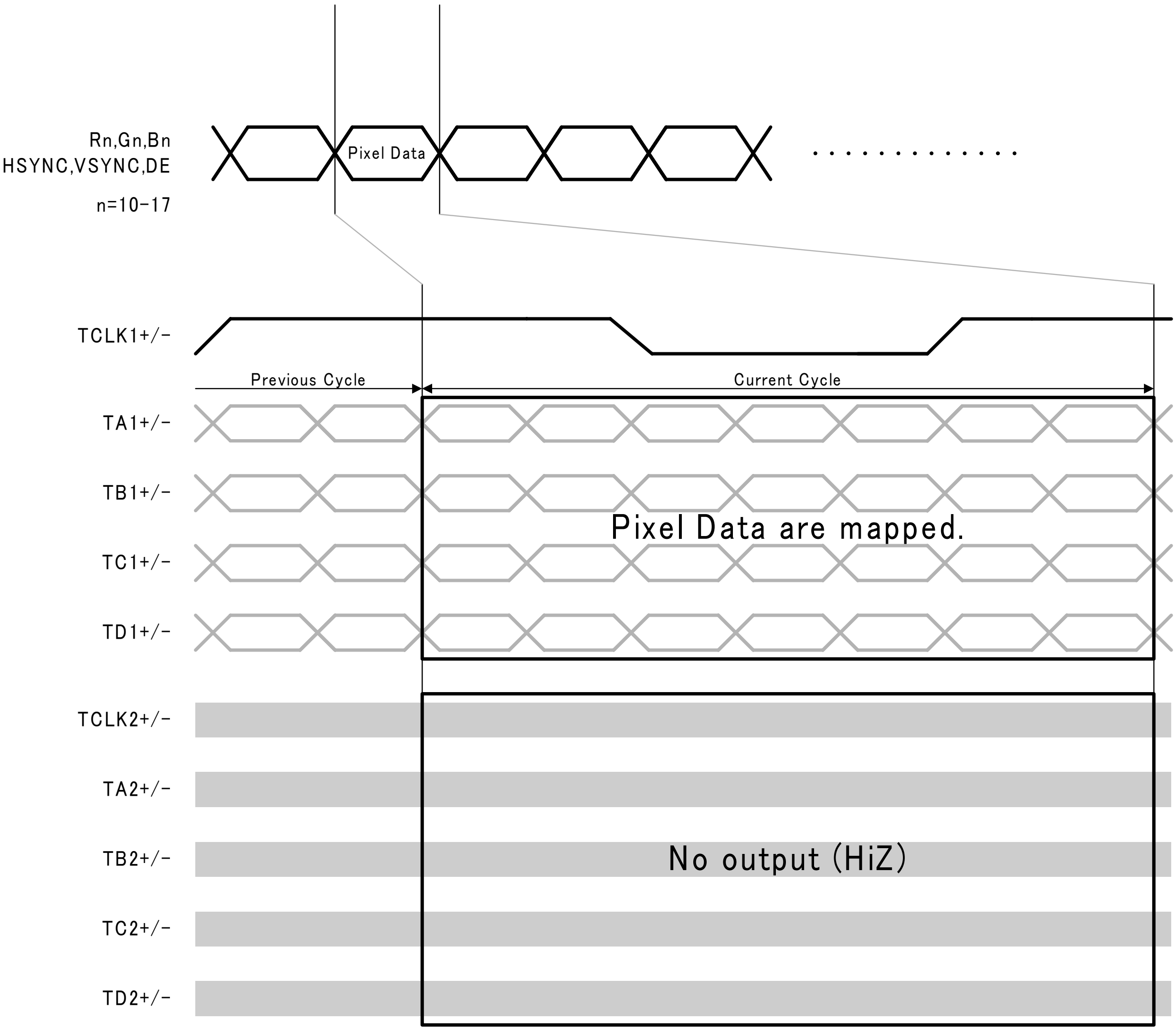
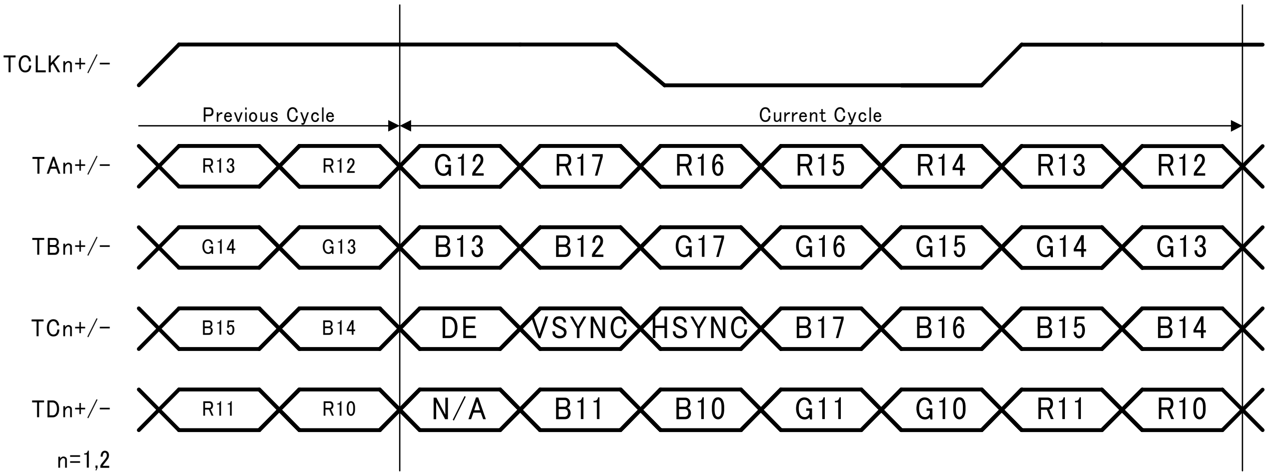
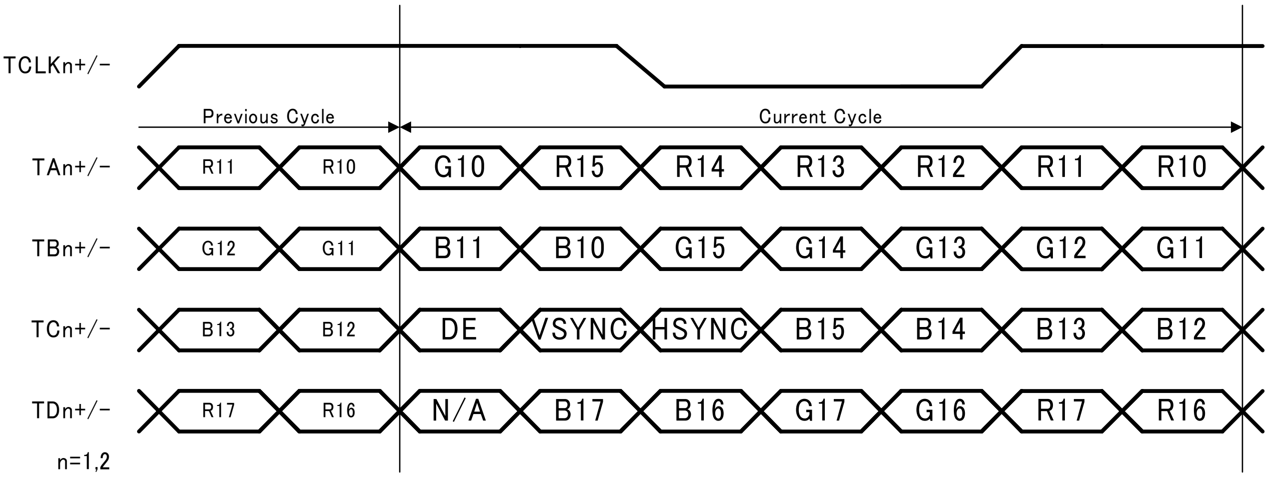


Fig8. Single-In / Single-Out Mode (MODE=H)

LVDS Data Mapping for 8 bit mode (6B/8B=L)



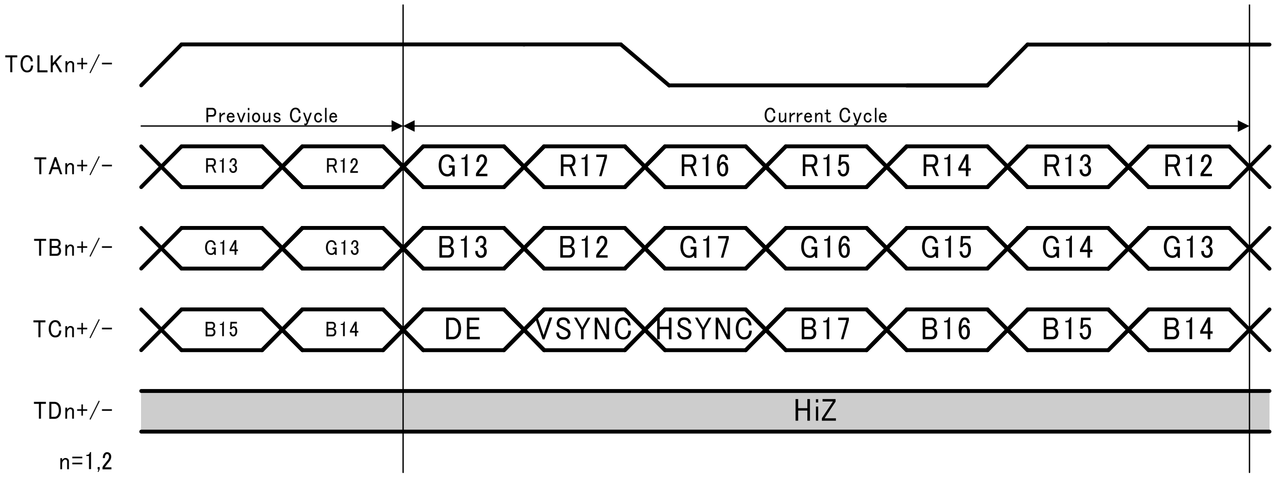
(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)



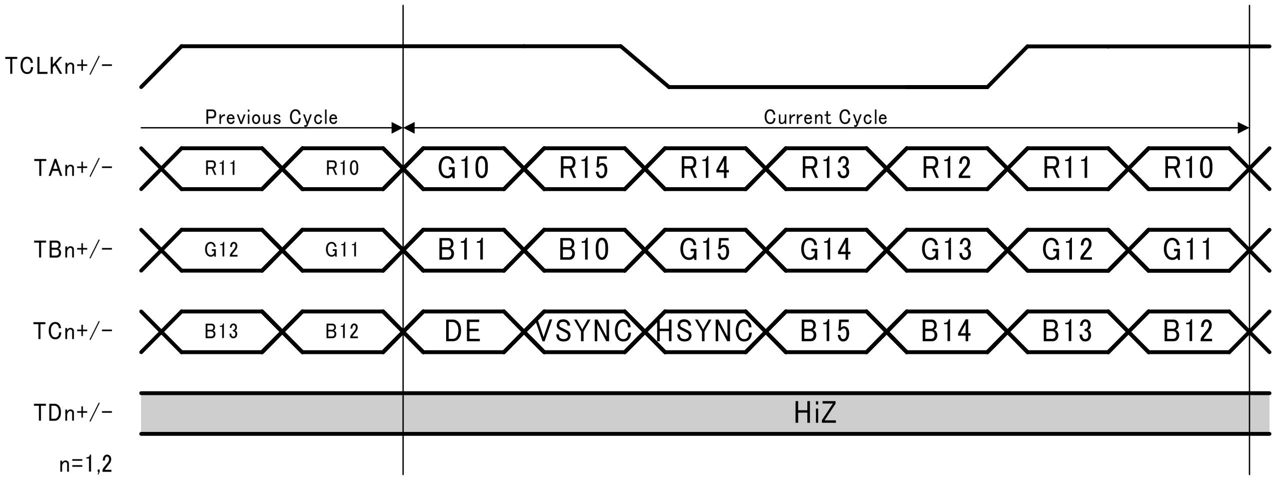
(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

Fig9. LVDS Data Mapping for 8 bit mode (6B/8B=L)

LVDS Data Mapping for 6 bit mode (6B/8B=H)



(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)



(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

Fig10. LVDS Data Mapping for 6 bit mode (6B/8B=H)

Note: Input pins which are not used in 6 bit mode (R10-11,G10-11,B10-11 on Mapping Mode 1, R16-17,G16-17,G16-17 on Mapping Mode 2) can be H, L, or Open.

Note

1)Cable Connection and Disconnection

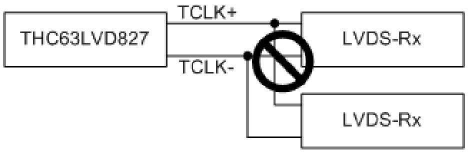
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2)GND Connection

Connect the each GND of the PCB which THC63LVD827 and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

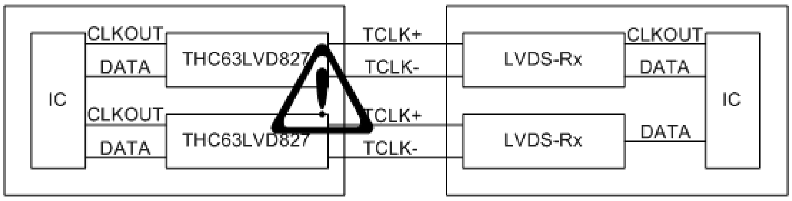
3)Multi Drop Connection

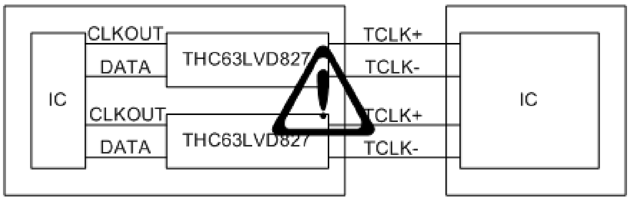
Multi drop connection is not recommended.



4)Asynchronous use

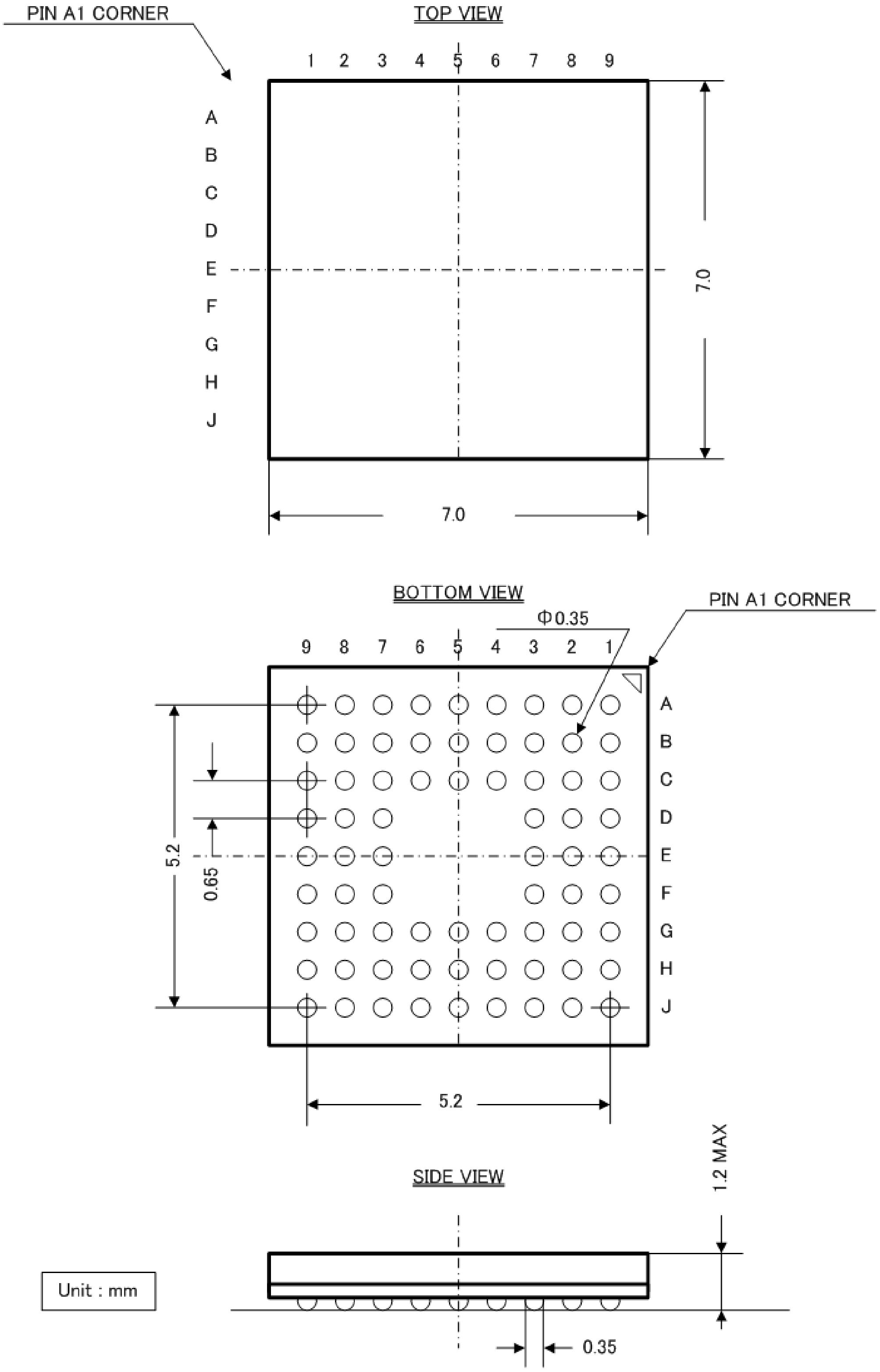
Asynchronous use such as following systems are not recommended.





Package

TFBGA



Notices and Requests

1.)The product specifications described in this material are subject to change without prior notice.
2.)The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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5.)This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6.)Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7.)Please note that this product is not designed to be radiation-proof.
8.)Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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