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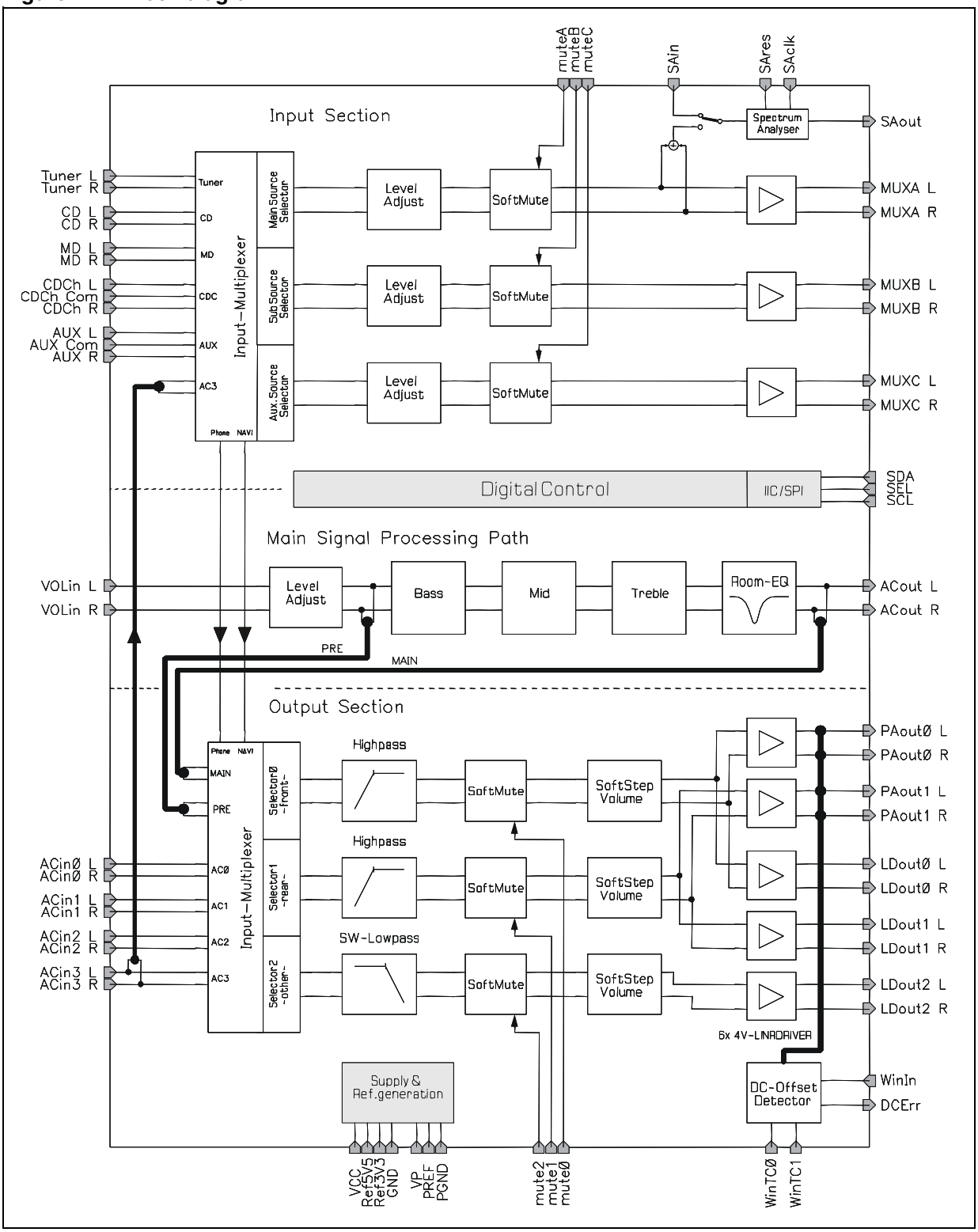
1 Block diagram

Figure 1. Block diagram



2 Pin description

2.1 ESD:

All pins are protected against ESD according to the MIL883 standard.

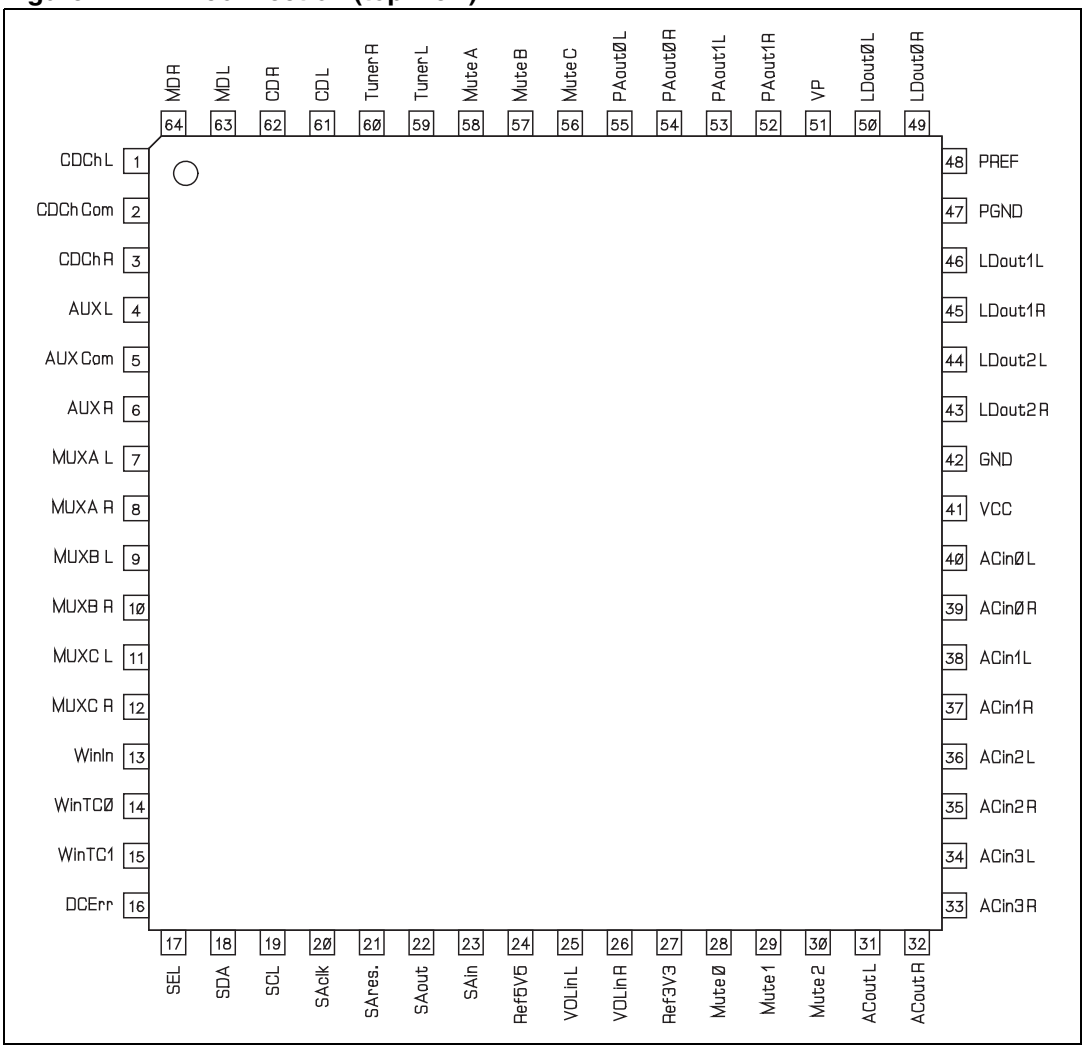
2.2 Thermal data

Table 2. Thermal data

Symbol	Description	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal resistance junction-to-pins	50	°C/W

2.3 Pin assignment

Figure 2. Pin connection (top view)



2.4 Pin function

Table 3. Pin description

PIN	Direction (1)	Name	Description
1	I	CDCh L	CD-changer input, pseudo differential, left channel
2	I	CDCh Common	CD-changer input, pseudo differential common
3	I	CDCh R	CD-changer input, pseudo differential, right channel
4	I	AUX L	Aux./Navigation input, pseudo differential, left channel
5	I	AUX Common	Aux./Navigation input, pseudo differential common
6	I	AUX R	Aux./Navigation input, pseudo differential, right channel
7	O	MUXA L	IN-Section, signal path A output (Main), left channel
8	O	MUXA R	IN-Section, signal path A output (Main), right channel
9	O	MUXB L	IN-Section, signal path B output (Sub), left channel
10	O	MUXB R	IN-Section, signal path B output (Sub), right channel
11	O	MUXC L	IN-Section, signal path C output (Aux.), left channel
12	O	MUXC R	IN-Section, signal path C output (Aux.), right channel
13	I	WinIn	Zero-window Sense input (from power-amp)
14	P	WinTC0	Zero-window comparator 0 time constant
15	P	WinTC1	Zero-window comparator 1 time constant
16	O	DCErr	DC-detector Error output
17	I	SEL	Interface-select; SPI: receive enable
18	I / OC	SDA	I^2C/SPI-bus serial data input/output
19	I	SCL	I^2C/SPI-bus serial clock input
20	I	SAclk	Spectrum analyzer clock input
21	I	SAres.	Spectrum analyzer reset
22	O	SAout	Spectrum analyzer analog voltage output
23	I	SAin	Spectrum analyzer external input
24	P	Ref5V5	5.5V-reference decoupling pin, connects to external capacitor
25	I	VolIn L	Main signal path input, left channel
26	I	VolIn R	Main signal path input, right channel
27	P	Ref3V3	3.3V-reference decoupling pin, connects to external capacitor
28	I	Mute0	OUT-section, signal path 0 (front) direct mute
29	I	Mute1	OUT-section, signal path 1 (rear) direct mute
30	I	Mute2	OUT-section, signal path 2 (other) direct mute
31	O	ACout L	Main signal path output, left channel

Table 3. Pin description (continued)

PIN	Direction (1)	Name	Description
32	O	ACout R	Main signal path output, right channel
33	I	ACin3 R	OUT-section, AC-coupled input 3, right channel
34	I	ACin3 L	OUT-section, AC-coupled input 3, left channel
35	I	ACin2 R	OUT-section, AC-coupled input 2, right channel
36	I	ACin2 L	OUT-section, AC-coupled input 2, left channel
37	I	ACin1 R	OUT-section, AC-coupled input 1, right channel
38	I	ACin1 L	OUT-section, AC-coupled input 1, left channel
39	I	ACin0 R	OUT-section, AC-coupled input 0, right channel
40	I	ACin0 L	OUT-section, AC-coupled input 0, left channel
41	S	VCC	Device supply pin
42	S	GND	Device ground pin
43	O	LDout2 R	Line-driver output, signal path 2 (other), right channel
44	O	LDout2 L	Line-driver output, signal path 2 (other), left channel
45	O	LDout1 R	Line-driver output, signal path 1 (rear), right channel
46	O	LDout1 L	Line-driver output, signal path 1 (rear), left channel
47	S	PGND	Device ground pin (dual supply), connects to system ground
48	P	PREF	Line-driver-reference decoupling pin, connects to external capacitor
49	O	LDout0 R	Line-driver output, signal path 0 (front), right channel
50	O	LDout0 L	Line-driver output, signal path 0 (front), left channel
51	S	VP	Device supply pin (dual supply), Output section
52	O	PAout1 R	Out-section rear output, right channel
53	O	PAout1 L	Out-section rear output, left channel
54	O	PAout0 R	Out-section front output, right channel
55	O	PAout0 L	Out-section front output, left channel
56	I	Mute C	IN-section, signal path 2 (Aux.) direct mute
57	I	Mute B	IN-section, signal path 1 (Sub) direct mute
58	I	Mute A	IN-section, signal path 0 (Main) direct mute
59	I	Tuner L	Tuner input, left channel
60	I	Tuner R	Tuner input, right channel
61	I	CD L	CD input, left channel
62	I	CD R	CD input, right channel
63	I	MD L	Minidisk (mono-differential Phone+) input, left channel
64	I	MD R	Minidisk (mono-differential Phone-) input, right channel

1. I= input, O= output, OC =open collector, P= passive external component, S= supply

3 Deatailed features

The TDA7415CB is composed of four major building blocks. - The IN-section, the spectrum-analyzer, the main signal processing path and the OUT-section; Individually featuring:

IN section

- Three independent signal-paths (front, rear and auxiliary) with independent soft-mute.
- Six stereo inputs; 3 single ended; 1 single ended or full differential mono; 2 quasi-differential.
- ±15dB level-adjust with 1 dB steps.
- Pin-accessible and/or I^2C/SPI-controlled soft-mute (direct mute) for each signal path.

Spectrum analyzer

- 7-band, fully integrated 2^{nd}-order band-pass filters with programmable filter quality for different visual behavior.
- Dedicated one or two-wire serial port for analog data-readout.
- Analog output voltage 3.3 V-µP compatible.

Main signal processing path

- ±15dB level-adjust with 1dB steps.
- Fully integrated bass-, middle- and treble-tone control. All filters offer 2^{nd}-order frequency response with programmable filter quality and center frequency.
- Room-acoustics notch filter (Room-EQ) allows the suppression of primary car-body resonance.

OUT section

- Three independent signal-paths (front, rear and others) with individual soft-mute.
- Four AC-coupled, single ended stereo inputs.
- Pin-accessible soft-mute (direct mute), for each signal path.
- I^2C/SPI-controlled soft-mute, independent for all six (mono) channels
- Main signal path monitor-select (pre/post tone control).
- L/R-channel independent phone, navigation or phone/navigation-mix signal interrupts for front signal path; L/R-channel independent phone or navigation interrupts for rear- and others-path.
- 2^{nd}-order frequency response high-pass filters for front- and rear-signal path.
- 2^{nd}-order frequency response subwoofer low-pass filter for others-signal path.
- Soft-step volume with 79 to 25 dB range for each signal path.
- Four dedicated outputs for an internal (on-board) power amplifier.
- Six $4V_{RMS}$ line-driver outputs for an external (remote) power amplifier.
- Offset voltage detection circuit for on-board power amplifier failure diagnosis.

4 Electrical specification

4.1 Supply

Table 4. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	-	7.5	8.5	9.5	V
V_P	Supply current (line driver)	-	7.5	12	13	V
I_{total}	Total supply current	V_{CC} = 8.5 V; V_P = 12V	-	45	-	mA
SVRR	Ripple rejection @ 1 kHz	Audio processor (all filters flat)	-	60	-	dB

4.2 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Operating supply voltage	10	V
V_P	Operating supply voltage	13	V
T_{amb}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

4.3 Electrical characteristcs

4.3.1 Input section

V_{CC} = 8.0 V; V_P = 12.0 V; T_{amb} = 25 °C; R_L =10 kΩ ; all gains = 0 dB; f = 1 kHz; unless otherwise specified.

Table 6. Input section

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
R_{in}	Input Impedance	Single-ended inputs	70	100	130	kΩ
		Differential inputs	70	100	130	kΩ
		MD-input, differential mode	35	56	65	kΩ
V_{CL}	Input Clipping Level (THD ≤ 0.1%)	Single ended inputs	1.4	1.5	-	V_{RMS}
		Differential inputs; (1)	2.0	2.2	-	V_{RMS}
CMRR	Common mode rejection ratio Differential inputs (CD, AUX.)	V_{CM} = 1 V_{RMS} @ 1 kHz	40	70	-	dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	40	60	-	dB

Table 6. Input section (continued)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
$CMRR_{MD}$	Common mode rejection ratio Mono differential input (MD)	V_{CM} = 1 V_{RMS} @ 1 kHz	40	66	-	dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	40	56	-	dB
S_{IN}	Input separation	-	80	100	-	dB
$G_{IN\ MIN}$	Min. input gain	input to output, (1)	-16	-15	-14	dB
$G_{IN\ MAX}$	Max. input gain		14	15	16	dB
G_{STEP}	Gain-adjust step resolution	-	0.5	1	1.5	dB
V_{DC}	DC-offset steps	Adjacent gain steps	-	0.5	6	mV
		G_{MIN} to G_{MAX}	-	5	35	mV
ATT_{MUTE}	Mute attenuation	-	80	100	-	dB
t_{SMC}	Soft-mute completion time, ramp-up or -down	T1	0.1	0.24	0.4	ms
		T2	0.25	0.48	0.75	ms
		T3	7	10.2	13	ms
		T4	16	20.4	26	ms
V_{NO}	Output-noise, MUX-Outputs	20 Hz - 20 kHz; all flat, 0 dB	-	8	15	µV
$V_{OUT,max}$	Maximum output level	$R_{LOAD} \geq 2$ kΩ; THD ≤ 0.1 %	1.4	1.5	-	V_{RMS}
RL	Output load resistance	THD ≤ 0.1 %	1.0	-	-	kΩ
C_L	Output load capacitance	-	-	-	10	nF
R_{OUT}	Output impedance	-	-	24	100	Ω
V_{DC}	DC voltage level	-	3.1	3.3	3.5	V
Spectrum Analyzer (see figure 21)						
R_{in}	Input impedance	-	70	100	130	kΩ
V_{SAin}	Max. Input level, SAin-pin	3.3V full scale at SAout-pin	-	1.0	-	V_{RMS}
V_{SAout}	Output Voltage Range	$R_{LOAD} \geq 1$MΩ; $V_{SAin} \leq 1V_{RMS}$	0	-	3.3	V
f_{C1}	Center Frequency, band 1 (2)	-	55	62	69	Hz
f_{C2}	Center Frequency, band 2 (2)	-	141	157	173	Hz
f_{C3}	Center Frequency, band 3 (2)	-	356	396	436	Hz
f_{C4}	Center Frequency, band 4 (2)	-	0.9	1	1.1	kHz
f_{C5}	Center Frequency, band 5 (2)	-	2.26	2.51	2.76	kHz
f_{C6}	Center Frequency, band 6 (2)	-	5.70	6.34	6.98	kHz
f_{C7}	Center Frequency, band 7 (2)	-	14.4	16.0	17.6	kHz
Q_f	Filter Quality Factor (2)	Q_1	1.40	1.75	2.10	-
		Q_2	2.80	3.5	4.20	-
f_{SAclk}	Read-out clock frequency	-	1	-	100	kHz
t_{SAdel}	Analog output delay time	C_{Load} at SAout-pin ≤ 100 pF	-	1	2	µs

Table 6. Input section (continued)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
t_{repeat}	Read-out cycle repeat time	Recommended refresh rate	50	-	-	ms
t_{intres}	Internal reset time	Auto-reset mode enabled	3	4	5	ms
t_{SAres}	Reset pulse width	Auto-reset mode disabled	500	-	-	ns

1. All differential inputs or differential configurations have -3 dB input gain.

4.3.2 Main signal processing path

Table 7. Main signal processing path

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
R_{in}	Input impedance	-	35	50	65	kΩ
V_{CL}	Input clipping level	THD ≤ 0.1 %	1.4	1.5	-	V_{RMS}
$G_{IN\ MIN}$	Min. input gain	input to output; all filters flat	-16	-15	-14	dB
$G_{IN\ MAX}$	Max. input gain	-	14	+15	16	dB
G_{STEP}	Gain-adjust step resolution	-	-	1	-	dB
V_{DC}	DC-offset steps	Adjacent gain steps	-	0.5	6	mV
		G_{MIN} to G_{MAX}	-	5	30	mV
$V_{OUT,max}$	Maximum output level	R_{LOAD} ≥ 2 kΩ; THD ≤ 0.1 %	1.4	1.5	-	V_{RMS}
R_L	Output load resistance	THD ≤ 0.1 %	1.0	-	-	kΩ
C_{OUT}	Output load capacitance	-	-	-	10	nF
R_{OUT}	Output impedance	-	-	24	36	Ω
V_{DC}	DC voltage level	-	3.1	3.3	3.5	V
Bass Control						
G_{RANGE}	Gain control range	-	±13	±15	±17	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_C	Center frequency (1)	f_{C0}	30	40	50	Hz
		f_{C1}	40	50	50	Hz
		f_{C2}	50	60	70	Hz
		f_{C3}	60	70	90	Hz
		f_{C4}	60	80	100	Hz
		f_{C5}	80	100	120	Hz
		f_{C6}	100	120	140	Hz
		f_{C7}	120	150	170	Hz

Table 7. Main signal processing path (continued)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
Q_{BASS}	Quality factor (1)	Q_1	0.9	1	1.1	-
		Q_2	1.13	1.25	1.38	-
		Q_3	1.35	1.5	1.65	-
		Q_4	1.8	2	2.2	-
DC_{GAIN}	Bass DC-gain	DC-mode= off	-1	0	1	dB
		DC-mode= on	3.5	4.4	5.5	dB
MID control						
G_{RANGE}	Gain control range	-	±13	±15	±17	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_C	Center frequency (2)	f_{C1}	450	500	550	Hz
		f_{C2}	0.9	1	1.1	kHz
		f_{C3}	1.35	1.5	1.65	kHz
		f_{C4}	1.8	2	2.2	kHz
Q_{MID}	Quality factor (2)	Q_1	0.5	1	1.1	-
		Q_2	1.8	2	2.2	-
Treble Control						
G_{RANGE}	Gain control range	-	±13	±15	±17	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_C	Center frequency (1))	f_{C1}	6.4	10	13.6	kHz
		f_{C2}	8.0	12.5	17	kHz
		f_{C3}	9.6	15	20.4	kHz
		f_{C4}	11.2	17.5	23.8	kHz
ROOM-EQ (acoustics notch-filter)						
G_{RANGE}	Gain control range	-		-0…9	-	dB
A_{STEP}	Step resolution	Non-uniform, see description	1	-	2	dB
f_C	Notch frequency (1)	f_{N1}	162	180	198	Hz
		f_{N2}	180	200	220	kHz
		f_{N3}	198	220	242	kHz
		f_{N4}	216	240	264	kHz
Q_{EQ}	Quality factor(1)	Q_1	0.9	1	1.1	-
		Q_2	1.8	2	2.2	-

1. Min and Max values are calculated according to simulation results; Functionality is guaranteed by measuring a directly correlated parameter

4.3.3 Output section

V_{CC} = 8.0 V; V_P = 12.0 V; T_{amb} = 25 °C; R_L =10 kΩ ; all gains = 0 dB; f = 1 kHz; unless otherwise specified

Table 8. Output section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{in}	Input impedance	AC0…3 inputs	35	50	65	kΩ
V_{CL}	Input Clipping Level	THD ≤ 0.1%	1.4	1.5	-	V_{RMS}
ATT_{MUTE}	Mute Attenuation	-	80	100	-	dB
t_{SMC}	Soft-mute completion time, ramp-up or -down	T1	0.21	0.24	0.26	ms
		T2	0.43	0.48	0.52	ms
		T3	10.47	11.5	12.45	ms
		T4	5.23	5.76	6.22	ms
Volume (Soft-step)						
G_{MAX}	Max. gain	-	-	25	-	dB
A_{MAX}	Max. attenuation	-	-82	-79	-76	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
E_A	Attenuation set error	G= -20 to +20 dB	-1.25	0	+1.25	dB
		G= -20 to -60 dB	-3	0	3	dB
E_T	Tracking error	-	-	-	2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-	0.1	3	mV
		From 0dB to G_{MIN}	-	0.5	5	mV
High Pass						
f_C	Center frequency (1)	f_{C0}	34	40	46	Hz
		f_{C1}	52	60	68	Hz
		f_{C2}	72	80	88	Hz
		f_{C3}	90	100	110	Hz
		f_{C4}	108	120	132	Hz
		f_{C5}	135	150	165	Hz
		f_{C6}	162	180	198	Hz
		f_{C7}	198	220	242	Hz
Q_{HP}	Quality factor (2)	Butterworth characteristics	0.665	0.707	0.750	-
Subwoofer low pass						
f_C	Center Frequency (2)	f_{C0}	44	50	56	Hz
		f_{C1}	54	60	66	Hz
		f_{C2}	72	80	88	Hz
		f_{C3}	90	100	110	Hz
		f_{C4}	108	120	132	Hz
Q_{HP}	Quality Factor (2)	Butterworth characteristics	0.665	0.707	0.750	-
Audio outputs						
$V_{PA,max}$	Max. output level; PA-outputs	R_{LOAD} ≥ 2 kΩ; THD ≤ 0.1 %	1.88	2	-	V_{RMS}

Table 8. Output section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LD,max}$	Max. output level; LD-outputs	as above; V_{CC} = 8.0 V	2.20	2.75		V_{RMS}
		as above; V_P = 12 V	3.75	4		V_{RMS}
R_L	Output load resistance	THD ≤ 0.1 %; all outputs	1.0			kΩ
C_L	Output load capacitance	All outputs			10	nF
R_{OUT}	Output impedance	All outputs		24	100	Ω
V_{DC}	DC voltage level	PA-outputs	3.8	4.0	4.2	V
		LD-outputs	V_P / 2 -200mV	V_P / 2	V_P / 2 +200mV	V

1. All differential inputs or differential configurations have -3dB input gain.
2. Min and Max values are calculated according to simulation results; Functionality is guaranteed by measuring a directly correlated parameter

4.3.4 General

Table 9. General

Symbol	Parameter	Test conditions / remark		Min.	Typ.	Max.	Unit
V_{NO}	Output noise	BW = 20 Hz to 20 kHz	output mode	-	10	15	μV
		unveighted	all flat, 0 dB	-	12	20	μV
S/N	Signal to noise ratio	all flat, 0 dB; V_O= 1.5 V_{RMS}		-	110	-	dB
		All tone filters +10 dB; A-weighted; V_O= 1.5 V_{RMS}		-	84	-	dB
d	Distortion	V_{OUT}= 1 V_{RMS}; all stages 0 dB		-	0.01	0.1	%
		All tone filters +10 dB; A-weighted; V_O= 1.5 V_{RMS}		-	0.05	0.1	%
S_C	Channel separation L/R	-		80	100	-	dB
E_T	Total tracking error	A_V = 0 to -20 dB		-	0	1	dB
		A_V = -20 to -60 dB		-	0	2	dB
V_{POR}	Internal POR Voltage	-		-	-	3.4	V

4.3.5 Bus and control inputs

Table 10. Bus and control inputs
(I^2C/SPI, spectrum analyzer, direct-mute, offset detector)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	*SDA-, SCL-, SEL-, WinIn*-pin	-	0.8	0.7	V
V_{IH}	Input high voltage	-	2.5	2.4	-	V
V_{TH}	Input threshold voltage	*SAres-, SAclk-, all Mute*-pins	-	1.5	-	V
V_{TH}	Input threshold hysteresis	-	-	100	-	mV
I_{IN}	Input current	V_{IN}= 0.4V; *SDA-, SCL*-pin	-5	-	5	µA
$V_{TH,SPI}$	SPI-mode threshold voltage	(1)	-	-	5.5	V
$V_{O,ACK}$	SDA-acknowledge output volt.	I_O= 1.6mA	-	-	0.4	V
R_{PULLUP}	Pull-up resistance	*WinIn*-pin	30	50	70	kΩ
I_{PULLUP}	Pull-up current	V_{IN}= 0V, all Mute-pins	50	100	150	µA
f_{SCKmax}	Maximum clock speed	SPI-mode	-	-	2000	kbit/s
		I^2C-mode	-	-	800	kbit/s

1. pull-up is needed for I^2C Mute

4.3.6 DC offset detector

Table 11. DC offset detector

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
V_{th}	Zero comp. window size	V1	-	±25	-	mV
		V2	-	±50	-	mV
		V3	-	±75	-	mV
		V4	-	±100	-	mV
τ_{sp}	Max. rejected spike length	τ1	-	7.5	-	µs
		τ2	-	15	-	µs
		τ3	-	22.5	-	µs
		τ4	-	30	-	µs
$I_{Err,charge}$	DCErr charge current	-	1	5	10	µA
$I_{Err,discharge}$	DCErr discharge current	-	2.5	5	7.5	mA
V_{OutH}	DCErr high voltage	-	2.5	3.3	-	V
V_{OutL}	DCErr low voltage	-	-	150	300	mV

5 Description of the audio processor

As can be seen from the block diagram in *Figure 1*, the Audio processor is composed of three building blocks. - The INPUT-Section, the MAIN-SIGNAL-PROCESSING-path and the OUTPUT-Section.

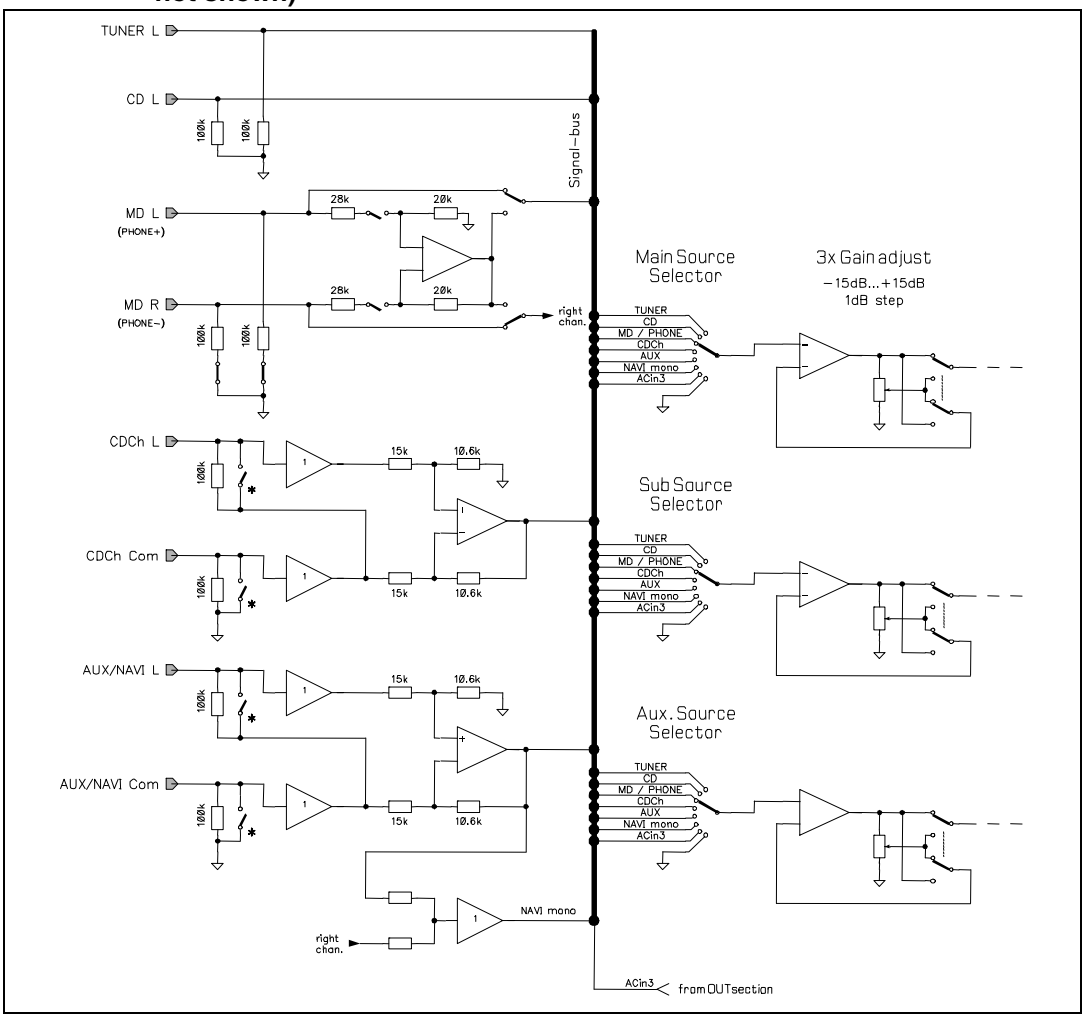
This chapter will give more insight into the different blocks and describe their function.

5.1 Input section

The Input-Section of the TDA7415CB incorporates three independent stereo signal paths, where each can connect to a variety of inputs and the AC3 input from the Output-section for monitoring purposes. For simplicity only the left inputs are shown.

After selection by the Main-, Sub-, and/or Auxiliary-source selector, the signal passes a gain-adjust amplifier, a soft-mute stage and finally a buffer before it is output at the device output-pins. The soft-mute circuit will be described later.

Figure 3. Signal-flow input-section (the following soft-mute and output buffer are not shown)



The CD-Changer- and Auxiliary/Navigation-inputs are quasi-differential inputs, where the 'out-of-phase' or ground signals of both channels share one common input. The Minidisk-input (MD) may be reconfigured for a true mono differential input as required by many phone units. Please note that all differential inputs dampen the signal by 3dB.

Additionally, each differential input-pin features a 'fast charge'-switch (*) allowing quickly charging external, large coupling capacitors upon power-on of the device. For normal operation, these switches **need to be released** by programming the corresponding bit.

For programming of the Input-section, see the programming chapter

5.2 Main signal processing path

The main-signal-processing path incorporates a classical three-band tone control (bass, mid and treble) that is preceded by a gain-adjust amplifier and completed by a dedicated room acoustics notch-filter (Room-EQ, see figure 1) that allows defeating the main car-body resonance.

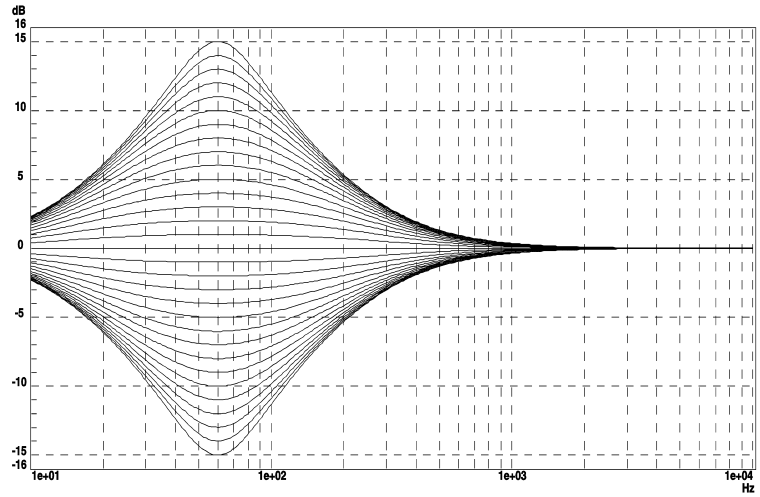
Hereafter, the filters composing the tone control and room-EQ will be presented.

5.2.1 Bass filter

There are four parameters programmable in the bass-filter stage.

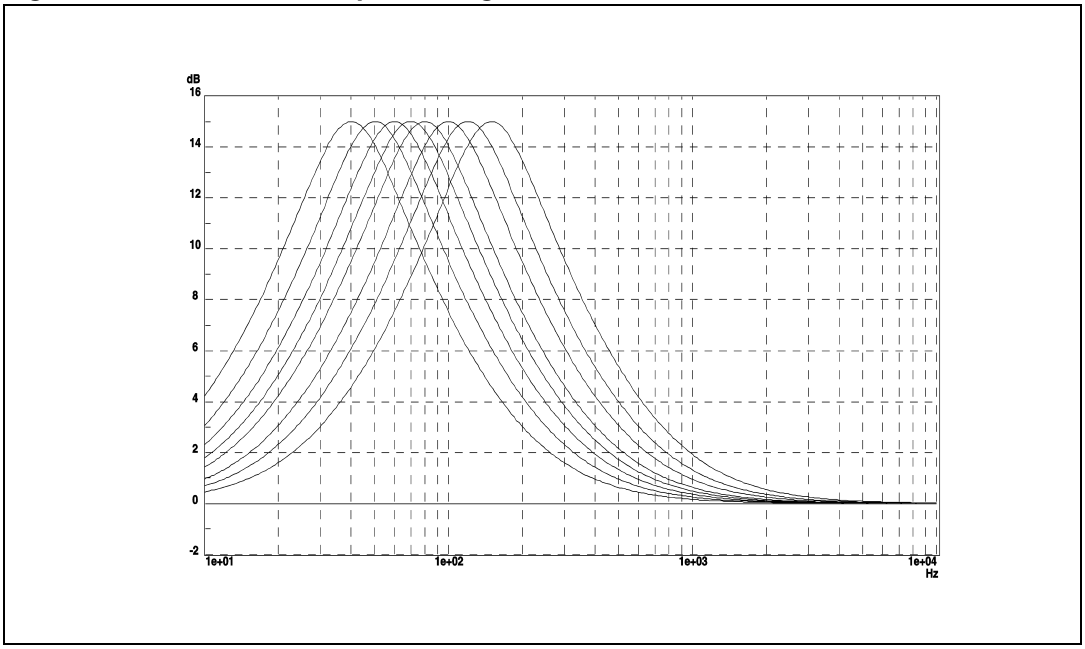
1. ***Control range:*** *Figure 4* shows the control range in the frequency domain at 60Hz center frequency.

Figure 4. Bass control range; f_C= 60Hz, Q= 1.0



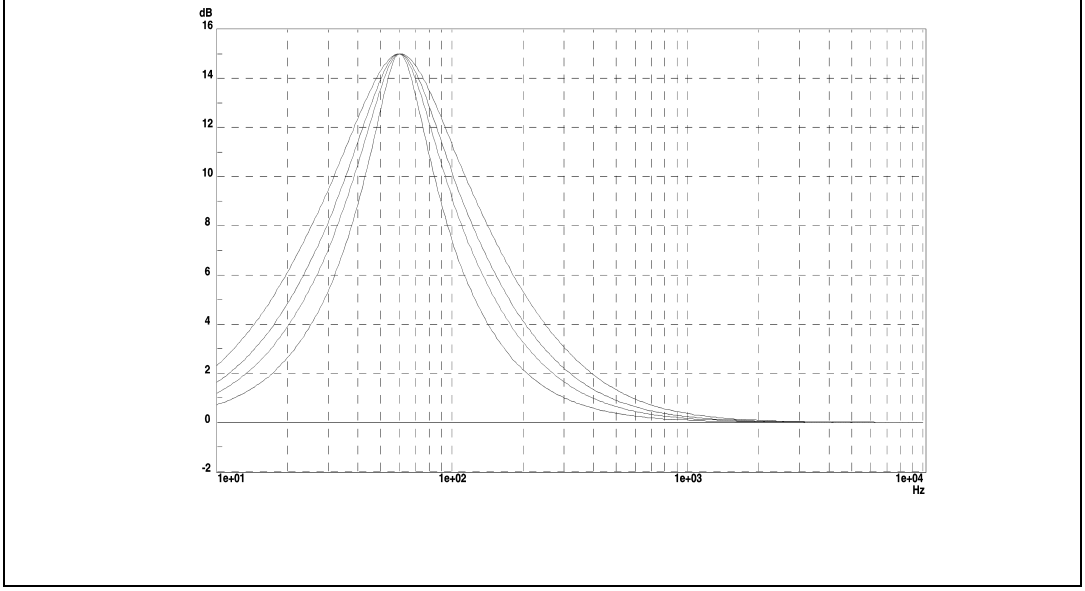
2. ***Center frequency:*** *Figure 5* shows all the selectable center frequencies at a gain of 15dB

Figure 5. Bass center frequencies; gain= 15dB, Q= 1.0



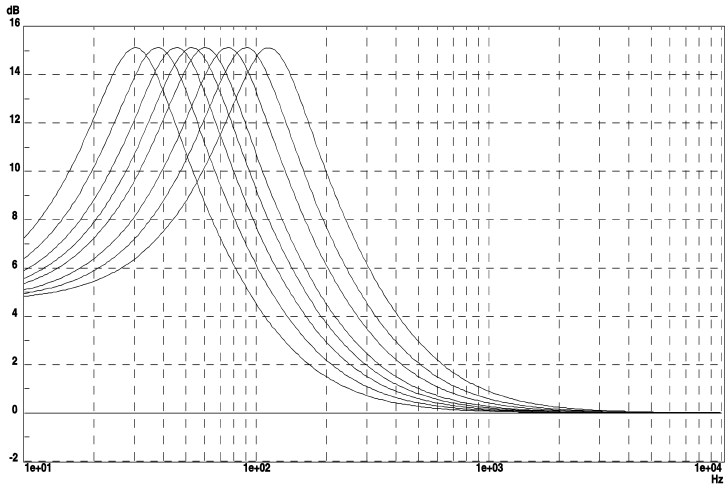
3. ***Quality factor:*** *Figure 6* shows the four selectable filter quality factors at a gain of 15dB

Figure 6. Bass filter quality factors; f_C= 60Hz, gain= 15dB.



4. ***DC-mode:*** *Figure 7* shows the effect of the DC-mode at a filter gain of 15dB. In this mode the DC-gain is increased by 4.4dB. In addition the programmed center frequencies and quality factors are decreased by 25%, which realizes alternative frequency responses.

Figure 7. Bass DC-mode frequency responses; gain= 15dB, Q= 1.5

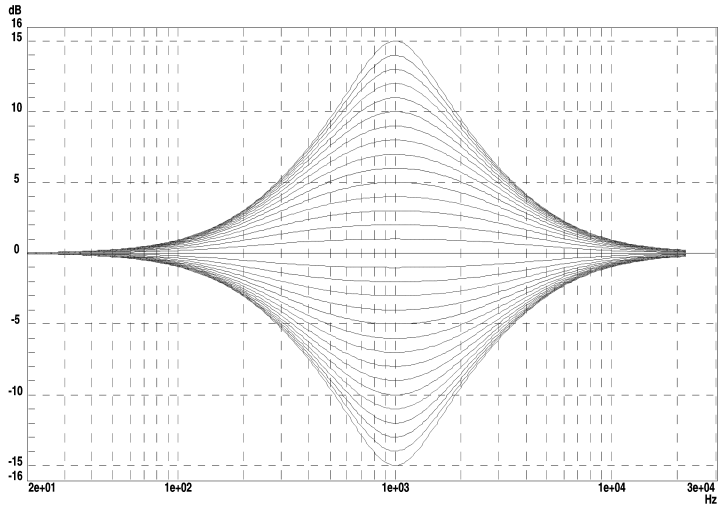


5.2.2 Mid filter

There are three parameters programmable in the mid-filter stage.

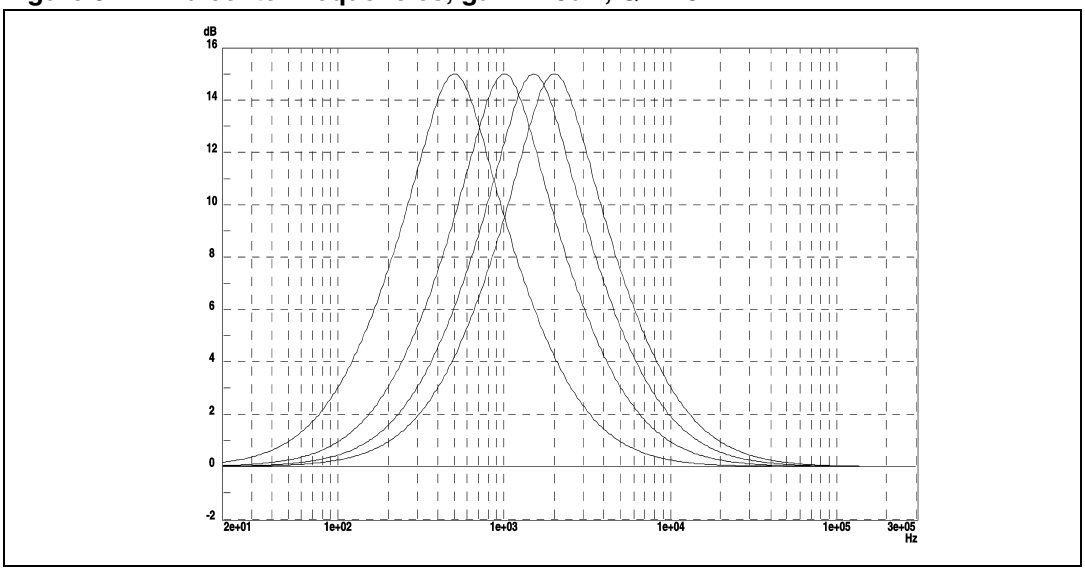
1. ***Control Range:*** *Figure 8* shows the control range in the frequency domain at 1kHz center frequency.

Figure 8. Mid control range; f_C= 1kHz, Q= 1.0



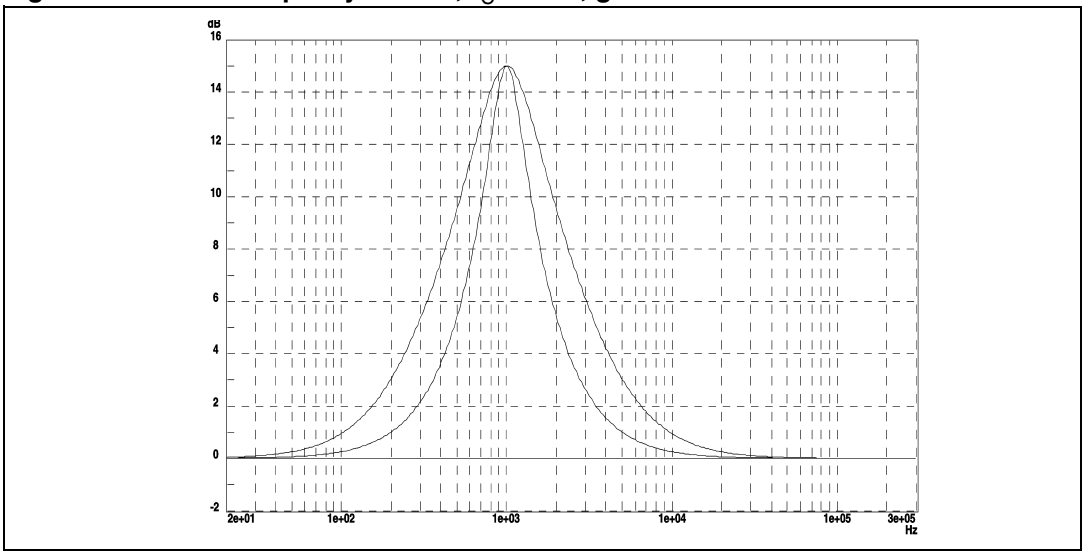
2. **Center frequency:** *Figure 9* shows the four selectable center frequencies at a gain of 15dB.

Figure 9. Mid center frequencies; gain= 15dB, Q= 1.0



3. ***Quality Factor:*** *Figure 10* shows the two selectable filter quality factors at a gain of 15dB.

Figure 10. Mid filter quality factors; f_C= 1kHz, gain= 15dB

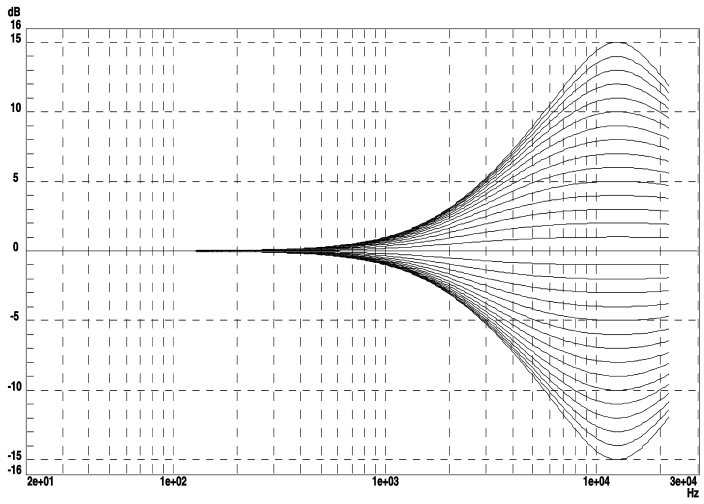


5.2.3 Treble filter

There are two parameters programmable in the treble-filter stage.

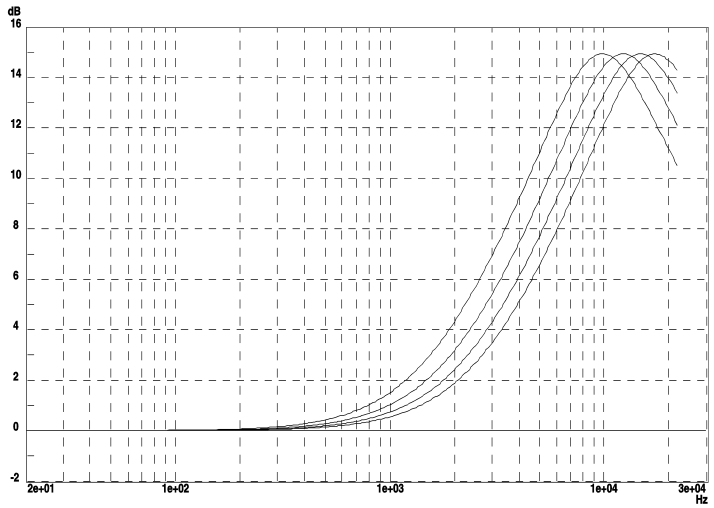
1. ***Control Range:*** *Figure 11* shows the control range in the frequency domain at 12.5kHz center frequency.

Figure 11. Treble control range; f_C= 12.5kHz, Q= 1.0



2. ***Center frequency:*** *Figure 12* shows the four selectable center frequencies at a gain of 15dB

Figure 12. Treble center frequencies; gain= 15dB, Q= 1.0

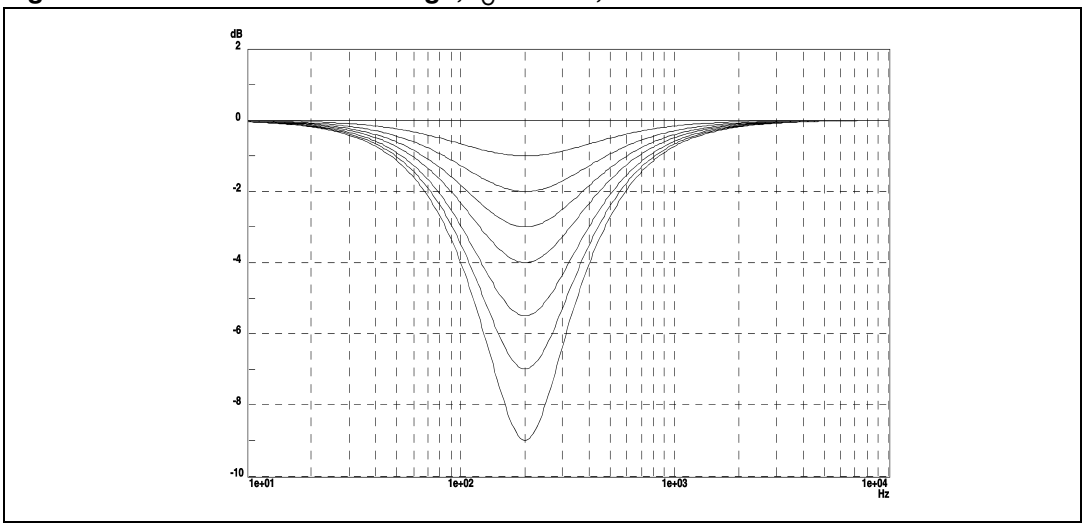


5.2.4 Room EQ filter

There are three parameters programmable in the room-EQ stage.

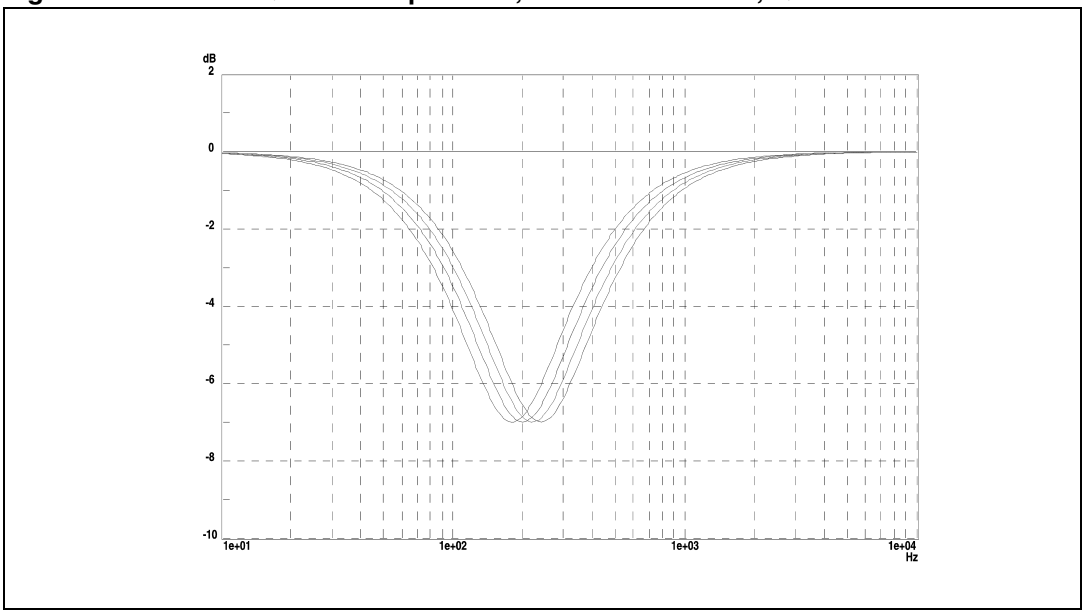
1. ***Control range:*** *Figure 13* shows the control range in the frequency domain at 200Hz center frequency. The filter has intentional non-uniform attenuation steps. These are 1dB, 2dB, 3dB, 4dB, 5.5dB, 7dB and 9dB.

Figure 13. Room-EQ control range; f_C= 200Hz, Q= 1.0



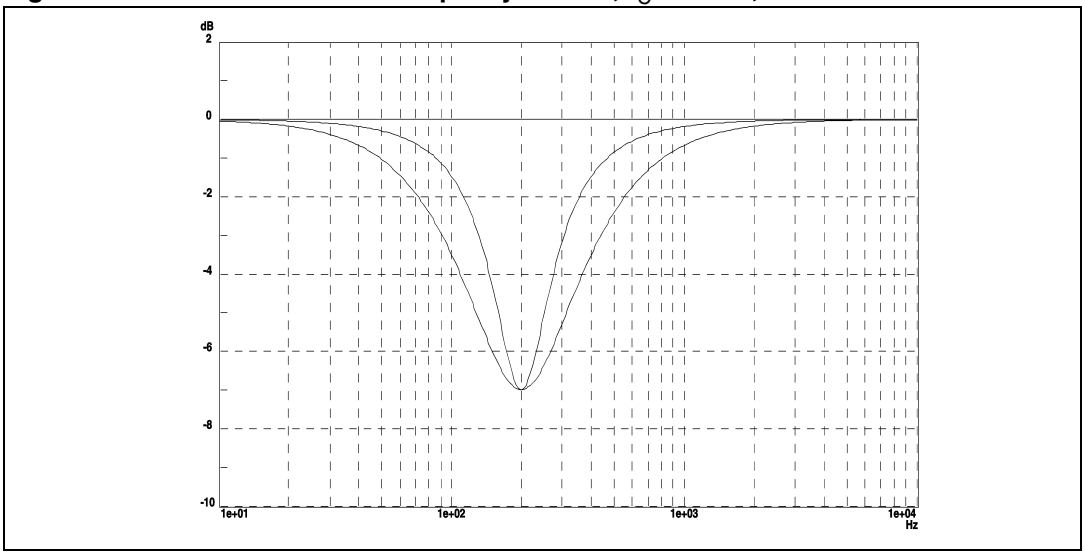
2. ***Notch frequency:*** *Figure 14* shows the four selectable notch frequencies at a gain of 15dB

Figure 14. Room-EQ notch frequencies; attenuation= -7dB, Q= 1.0.



3. ***Quality factor:*** *Figure 15* shows the two selectable filter quality factors at a gain of 15dB

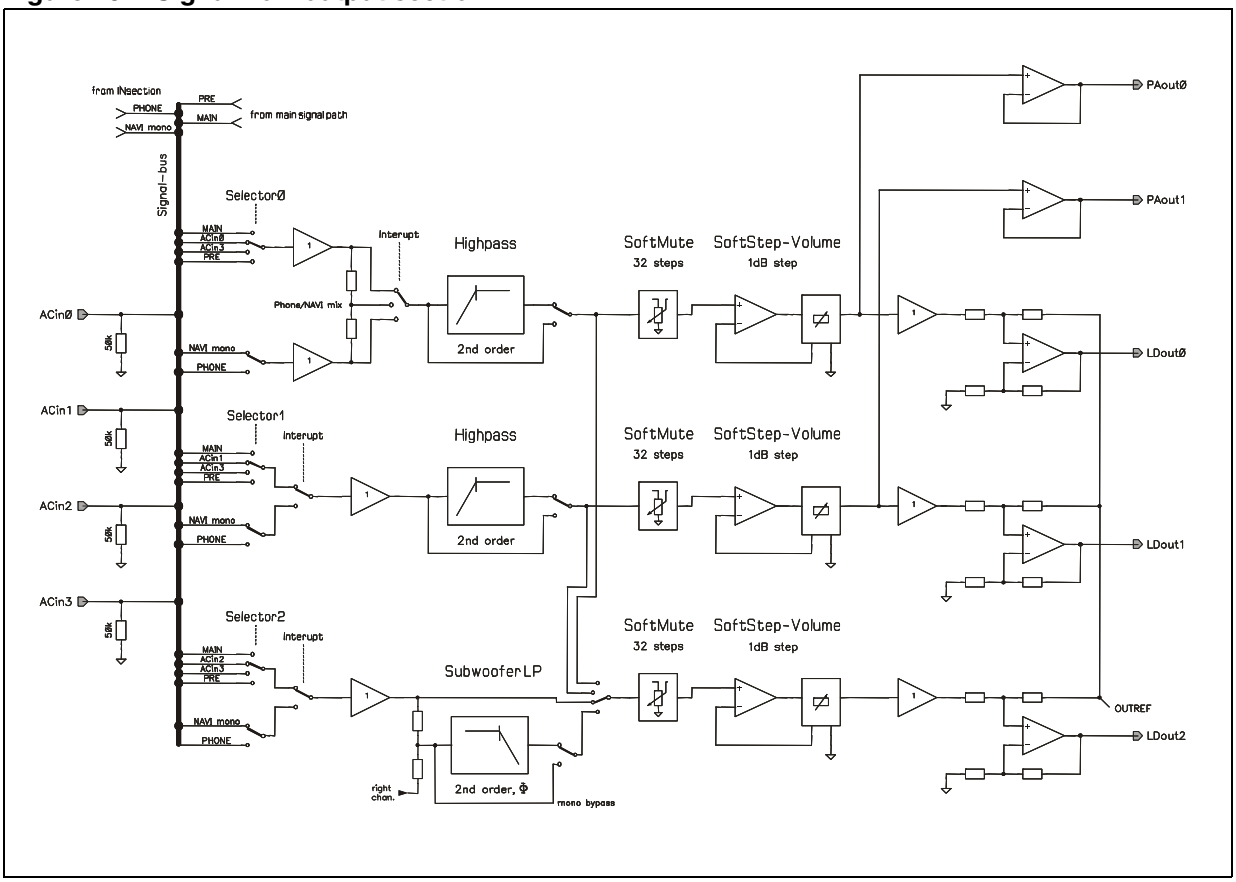
Figure 15. Room-EQ notch filter quality factors; f_C= 200Hz, attenuation= 7dB.



5.3 Output path

As the Input-Section, the Output-Section of the TDA7415CB incorporates also three independent stereo signal paths, where each can connect to two out of four AC-coupled, single-ended inputs and to some dedicated signals originating from the input-section and/or main-signal-path. For simplicity only one channel is shown in *Figure 16*. Interruption switches follow the input selectors that can quickly toggle to the phone-, navigation-, or phone/navigation-mix signal independently for each signal path and single L/R-channel. The pre-selection of the interrupt source is common for all signal paths.

Figure 16. Signal flow output section



Signal path 0 and 1 (front and rear) may optionally enter high-pass filters whereas signal path 2 (other) can be low-pass filtered for subwoofer applications. Anti-radiation filters are integrated for all signal paths but there are no anti-alias filters present at the inputs, since for most signal sources it is unlikely to introduce significant high frequency energy. However, if present, the system designer must take care to filter out high frequency components by means of an external RC-low-pass filter located at the AC-input pins. Soft-mute stages and a soft-step volume, that offer fast and click-less muting and/or volume changing follow all three filters. The soft mute circuit will be described later.

Five stereo pairs of output buffers finally complete the Output-section: Signal-path 2 exclusively feeds a line driver output that is capable of $4V_{RMS}$ output level as required by external (remote) power amplifiers. The other signal-paths 1 & 2 feature both, a line driver output and a dedicated internal (on board) power amplifier output with 3dB fixed gain. To maximize the line-driver output swing, when the dual-supply option (V_{CC} = 9V, V_P = 12V) is

not needed or available, the line-driver output stages may be programmed for lower gain, still delivering 2.75V_{RMS}.

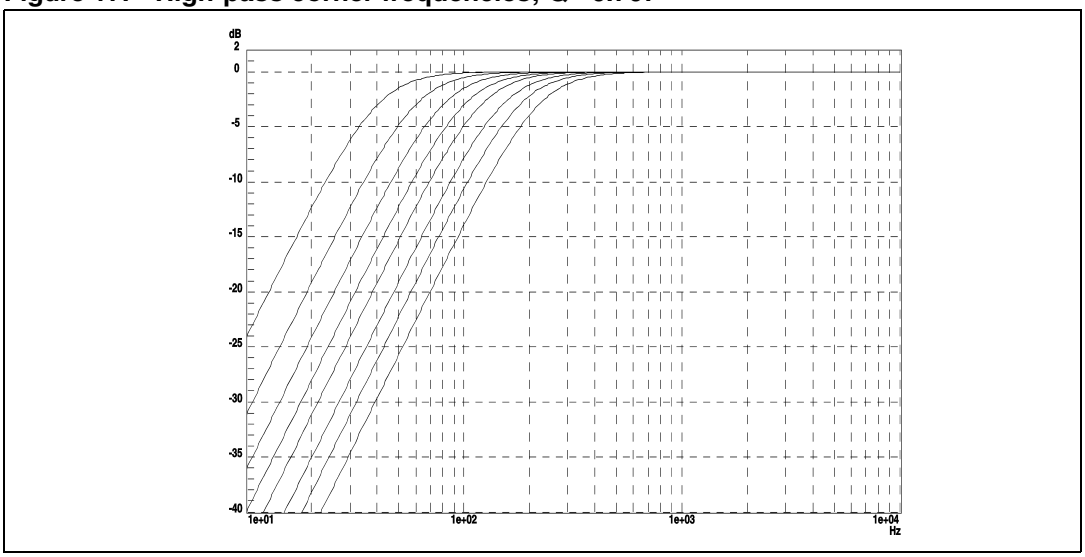
For programming of the Output-section, see the programming chapter

Hereafter, the different circuits composing the Output-section will be presented.

5.3.1 High pass filter

1. ***Corner frequency:*** *Figure 17* shows all the selectable corner frequencies for the high-pass filter

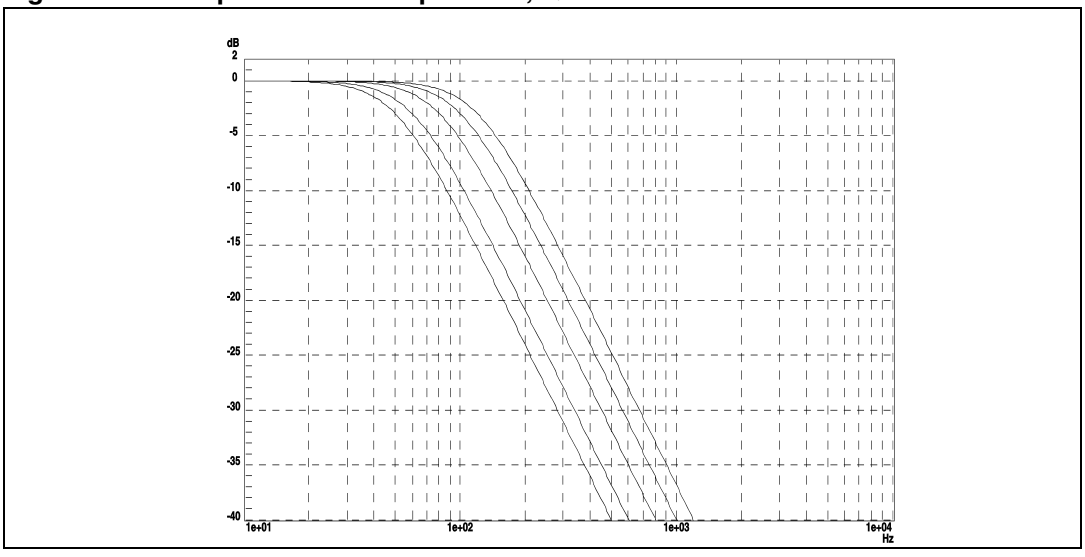
Figure 17. High-pass corner frequencies; Q= 0.707



5.3.2 Low pass (subwoofer) filter

1. ***Corner frequency:*** *Figure 18* shows all the selectable corner frequencies for the low-pass filter.

Figure 18. Low-pass corner frequencies; Q= 0.707

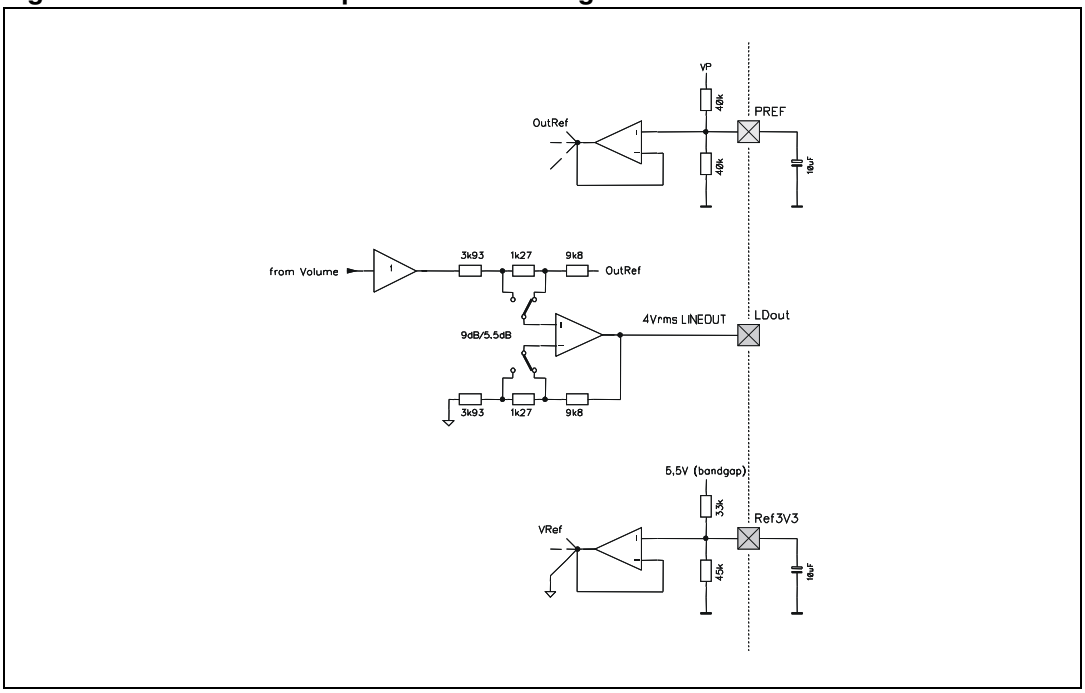


Remark: **Both filters offer a 'Butterworth' roll-off response**

5.3.3 Line driver output stage (presenting the reference concept)

In order to adapt to two different supply-voltages for the dual-supply option, while maintaining the highest possible output swing when only a single supply is available, the line-driver output was realized as differential amplifier biased around the two device references PREF and Vref3V3 (see *Figure 19*). The output DC-voltage precisely tracks the DC-voltage present at the PREF-pin that is half the VP-supply. However, forcing the PREF pin to any desired value could alter this DC-voltage, neglected the remaining output swing.

Figure 19. Line-driver output with reference generation scheme



In a dual-supply application (V_{CC} = 8.5V, V_P = 12V) the output gain should be set to 9dB to obtain a 4VRMS output level. For a single-supply application (V_{CC} =V_P = 8.5V) there is still an output level of 2.75V_{RMS} obtainable. Consequently, to avoid clipping in the output stages the gain needs to be reduced to 5.5dB. For the programming of the output gain, see the programming chapter.

Proper power sequencing is no critical issue for the TDA7415. However, it is recommended that both supply-voltages should follow each other within one diode forward-drop (<1V) before reaching their final value.

5.3.4 Soft mute

As can be seen from the block-diagram in figure 1, there are 6 soft-mute circuits placed inside the TDA7415CB: Three each, in both the Input-section and the Output-section that serve the independent signal-paths. A soft-mute can either be achieved by pulling one of the

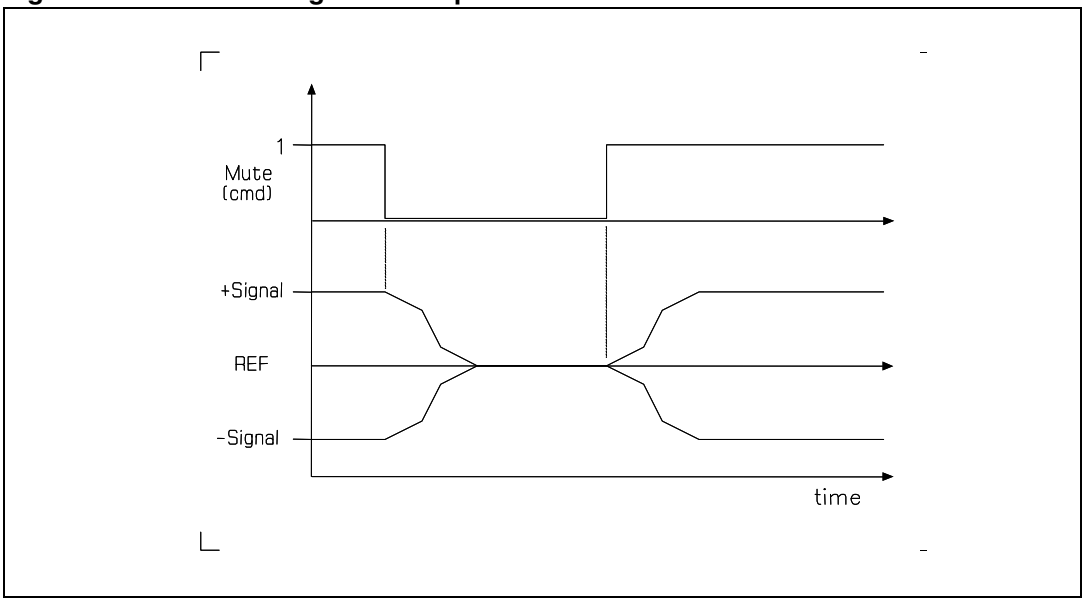
six soft-mute pins low (hardware-mute) or by assessing the corresponding programming bits (software-mute).

For the In-section, a soft-mute is always stereo for each of the three signal-paths and the bus-triggered mute exactly corresponds to the pin-triggered mute, with the exception that the later is inherently faster in response. This behavior is also true for the Out-section, but here the bus-triggered mute is independent for all six single L/R-channels.

All mute-pins have internal pull-ups connected to a 3,3Volts reference that allow the connection to either a 3,3V- or a 5V-microproccessor. Reverse flowing currents are limited to 100µA, so that the mute-pins may be driven by both, open-drain or push-pull outputs.

The envelope slope of the soft-mute was realized in a special S-shaped curve to soften the mute transitions in the critical regions (see *Figure 20*). The completion time for full mute / no mute is programmable by I^2C/SPI-bus in four different values.

Figure 20. Soft-mute signal envelope versus time



Note: A triggered mute is always completed and cannot be interrupted by a change of the initial mute condition.

For the programming of the soft-mute, see the programming chapter.

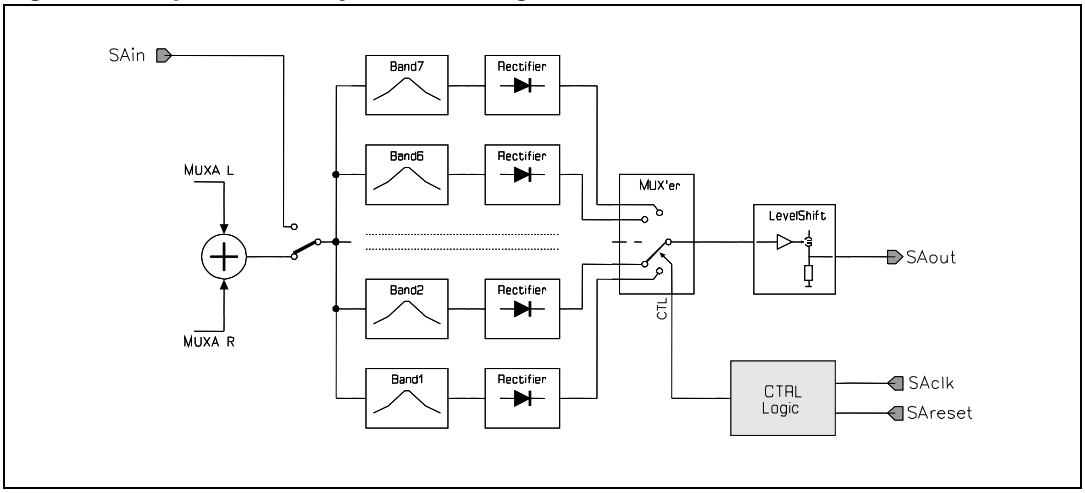
5.4 Spectrum analyzer

A fully integrated seven-band spectrum analyzer is present in the TDA7415CB (*Figure 21*).

The spectrum analyzer consists of seven band pass filters followed by rectifiers with sample capacitors that store the maximum peak signal level for each band since the last read cycle. This peak signal level can be read by a microprocessor at the SAout-pin. To allow easy interfacing to an analog input-port of a microprocessor, the output voltage at this pin is referred to device ground. Since the output voltage follows the peak level linearly, the microprocessor should take care for a logarithmic conversion (e.g. logarithmic look-up table).

The spectrum analyzer's input signal is either the mono-sum of the stereo MUXA-output or alternatively a signal input at the SAin-pin. In order to have some influence on the visual behavior in a given application the filter quality for all band-pass filters may be programmed for two different qualities, with the higher filter quality creating a faster, more differentiating optical response. If the spectrum analyzer is disabled both, the SAres- and the SAclk-pin should be tied to ground.

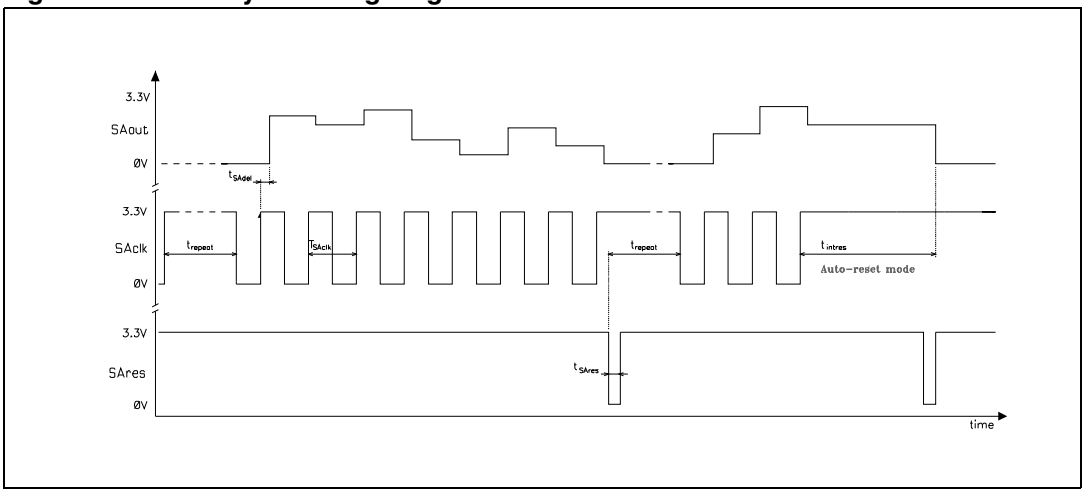
Figure 21. Spectrum analyzer block diagram



The microprocessor starts a read cycle with a negative going clock edge at the SAclk input. On the following positive clock edges, the stored peak signal level of the band pass filters is subsequently switched to SAout. Each analog output value is valid after the time t_{SAdel}. A reset of the sample capacitors is triggered by either pulling the SAres-pin low any time or by setting-up the spectrum-analyzer for Auto-reset mode. Although not shown in *Figure 22*, for the Auto-reset mode a reset is generated whenever SAclk remains high for the time t_{intres}.

Note that a proper auto-reset requires the clock signal SAclk to be held at high potential and that the reset is not repetitive. Once a reset was triggered, a new read-out cycle should not be initiated before the time t_{repeat} has passed. This allows sufficient settling of the filters. *Figure 22* illustrates the read cycle timing of the spectrum analyzer.

Figure 22. Read cycle timing diagram



5.5 DC offset detector

Using the DC offset detection circuit (figure 22) an offset voltage difference between the audio power amplifier and theTDA7415CB's PA-outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the TDA7415CB. The WinIn-input has an internal pull-up resistor connected to 5,5Volts. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC0/1-pins are implemented, with external capacitors introducing the same delay $\tau = 5k\Omega * Cext$ as the AC-coupling between the TDA7415 and the power amplifier introduces. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

For electrical characteristics see page 8.

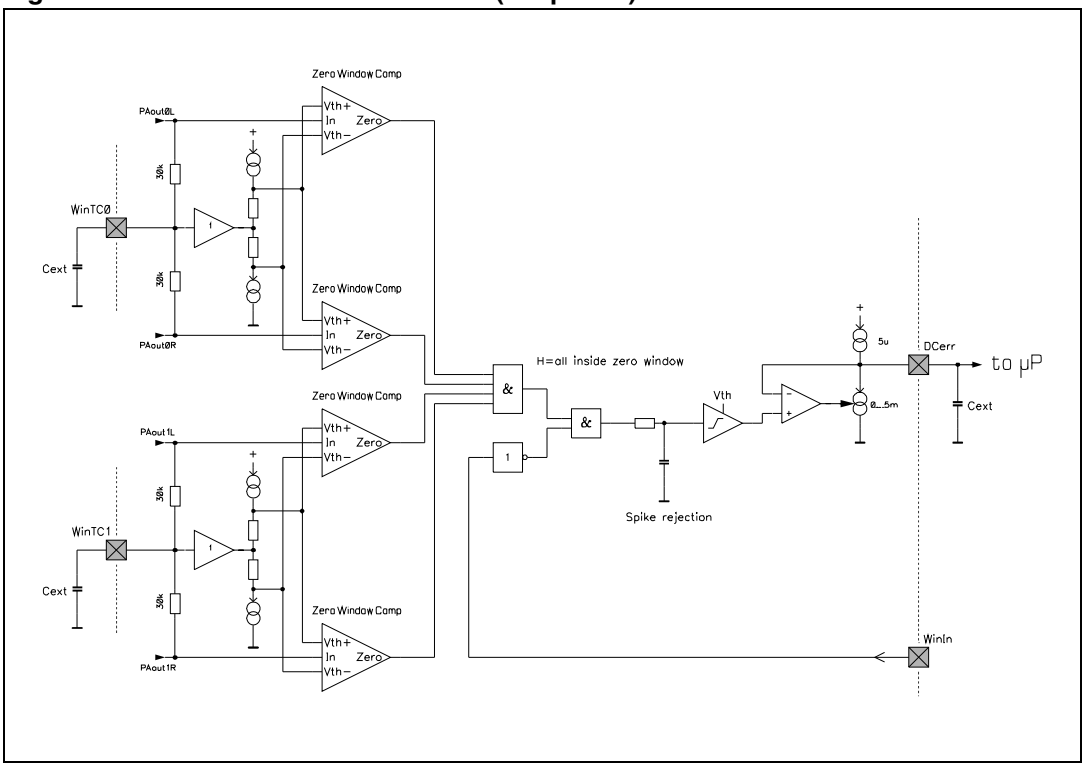
A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

a) All PA-outputs (front and rear) are inside zero crossing windows.

b) The Input voltage VWinIn is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication. The fast mode has to be turned off by a manual release of the fast-charge

Figure 23. DC-offset detection circuit (simplified)



6 Digital interface

The TDA7415CB digital interface supports two different protocols: SPI and I^2C. To select the I^2C-mode the SEL-pin has to be tied to the system supply by means of a 68k -resistor. If the voltage at the SEL-pin falls below 5.5V, the interface switches to SPI-mode. Consequently, the interface is able to work with a microprocessor either supplied by a 3.3V or a 5V power supply. The SPI-mode has to be set and remain static before the device leaves the reset state caused by power-on reset (POR).

For details of both protocols refer to the programming section.

6.1 Interface in SPI -mode

- Interface protocol

The SPI interface protocol comprises:

  – A sub-address (SAx) and

A sequence of n data bytes (Dy); each consisting of 8 bits.

A negative going edge at SEL enables the interface receiving data. The interface accepts both a positive (Cpol=1, Cpha=1; SPI-mode 0) as well as a negative (Cpol=0, Cpha=0; SPI-mode 3) clocking scheme. However, the data transmitted has to be valid on the **rising edges** of the serial clock SCL.

Figure 24. Switching characteristics (SPI-mode):

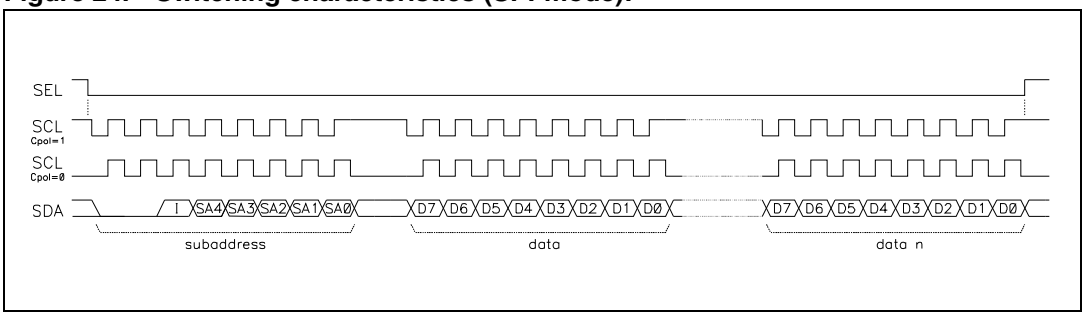


Figure 25. Interface in SPI -mode diagram

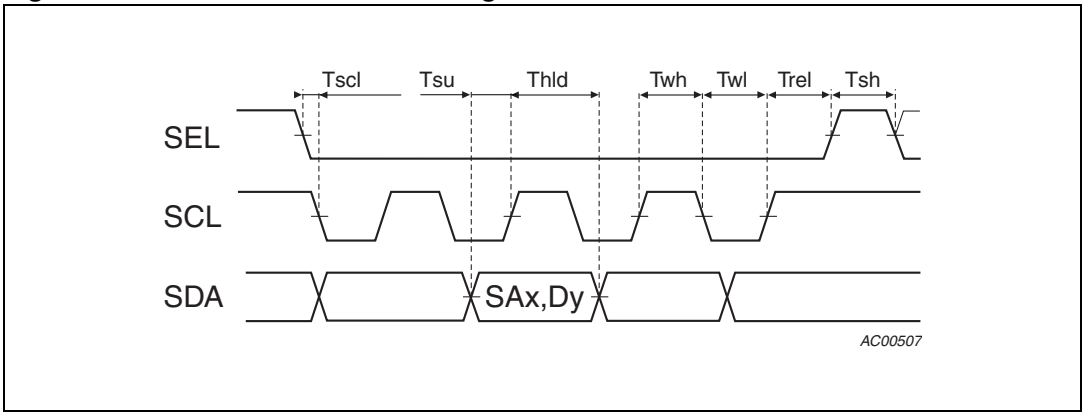


Table 12. Interface in SPI -mode

Symbol	Parameter	Min	Typ	Max	Units
f_{SCLK}	Serial input clock frequency (SCL)	0,00	-	4	MHz
T_{su}	Serial data setup time	40,00	-	-	ns
T_{hld}	Serial data hold time	40,00	-	-	ns
T_{wh}	Serial clock high time width	100,00	-	-	ns
T_{wl}	Serial clock low time width	100,00	-	-	ns
T_{scl}	Select (SEL) to clock (SCL) falling setup time	200,00	-	-	ns
T_{rel}	Clock (SCL) to select (SEL) rising release time	200,00	-	-	ns
t_r	Data rise time	-	-	2,00	µs
t_f	Data fall time	-	-	2,00	µs
T_{sh}	Chip select high time	200,00	-	-	µs

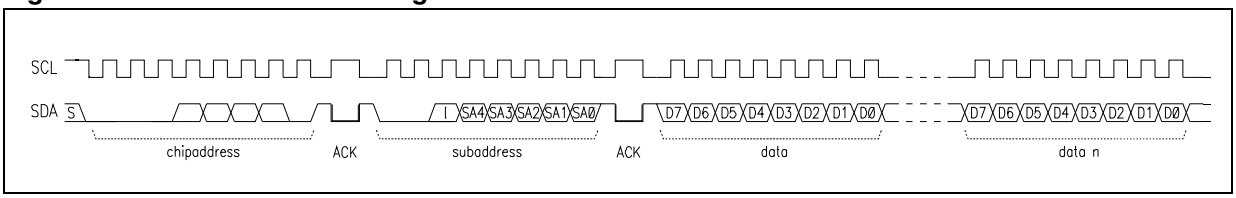
6.2 I²C bus interface description

- Interface Protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read / write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 26. I²C bus interface diagram



S = Start

ACK = Acknowledge

Auto increment

If bit I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled which is also true for the SPI mode.

Chip-address

For the TDA7415CB the chip address is **$8C** (10001100).

Reset condition

A power-on reset (POR) is generated whenever the supply voltage falls below 4.5V. After that, the following data is written automatically into all sub-address registers:

MSB							LSB
1	1	1	1	1	1	1	0

The programming after POR is marked bold face / underlined in the programming tables.

7 Programming

Table 13. Subaddress allocation (receive mode)

MSB							LSB	Description	Byte (dec)
I_2	I_1	I_0	A_4	A_3	A_2	A_1	A_0		
0	-	-	-	-	-	-		Unassigned	-
-	0 1	-	-	-	-	-	-	**Test Mode** off on	-
-	-	0 1	-	-	-	-	-	**Auto Increment Mode** off on	-
-	-	-	0	0	0	0	0	Main signal path input gain adjust	0
			0	0	0	0	1	Main signal path Bass-filter settings I	1
			0	0	0	1	0	Main signal path Bass-filter settings II	2
			0	0	0	1	1	Main signal path Mid-filter settings	3
			0	0	1	0	0	Main signal path Treble-filter settings	4
			0	0	1	0	1	Main signal path Room-EQ settings	5
			0	0	1	1	0	Input section, path A input select & gain adjust	6
			0	0	1	1	1	Input section, path B input select & gain adjust	7
			0	1	0	0	0	Input section, path C input select & gain adjust	8
			0	1	0	0	1	Global Input section settings; Bus contr. mutes	9
			0	1	0	1	0	Output section, path 0 input select & interrupt	10
			0	1	0	1	1	Output section, path 1&2 input select & interrupt	11
			0	1	1	0	0	f_C-select high-pass filter signal path 0&1	12
			0	1	1	0	1	Output section, path 0 left channel Volume	13
			0	1	1	1	0	Output section, path 0 right channel Volume	14
			0	1	1	1	1	Output section, path 1 left channel Volume	15
			1	0	0	0	0	Output section, path 1 right channel Volume	16
			1	0	0	0	1	f_C-select subwoofer filter, path 2 monitor select	17
			1	0	0	1	0	Output section, path 2 left channel Volume	18
			1	0	0	1	1	Output section, path 2 right channel Volume	19
			1	0	1	0	0	Output section, Bus-controlled mutes	20
			1	0	1	0	1	Dc-detector settings; PA-mutes; Linedriver gain	21
			1	0	1	1	0	Softstep & Softmute fade-times	22
			1	0	1	1	1	Spectrum-analyzer settings	23
			1	1	0	0	0	----------	24
			…	…	…	…	…	Unassigned	
			1	1	1	1	0	----------	30
			1	1	1	1	1	Test multiplexer; device clocking	31

7.1 Data byte specification

The status after power-on reset is marked bold face / underlined in the programming tables.

Table 14. Main signal path input (addr. 00)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Input gain adjust level
			0	0	0	0	0	–15dB
			0	0	0	0	1	–14dB
			0	:	:	:	:	…
			0	1	1	1	0	–1dB
-	-	-	0	1	1	1	1	–0dB
			1	1	1	1	1	+0dB
			1	1	1	1	0	+1dB
			1	:	:	:	:	…
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
1	1	1	-	-	-	-	-	**Unused**, do not alter

Table 15. Main signal path, bass-filter (addr. 01)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Level
				0	0	0	0	0dB
				0	0	0	1	1dB
-	-	-	-	:	:	:	:	:
				1	1	1	0	14dB
				1	1	1	1	15dB
								Boost / Cut
-	-	-	0	-	-	-	-	Boost
			1					Cut
								Soft-step
-	-	0	-	-	-	-	-	On
		1						Off
								Quality factor
0	0							1.00
0	1	-	-	-	-	-	-	1.25
1	0							1.50
1	1							2.00

Table 16. Main signal path, bass-filter (addr. 02)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	1	1	1	0	**Unused**, do not alter
-	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	-	-	-	-	Center frequency 150Hz 120Hz 100Hz 80Hz 70Hz 60Hz 50Hz 40Hz
0 1	-	-	-	-	-	-	-	DC-mode Off On

Table 17. Main signal path, mid-filter (addr. 03)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	**Level** 15dB 14dB : 1dB 0dB
-	-	-	0 1	-	-	-	-	**Boost / Cut** Cut Boost
-	0 0 1 1	0 1 0 1	-	-	-	-	-	**Center frequency** 500Hz 1.0kHz 1.5kHz 2.0kHz
0 1	-	-	-	-	-	-	-	**Quality factor** 1.0 2.0

Table 18. Main signal path, treble-filter (addr. 04)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-					**Level**
				0	0	0	0	15dB
				0	0	0	1	14dB
				:	:	:	:	:
				1	1	1	0	1dB
				1	1	1	1	0dB
-	-	-	0	-	-	-	-	**Boost / Cut**
			1					Cut
								Boost
-			-	-	-	-	-	**Center frequency**
	0	0						10kHz
	0	1						12.5kHz
	1	0						15kHz
	1	1						17.5KHz
1	-	-	-	-	-	-	-	**Unused**, do not alter

Table 19. Main signal path, room-EQ (addr. 05)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	1	0	**Unused**, do not alter
-	-	-				-	-	**Attenuation level**
			0	0	0			9dB
			0	0	1			7dB
			0	1	0			5.5dB
			0	1	1			4dB
			1	0	0			3dB
			1	0	1			2dB
			1	1	0			1dB
			1	1	1			0dB
-			-	-	-	-	-	**Center frequency**
	0	0						240Hz
	0	1						220Hz
	1	0						200Hz
	1	1						180Hz
								Quality factor
0	-	-	-	-	-	-		1.0
1								2.0

Table 20. Input section, signal paths A-C (addr. 06-08)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Input gain adjust level
			0	0	0	0	0	–15dB
			0	0	0	0	1	–14dB
			0	:	:	:	:	…
			0	1	1	1	0	–1dB
-	-	-	0	1	1	1	1	–0dB
			1	1	1	1	1	+0dB
			1	1	1	1	0	+1dB
			1	:	:	:	:	…
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								Input select
0	0	0						Tuner
0	0	1						CD
0	1	0						MD / Phone
0	1	1	-	-	-	-	-	CD-Changer (quasi-differential)
1	0	0						AUX./Navigation (quasi-differential)
1	0	1						Navigation (mono-Mix)
1	1	0						AC3in-monitor (from OUT-section)
1	1	1						Full mute

Table 21. Input section; other settings (addr. 09)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-							0	**Unused**, do not alter
								Soft-mute, signal path A
-	-	-	-	-	-	0	-	No mute
						1		Mute
								Soft-mute, signal path B
-	-	-	-	-	0	-	-	No mute
					1			Mute
								Soft-mute, signal path C
-	-	-	-	0	-	-	-	No mute
				1				Mute
-		1	1	-	-	-	-	**Unused**, do not alter
								MD-mode
-	0	-	-	-	-	-	-	Single ended, stereo (e.g. Minidisk)
	1							Full differential, mono (e.g. external Phone)
								Fast-charge (quasi-differential inputs)
0	-	-	-	-	-	-	-	Release
1								Engage

Table 22. Output section, signal path 0 (addr. 10)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Input select
						0	0	Main signal path Output select
-	-	-	-	-	-	0	1	AC0in
						1	0	AC3in
						1	1	Main signal path PRE-Tone select
								Interrupts select, right channel
				0	0			Not allowed
-	-	-	-	0	1	-	-	Interrupt enable
				1	0			Interrupt, 50% signal mix
				1	1			Interrupt bypass, normal operation
								Interrupts select, left channel
		0	0					Not allowed
-	-	0	1	-	-	-	-	Interrupt enable
		1	0					Interrupt, 50% signal mix
		1	1					Interrupt bypass, normal operation
-	1	-	-	-	-	-	-	**Unused**, do not alter
								Interrupt Pre-select (common for all paths)
0	-	-	-	-	-	-	-	Navigation
1								Phone

Table 23. Output section, signal path 1 and 2 (addr. 11)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Input select signal path1
						0	0	Main signal path Output select
-	-	-	-	-	-	0	1	AC1in
						1	0	AC3in
						1	1	Main signal path PRE-Tone select
								Interrupts select, right channel signal path 1
-	-	-	-	-	0	-	-	Interrupt enable
					1			Interrupt bypass, normal operation
								Interrupts select, left channel signal path 1
-	-	-	-	0	-	-	-	Interrupt enable
				1				Interrupt bypass, normal operation
								Input select signal path2
		0	0					Main signal path Output select
-	-	0	1	-	-	-	-	AC2in
		1	0					AC3in
		1	1					Main signal path PRE-Tone select
								Interrupts select, right channel signal path 2
-	0	-	-	-	-	-	-	Interrupt enable
	1							Interrupt bypass, normal operation
								Interrupts select, left channel signal path 2
0	-	-	-	-	-	-	-	Interrupt enable
1								Interrupt bypass, normal operation

Table 24. Output section, high-pass filters (addr. 12)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Corner frequency, High-pass signal path 0
					0	0	0	40 Hz
					0	0	1	60 Hz
					0	1	0	80 Hz
-	-	-	-	-	0	1	1	100 Hz
					1	0	0	120 Hz
					1	0	1	150 Hz
					1	1	0	180 Hz
					1	1	1	220 Hz
-	-	-	-	0	-	-	-	**Bypass**, High-pass signal path 0
				1				Filter bypass
								Filter insert
								Corner frequency, High-pass signal path 1
	0	0	0					40 Hz
	0	0	1					60 Hz
	0	1	0					80 Hz
-	0	1	1	-	-	-	-	100 Hz
	1	0	0					120 Hz
	1	0	1					150 Hz
	1	1	0					180 Hz
	1	1	1					220 Hz
								Bypass, High-pass signal path 1
0	-	-	-	-	-	-	-	Filter bypass
1								Filter insert

Table 25. Output section, volume 0L, 0R, 1L, 1R, 2L, 2R (addr. 13-16, 18, 19)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	-	**Volume level**
-	0	0	0	1	1 : 0	1 : 1	1 : 0	Not allowed
-	0	0	0	1 1 : 0 0	0 0 : 0 0	0 0 : 0 0	1 0 : 1 0	+25 dB +24 dB … +17 dB +16 dB
-	0	0	1	1 1 : 0 0	1 1 : 0 0	1 1 : 0 0	1 0 : 1 0	+15 dB +14 dB … +1 dB +0 dB
-	0	1	0	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	–0 dB –1 dB … –14 dB –15 dB
-	0	1	1	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	–16 dB –17 dB … –30 dB –31 dB
-	1	0	0	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	–32 dB –33 dB … –46 dB –47 dB
-	1	0	1	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	–48 dB –49 dB … –62 dB –63 dB
-	1	1	0	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	–64 dB –65 dB … –78 dB –79 dB
-	1	1	1	X	X	X	X	**Mute**
0 1	-	-	-	-	-	-	-	**Soft-step** On Off

Table 26. Output section, subwoofer low-pass filter (addr. 17)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0	**Unused**, do not alter
-	-	-	-	X X 0 1 X	0 0 1 1 1	0 1 0 0 1	-	**Monitor select** Signal path 0 (before Soft-mute) Signal path 1 (before Soft-mute) Low-pass filter (Subwoofer enable) Mono-sum bypass Stereo bypass (direct through)
-	0 0 0 0 1 1	0 0 1 1 X 1	0 1 0 1 X 1	-	-	-	-	**Corner frequency** 120 Hz 100 Hz 80 Hz 60 Hz 50 Hz 50 Hz
0 1	-	-	-	-	-	-	-	**Phase** No shift Inverted

Table 27. Output section, bus-mutes (addr. 20)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0	**Unused**, do not alter
-	-	-	-	-	-	0 1	-	**Soft-mute, right channel signal path 0** No mute Mute
-	-	-	-	-	0 1	-	-	**Soft-mute, left channel signal path 0** No mute Mute
-	-	-	-	0 1	-	-	-	**Soft-mute, right channel signal path 1** No mute Mute
-	-	-	0 1	-	-	-	-	**Soft-mute, left channel signal path 1** No mute Mute
-	-	0 1	-	-	-	-	-	**Soft-mute, right channel signal path 2** No mute Mute
-	0 1	-	-	-	-	-	-	**Soft-mute, left channel signal path 2** No mute Mute
1	-	-	-	-	-	-	-	**Unused**, do not alter

Table 28. DC-detector and other output section settings (addr. 21)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**Line drivers gain** 9dB 5.5dB
-	-	-	-	-	-	0 1	-	**PAout0 (front) mute** No mute Mute
-	-	-	-	-	0 1	-	-	**PAout1 (rear) mute** No mute Mute
-	-	-	-	0 1	-	-	-	**DCError output behavior** Forced high level by mute; (1) Normal operation, see description *Chapter 5.5*.
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Zero-comparator Window size** ± 100mV ± 75mV ± 50mV ± 25mV
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**Spike rejection time constant** 11µs 22µs 33µs 44µs

1. DCError output high for OUTsection signal paths 1&2 muted **or** all PAout muted

Table 29. Soft-mute and soft-step fader time (addr. 22)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	1	1	1	0	**Unused**, do not alter
-	-	-	-	0 1	-	-	-	**Input selection prcedure** Soft-mute completion time programmed according to bits D6 and D7 Soft-mute completion time fixed to 0.5ms
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Soft-step completion time** 0.32ms 0.64ms 1.28ms 2.56ms
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**Soft-mute completion time** 0.25ms 0.5ms 10ms 5ms

Table 30. Spectrum analyzer settings (addr. 23)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**Run/stop** (internal clocking) Stop Run
-	-	-	-	-	-	0 1	-	**Filter quality** High Low
-	-	-	-	-	0 1	-	-	**Reset mode** SAres-pin triggered reset Auto-reset mode
-	-	-	-	0 1	-	-	-	**Source select** Mono-sum of MUXA-outputs SAin-pin
1	1	1	1	-	-	-	-	**Unused,** do not alter

Table 31. Testing * (addr. 31)

MSB							LSB	Function	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
-	-	-	-	-	-	-	0 1	**Device clock** Enable internal clock generation Allow external clocking in *fast-mode*	
-	-	-	-	1	1	1	-	**Unused**, do not alter	
-	-	-	-	-	-	-	-	**Test selector**	
-	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	-	-	-	-	**TUNER L out:** DCDet., lower TC-Vth Spec.Anal. 60Hz-bandpass Spec.Anal. 160Hz-bandpass Spec.Anal. 400Hz-bandpass Spec.Anal. 1kHz-bandpass Spec.Anal. 2,5kHz-bandpass Spec.Anal. 6,3kHz-bandpass Spec.Anal. 16kHz-bandpass	**TUNER R out:** DCDet., upper TC-Vth 5,5V CMOS-supply DCDet., time constant 200kHz reference clock actual Soft-Mute clock actual Soft-Step clock SC-reference, left chan. DC-Offset monitor point
0 1	-	-	-	-	-	-	-	**Test mode** Enabled * Disabled	

Successfully entering the test-mode requires to set bit D6 of the sub address (test mode-bit) to "1". In test-mode, the TUNER L&R inputs are reconfigured as output for the selected test signals

Note: This byte is used for testing and/or evaluation purposes only and must not be set to other values than the default "11111110" in the application.

8 Application information

Figure 27. Typical application connections diagram

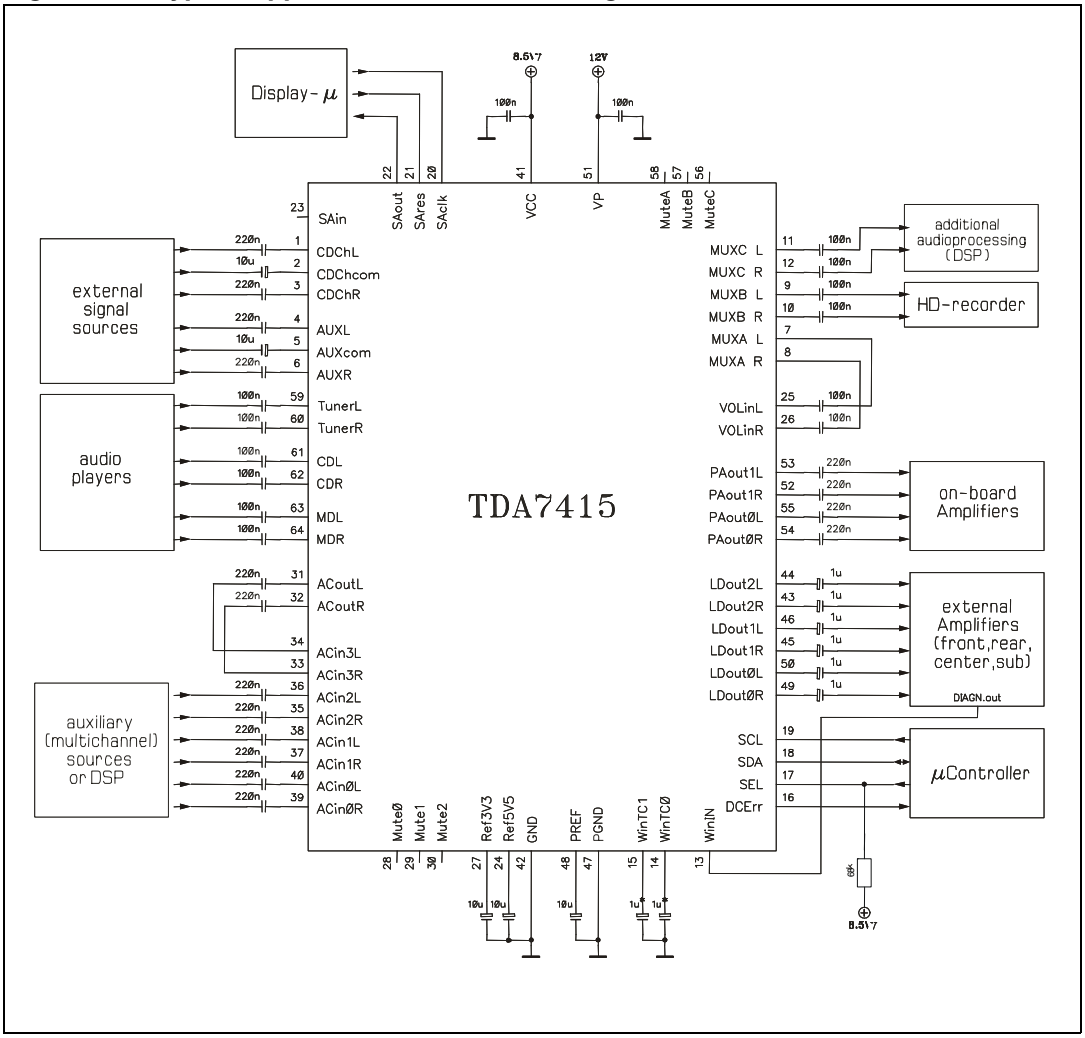


Figure 27 shows a proposal for a typical application. - However, the figure only represents one possible interconnection scheme with other devices (The shaded blocks could represent a complex digital sound reproducing/processing system). For simplicity, this proposal assumes the system designer not to take advantage from the direct muting feature and therefore let the corresponding Mute-pins floating.

All capacitor values are suggestions with their dimensioning still being dependant on girdling impedances. This is especially true for the capacitors located at the WinTC-pins as can be read in chapter 6.5. **In case the DC-detector function is not assessed in the application it is recommended to short both the WinTC-pins 14 and 15 to device-ground.**

9 Package information

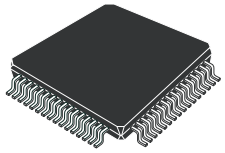
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

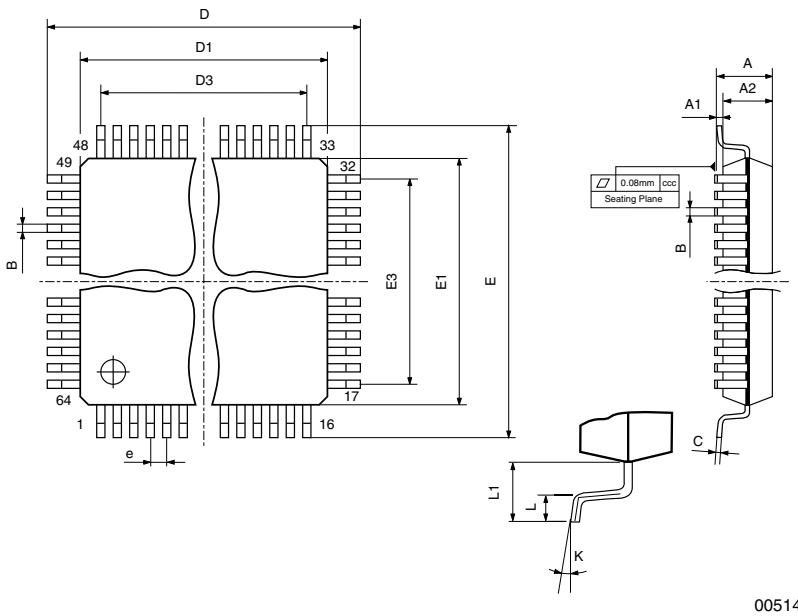
Figure 28. LQFP64 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09			0.0035		
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (typ.), 7° (max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)



10 Revision history

Table 32. Document revision history

Date	Revision	Changes
26-Oct-2007	1	Initial release.
24-Nov-2008	2	Updated the *Table 8: Output section on page 15*.
24-Jun-2009	3	Updated *Figure 28: LQFP64 mechanical data and package dimensions on page 48*.
24-Sep-2013	4	Updated disclaimer.

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