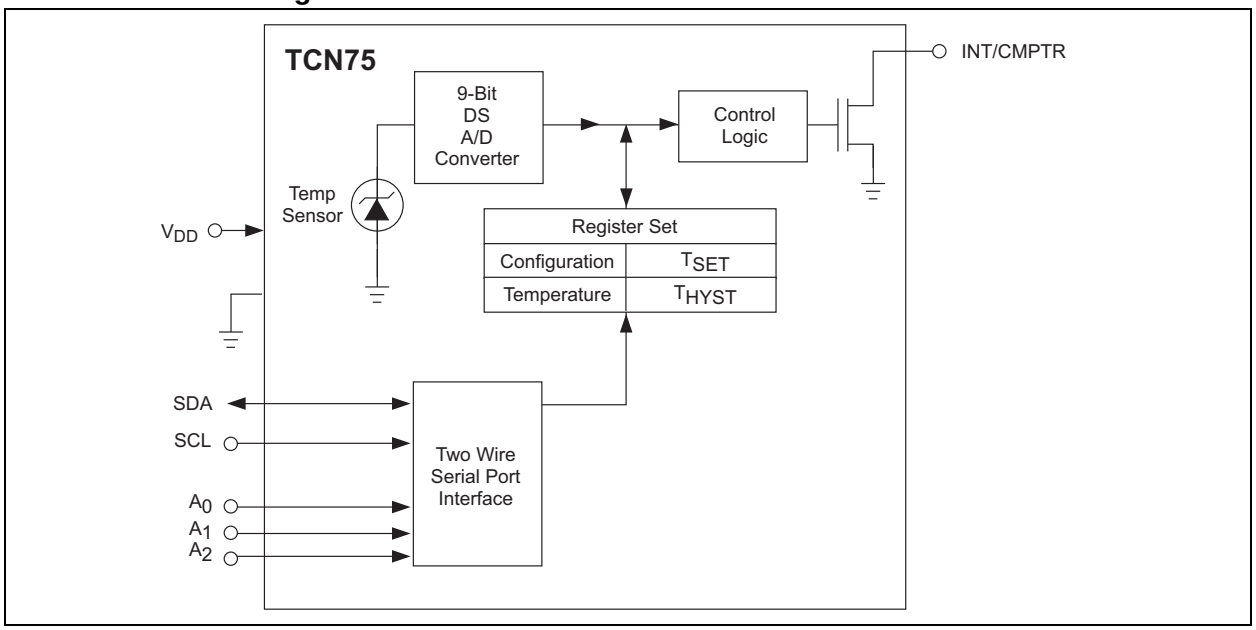
Device Selection Table

Part Number	Supply Voltage	Package	Junction Temperature Range
TCN75-3.3MOA	3.3	8-Pin SOIC	-55°C to +125°C
TCN75-5.0MOA	5.0	8-Pin SOIC	-55°C to +125°C
TCN75-3.3MUA	3.3	8-Pin MSOP	-55°C to +125°C
TCN75-5.0MUA	5.0	8-PIn MSOP	-55°C to +125°C

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V_{DD}) 6.0V

ESD Susceptibility **(Note 3)** 1000V

Voltage on Pins:
A0, A1, A2 ..... (GND – 0.3V) to (V_{DD} + 0.3V)

Voltage on Pins:
SDA, SCL, INT/CMPTR .. (GND – 0.3V) to 5.5V

Thermal Resistance (Junction to Ambient)
8-Pin SOIC ..... 170°C/W
8-Pin MSOP ..... 250°C//W

Operating Temperature Range (T_J): -55°C to +125°C

Storage Temperature Range (T_{STG}): -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TCN75 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = 2.7V – 5.5V, -55°C ≤ (T_A = T_J) ≤ 125°C, unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Power Supply						
V_{DD}	Power Supply Voltage	2.7	—	5.5	—	
I_{DD}	Operating Current	— —	0.250 —	— 1.0	mA	Serial Port Inactive (T_A = T_J = 25°C) Serial Port Active
I_{DD1}	Standby Supply Current	—	1	—	µA	Shutdown Mode, Serial Port Inactive (T_A = T_J = 25°C)
INT/CMPTR Output						
I_{OL}	Sink Current: INT/CMPTR, SDA Outputs	—	1	4	mA	**Note 1**
t_{TRIP}	INT/CMPTR Response Time	1	—	6	t_{CONV}	User Programmable
V_{OL}	Output Low Voltage	—	—	0.8	V	I_{OL} = 4.0 mA
Temp-to-Bits Converter						
ΔT	Temperature Accuracy **(Note 2)**	—	±3	—	°C	-55°C ≤ T_A ≤ +125°C
						V_{DD} = 3.3V: TCN75-3.3 MOA, TCN75-3.3 MUA V_{DD} = 5.0V: TCN75-5.0 MOA, TCN75-5.0 MUA
		—	±0.5	±3	°C	25°C ≤ T_A ≤ 100°C
t_{CONV}	Conversion Time	—	55	—	msec	
$T_{SET(PU)}$	TEMP Default Value	—	80	—	°C	Power-up
$T_{HYST(PU)}$	T_{HYST} Default Value	—	75	—	°C	Power-up
2-Wire Serial Bus Interface						
V_{IH}	Logic Input High	V_{DD} x 0.7	—	—	V	
V_{IL}	Logic Input Low	—	—	V_{DD} x 0.3	V	
V_{OL}	Logic Output Low	—	—	0.4	V	I_{OL} = 3 mA
C_{IN}	Input Capacitance SDA, SCL	—	15	—	pF	
I_{LEAK}	I/O Leakage	—	±100	—	pA	(T_A = T_J = 25°C)
$I_{OL(SDA)}$	SDA Output Low Current	—	—	6	mA	

TCN75 ELECTRICAL SPECIFICATIONS (CONTINUED)

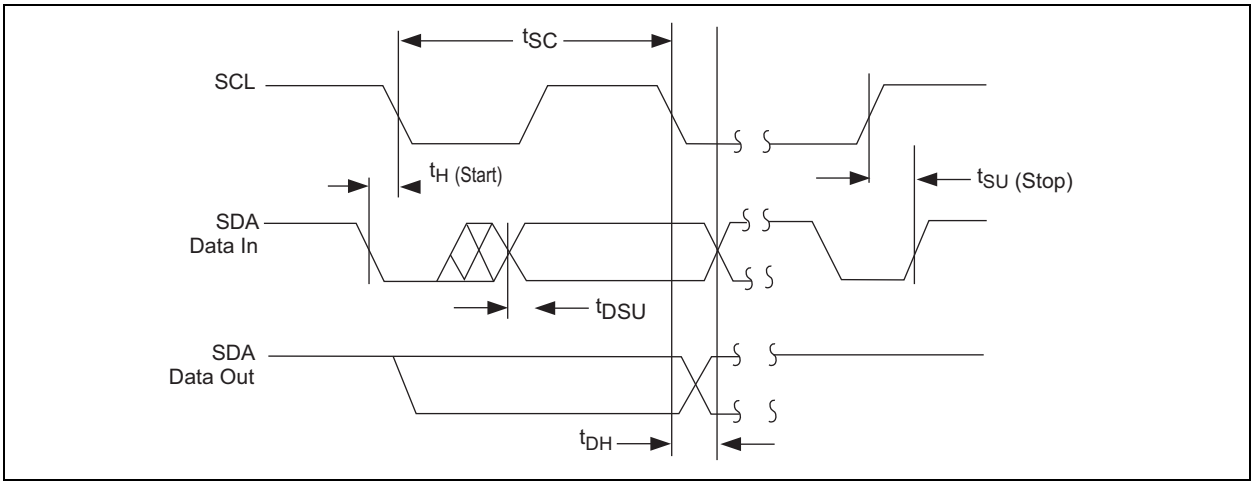
Electrical Characteristics: 2.7V ≤ V_{DD} ≤ 5.5V; -55°C ≤ (T_A = T_J) ≤ 125°C, C_L = 80 pF, unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Serial Port Timing						
f_{SC}	Serial Port Frequency	0	100	400	kHz	
t_{LOW}	Low Clock Period	1250	—	—	nsec	
t_{HIGH}	High Clock Period	1250	—	—	nsec	
t_R	SCL and SDA Rise Time	—	—	250	nsec	
t_F	SCL and SDA Fall Time	—	—	250	nsec	
$t_{SU(START)}$	Start Condition Setup Time (for repeated Start Condition)	1250	—	—	nsec	
t_{SC}	SCL Clock Period	2.5	—	—	µsec	
$t_{H(START)}$	Start Condition Hold Time	100	—	—	nsec	
t_{DSU}	Data in Setup Time to SCL High	100	—	—	nsec	
t_{DH}	Data in Hold Time after SCL Low	0	—	—	nsec	
$t_{SU(STOP)}$	Stop Condition Setup Time	100	—	—	nsec	
t_{IDLE}	Bus Free Time Prior to New Transition	1250	—	—	nsec	

Note 1: Output current should be minimized for best temperature accuracy. Power dissipation within the TCN75 will cause self-heating and temperature drift. At maximum rated output current and saturation voltage, 4 mA and 0.8V, respectively, the error amounts to 0.544°C for the SOIC.

2: All part types of the TCN75 will operate properly over the wider power supply range of 2.7V to 5.5V. Each part type is tested and specified for rated accuracy at its nominal supply voltage. As V_{DD} varies from the nominal value, accuracy will degrade 1°C/V of V_{DD} change.

3: Human body model, 100 pF discharged through a 1.5k resistor.

TIMING DIAGRAM



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (8-Pin SOIC) 8-Pin MSOP)	Symbol	Description
1	SDA	Bidirectional Serial Data.
2	SCL	Serial Data Clock Input.
3	INT/CMPTR	Interrupt or Comparator Output.
4	GND	System Ground.
5	A_2	Address Select Pin (MSB).
6	A_1	Address Select Pin.
7	A_0	Address Select Pin (LSB).
8	V_{DD}	Power Supply Input.

3.0 DETAILED DESCRIPTION

A typical TCN75 hardware connection is shown in Figure 3-1.

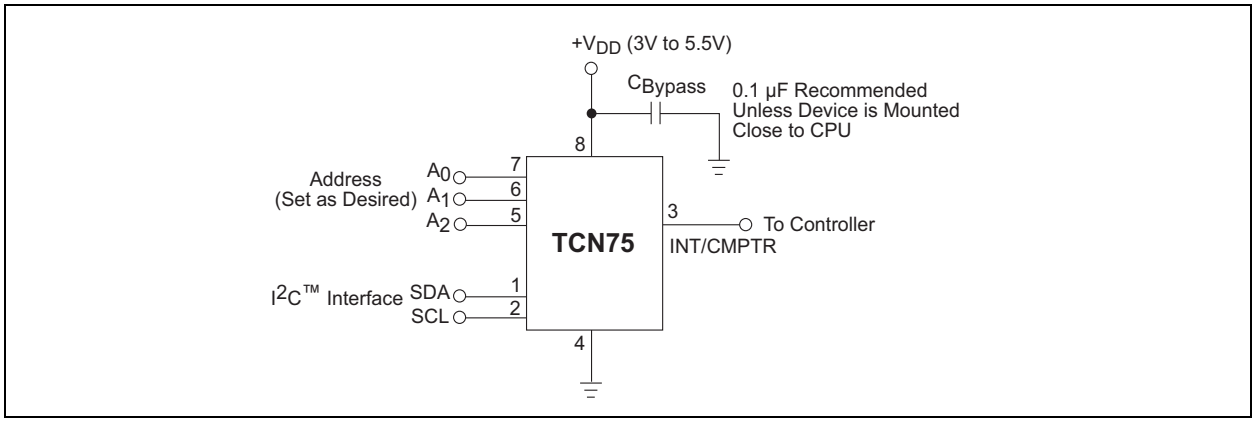


FIGURE 3-1: *Typical Application*

3.1 Serial Data (SDA)

Bidirectional. Serial data is transferred in both directions using this pin.

3.2 Serial Clock (SCL)

Input. Clocks data into and out of the TCN75.

3.3 INT/CMPTR

Open Collector, Programmable Polarity. In Comparator mode, unconditionally driven active any time temperature exceeds the value programmed into the T_{SET} register. INT/CMPTR will become inactive when temperature subsequently falls below the T_{HYST} setting. (See **Section 5.0 "Register Set and Programmer's ModeL"**, Register Set and Programmer's Model). In Interrupt mode, INT/CMPTR is also made active by TEMP exceeding T_{SET}; it is unconditionally reset to its inactive state by reading any register via the 2-wire bus. If and when temperature falls below T_{HYST}, INT/CMPTR is again driven active. Reading any register will clear the T_{HYST} interrupt. In Interrupt mode, the INT/CMPTR output is unconditionally reset upon entering Shutdown mode. If programmed as an active-low output, it can be wire-ORed with any number of other open collector devices. Most systems will require a pull-up resistor for this configuration.

Note that current sourced from the pull-up resistor causes power dissipation and may cause internal heating of the TCN75. To avoid affecting the accuracy of ambient temperature readings, the pull-up resistor should be made as large as possible. INT/CMPTR's output polarity may be programmed by writing to the INT/CMPTR POLARITY bit in the CONFIG register. The default is active low.

3.4 Address (A2, A1, A0)

Inputs. Sets the three Least Significant bits of the TCN75 8-bit address. A match between the TCN75's address and the address specified in the serial bit stream must be made to initiate communication with the TCN75. Many protocol-compatible devices with other addresses may share the same 2-wire bus.

3.5 Slave Address

The four Most Significant bits of the Address Byte (A6, A5, A4, A3) are fixed to 1001[B]. The states of A2, A1 and A0 in the serial bit stream must match the states of the A2, A1 and A0 address inputs for the TCN75 to respond with an Acknowledge (indicating the TCN75 is on the bus and ready to accept data). The Slave Address is represented in Table 3-1.

TABLE 3-1: TCN75 SLAVE ADDRESS

1	0	0	1	A2	A1	A0
MSB						LSBS

3.6 Comparator/Interrupt Modes

INT/CMPTR behaves differently depending on whether the TCN75 is in Comparator mode or Interrupt mode. Comparator mode is designed for simple thermostatic operation. INT/CMPTR will go active anytime TEMP exceeds T_{SET}. When in Comparator mode, INT/CMPTR will remain active until TEMP falls below T_{HYST}, whereupon it will reset to its inactive state. The state of INT/CMPTR is maintained in Shutdown mode when the TCN75 is in Comparator mode. In Interrupt mode, INT/CMPTR will remain active indefinitely, even if TEMP falls below T_{HYST}, until any register is read via the 2-wire bus. Interrupt mode is better suited to interrupt driven microprocessor-based systems. The INT/CMPTR output may be wire-OR'ed with other interrupt sources in such systems. Note that a pull-up resistor is necessary on this pin since it is an open-drain output. Entering Shutdown mode will unconditionally reset INT/CMPTR when in Interrupt mode.

4.0 SHUTDOWN MODE

When the appropriate bit is set in the configuration register (CONFIG) the TCN75 enters its low-power Shutdown mode (I_{DD} = 1 μA, typical) and the temperature-to-digital conversion process is halted. The TCN75's bus interface remains active and TEMP, T_{SET}, and T_{HYST} may be read from and written to. Transitions on SDA or SCL due to external bus activity may increase the standby power consumption. If the TCN75 is in Interrupt mode, the state of INT/CMPTR will be reset upon entering Shutdown mode.

4.1 Fault Queue

To lessen the probability of spurious activation of INT/CMPTR the TCN75 may be programmed to filter out transient events. This is done by programming the desired value into the Fault Queue. Logic inside the TCN75 will prevent the device from triggering INT/CMPTR unless the programmed number of sequential temperature-to-digital conversions yield the same qualitative result. In other words, the value reported in TEMP must remain above T_{SET} or below T_{HYST} for the consecutive number of cycles programmed in the Fault Queue. Up to a six-cycle "filter" may be selected. See **Section 5.0 "Register Set and Programmer's ModeL"**, Register Set and Programmer's Model.

4.2 Serial Port Operation

The Serial Clock input (SCL) and bidirectional data port (SDA) form a 2-wire bidirectional serial port for programming and interrogating the TCN75. The following table indicates TCN75 conventions that are used in this bus scheme.

TABLE 4-1: SERIAL BUS CONVENTIONS

Term	Explanation
Transmitter	The device sending data to the bus.
Receiver	The device receiving data from the bus.
Master	The device which controls the bus: initiating transfers (Start), generating the clock, and terminating transfers (Stop).
Slave	The device addressed by the master.
Start	A unique condition signaling the beginning of a transfer indicated by SDA falling (High – Low) while SCL is high.
Stop	A unique condition signaling the end of a transfer indicated by SDA rising (Low – High) while SCL is high.
ACK	A Receiver acknowledges the receipt of each byte with this unique condition. The Receiver drives SDA low during SCL high of the ACK clock-pulse. The Master provides the clock pulse for the ACK cycle.
NOT Busy	When the bus is idle, both SDA & SCL will remain high.
Data Valid	The state of SDA must remain stable during the High period of SCL in order for a data bit to be considered valid. SDA only changes state while SCL is low during normal data transfers. (See Start and Stop conditions).

All transfers take place under control of a host, usually a CPU or microcontroller, acting as the Master, which provides the clock signal for all transfers. The TCN75 *always* operates as a Slave. This serial protocol is illustrated in Figure 5-1. All data transfers have two phases; and all bytes are transferred MSB first. Accesses are initiated by a Start condition, followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a Stop condition. A convention called Acknowledge (ACK) confirms receipt of each byte. Note that SDA can change only during periods when SCL is LOW (SDA changes while SCL is HIGH are reserved for Start and Stop conditions).

4.3 Start Condition (Start)

The TCN75 continuously monitors the SDA and SCL lines for a Start condition (a HIGH-to-LOW transition of SDA while SCL is HIGH), and will not respond until this condition is met.

4.3.1 ADDRESS BYTE

Immediately following the Start condition, the host must next transmit the address byte to the TCN75. The four Most Significant bits of the Address Byte (A6, A5, A4, A3) are fixed to 1001(B). The states of A2, A1 and A0 in the serial bit stream must match the states of the A2, A1 and A0 address inputs for the TCN75 to respond with an Acknowledge (indicating the TCN75 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read/Write Bit. This bit is a '1' for a read operation or '0' for a write operation.

4.3.2 ACKNOWLEDGE (ACK)

Acknowledge (ACK) provides a positive handshake between the host and the TCN75. The host releases SDA after transmitting eight bits then generates a ninth clock cycle to allow the TCN75 to pull the SDA line LOW to acknowledge that it successfully received the previous eight bits of data or address.

4.3.3 DATA BYTE

After a successful ACK of the address byte, the host must next transmit the data byte to be written or clock out the data to be read. (See the appropriate timing diagrams.) ACK will be generated after a successful write of a data byte into the TCN75.

4.3.4 STOP CONDITION (STOP)

Communications must be terminated by a Stop condition (a LOW-to-HIGH transition of SDA while SCL is HIGH). The Stop condition must be communicated by the transmitter to the TCN75.

4.3.5 POWER SUPPLY

To minimize temperature measurement error, the TCN75-3.3 MOA and TCN75-3.3 MUA are factory calibrated at a supply voltage of 3.3V ±5% and the TCN75-5.0 MOA and TCN75-5.0 MUA are factory calibrated at a supply voltage of 5V ±5%. Either device is fully operational over the power supply voltage range of 2.7V to 5.5V, but with a lower measurement accuracy. The typical value of this power supply-related error is ±2°C.

5.0 REGISTER SET AND PROGRAMMER'S MODEL

TABLE 5-1: REGISTER (POINT), 8 BITS, WRITE ONLY

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Must Be Set To Zero						Pointer	

Register Selection Via the Pointer Register		
D1	**D0**	**Register Selection**
0	0	TEMP
0	1	CONFIG
1	0	T_{HYST}
1	1	T_{SET}

TABLE 5-2: CONFIGURATION REGISTER (CONFIG), 8 BITS, READ/ WRITE

D [7]	D [6]	D [5]	D [4]	D [3]	D [2]	D [1]	D [0]
Must Be Set To Zero			Fault Queue		INT/ CMPTR, Polarity	COMP/INT	Shut-down

D0: Shutdown:

0 = Normal Operation

1 = Shutdown Mode

D1: CMPTR/INT:

0 = Comparator Mode

1 = Interrupt Mode

D2: INT/CMPTR POLARITY:

0 = Active Low

1 = Active High

D3 – D4: Fault Queue: Number of sequential temperature-to-digital conversions with the same result before the INT/CMPTR output is updated:

D4	D3	Number of Conversions
0	0	1 (Power-up default)
0	1	2
1	0	4
1	1	6

TABLE 5-3: TEMPERATURE (TEMP) REGISTER, 16 BITS, READ ONLY

The binary value in this register represents ambient temperature following a conversion cycle.

D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	D7	D6	D5	D4	D3	D2	D1	LSB	X	X	X	X	X	X	X

TABLE 5-4: TEMPERATURE SET POINT (T_{SET}) REGISTER, 16 BITS, READ/WRITE

D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	D7	D6	D5	D4	D3	D2	D1	LSB	X	X	X	X	X	X	X

TABLE 5-5: HYSTERESIS (T_{HYST}) REGISTER, 16 BITS, READ/WRITE

D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	D7	D6	D5	D4	D3	D2	D1	LSB	X	X	X	X	X	X	X

In the TEMP, T_{SET}, and T_{HYST} registers, each unit value represents one-half degree (Celsius). The value is in 2's – complement binary format such that a reading of 000000000b corresponds to 0°C. Examples of this temperature to binary value relationship are shown in Table 5-6.

TABLE 5-6: TEMPERATURE TO DIGITAL VALUE CONVERSION

Temperature	Binary Value	HEX Value
+125°C	0 11111010	0FA
+25°C	0 00110010	032
+0.5°C	0 00000001	001
0°C	0 00000000	00
0.5°C	1 11111111	1FF
-25°C	1 11001110	1CE
-40°C	1 10110000	1B0
-55°C	1 10010010	192

TABLE 5-7: TCN75'S REGISTER SET SUMMARY

Name	Description	Width	Read	Write	Notes
TEMP	Ambient Temperature	16	X		2's Complement Format
TSET	Temperature Setpoint	16	X	X	2's Complement Format
T_{HYST}	Temperature Hysteresis	16	X	X	2's Complement Format
POINT	Register Pointer	8	X	X	
CONFIG	Configuration Register	8	X	X	

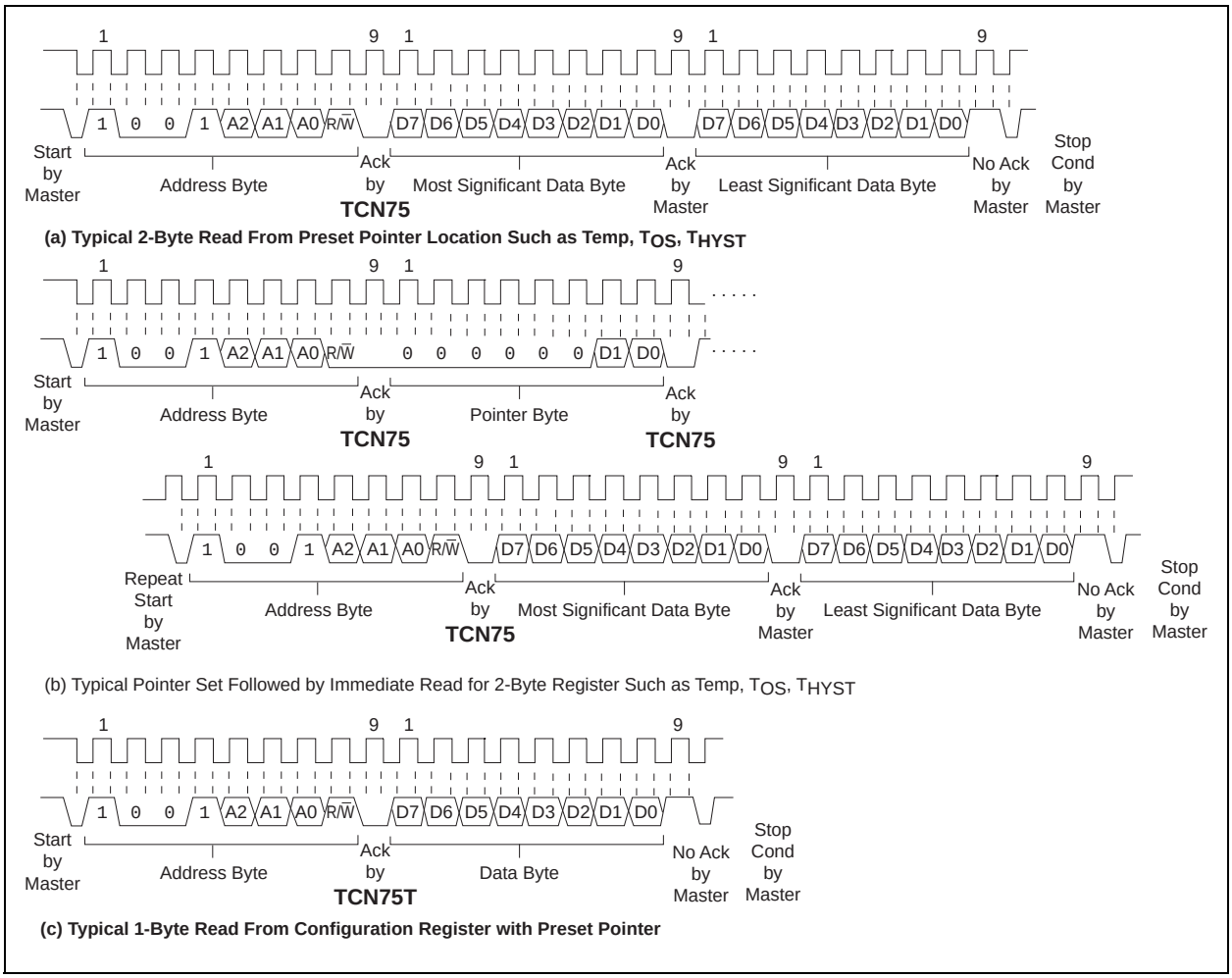
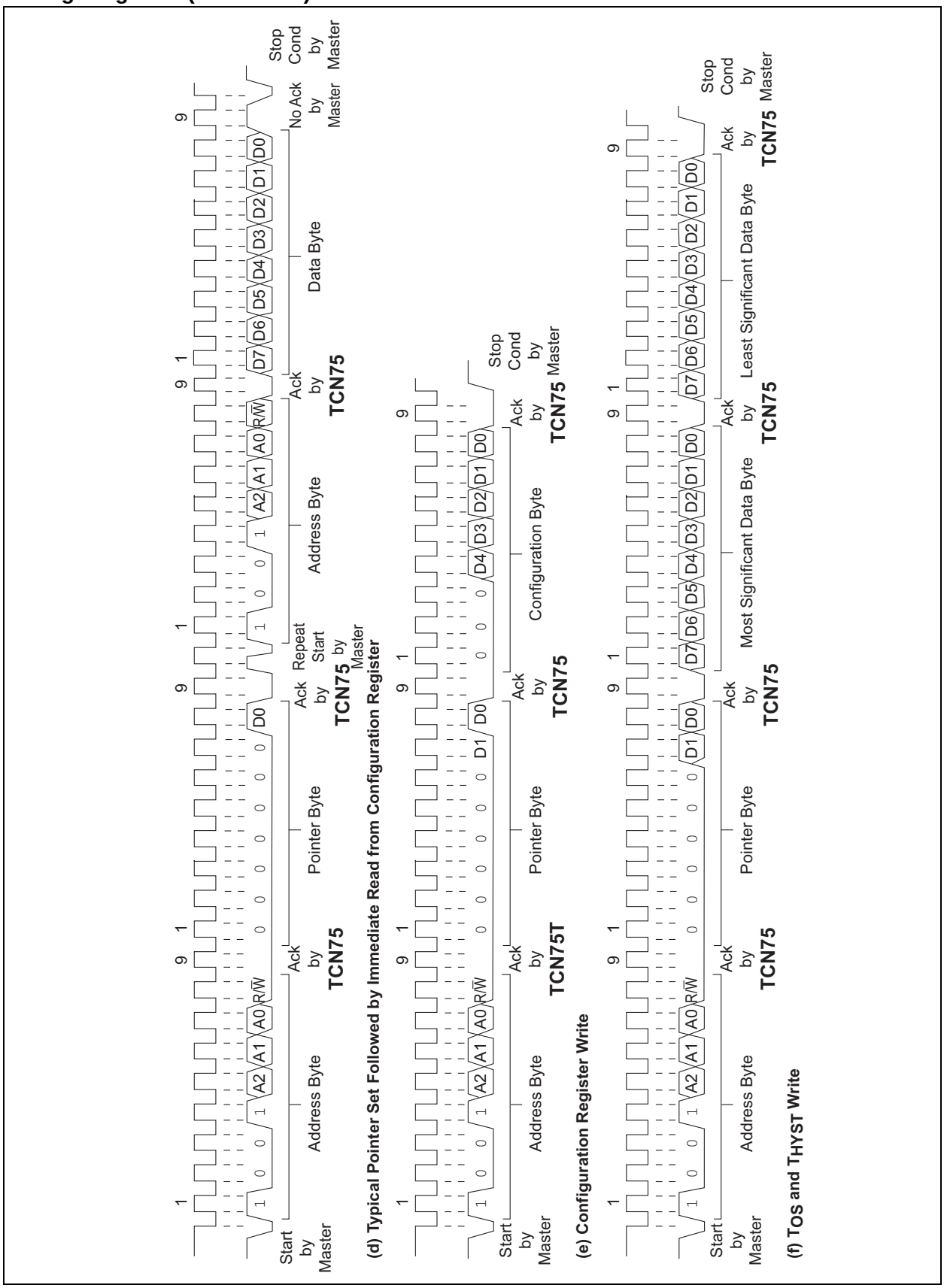


FIGURE 5-1: *Timing Diagrams*

Timing Diagrams (Continued)



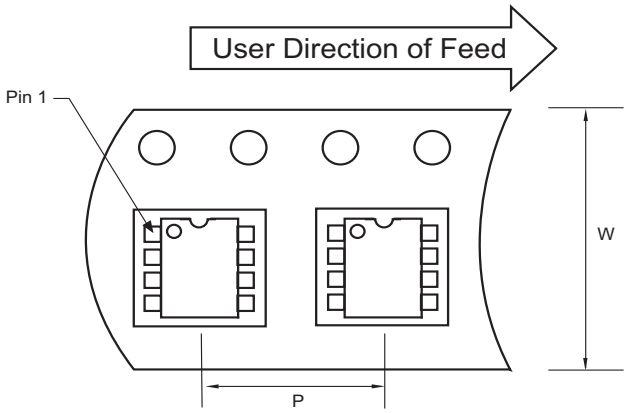
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Package marking data not available at this time.

6.2 Taping Form

Component Taping Orientation for 8-Pin MSOP Devices

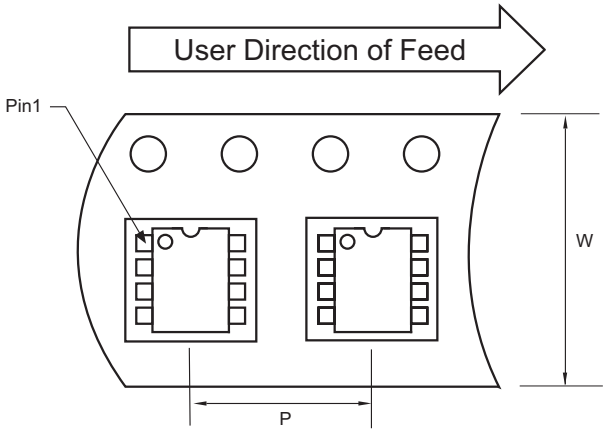


Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Standard Reel Component Orientation
for 713 Suffix Device

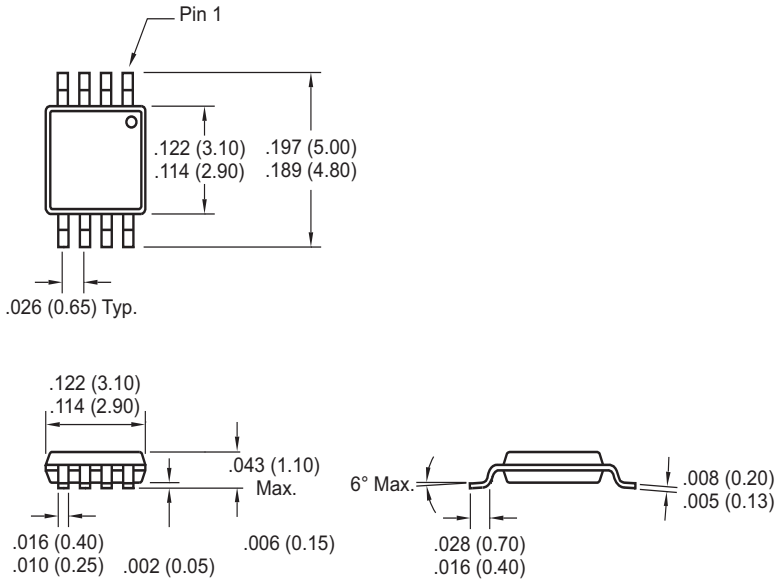
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

6.3 Package Dimensions

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

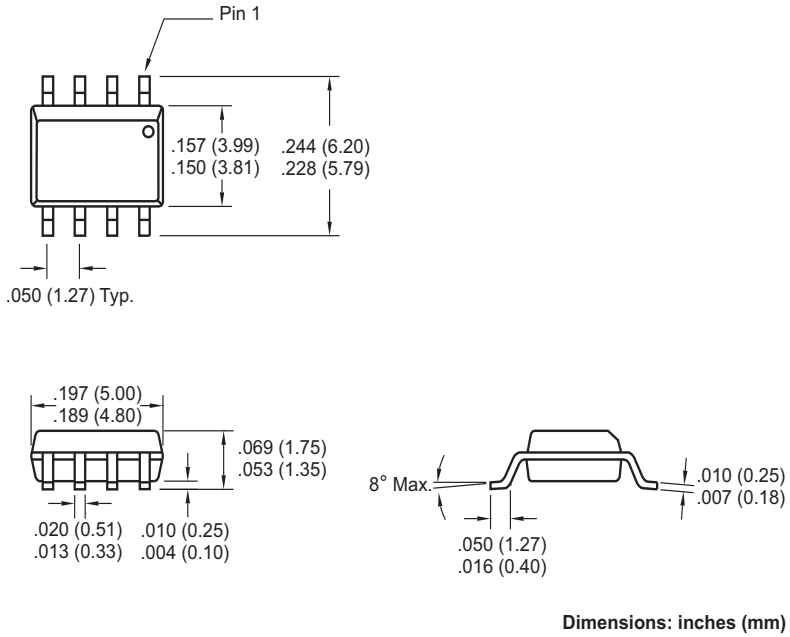
8-Pin MSOP



Dimensions: inches (mm)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

8-Pin SOIC



Dimensions: inches (mm)

7.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

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Hong Kong
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