

- ✧ No deep color support, Video input data formats: RGB666 and RGB888
    - TC358860XBG performs dithering for RGB888 video stream to RGB666 panel
    - TC358860XBG appends MSB bits of RGB666 video stream (RGB[5:0] → {RGB[5:0], RGB[5:4]}) to RGB888 panel
  - ✧ Interlaced video mode is not supported.
  - ✧ Dual links with Left-Right split: DSI0 carries the left half data of eDP Rx video stream and DSI1 carries the right one
    - DSI0 can be assigned/programmed to either DSITx port.
    - The maximum length of each half is limited to 2048-pixel plus up to 32-pixel overlap.
    - The skew (DSI1 delay w.r.t. to DSI0) between DSI0 and DSI1 can be programmed by register
  - ✧ Provide path for eDP host/transmitter to control TC358860XBG and its attached panel.
  - ✧ Built in Color Bar Generator to verify Dual DSI link without eDPRx input.
  - ✧ DSITx operates in video mode when video stream is continuously received at eDPRx port.
- Video function
    - ✧ Compression engine : 2 to 1 compression for 4k2k resolution
    - ✧ Magic square
    - ✧ Color bar output for debug
  - I<sup>2</sup>C Slave Port
    - ✧ Support for normal (100 kHz), fast (400 kHz or 1 MHz, if SysClk is running at 25 MHz) modes.
    - ✧ External I<sup>2</sup>C master can access TC358860XBG internal and DPCD registers and read/write DSI panel register (via DSI link).
    - ✧ Address auto increment is supported.
    - ✧ TC358860XBG Slave Port address is 0x68, (binary 1101\_000x) where x = 1 for read and x = 0 for write. The slave address can be changed to 0x0E (binary 0001\_110x) by a weak pull up to pin GPIO0 during boot time.
  - Power Supply
    - ✧ MIPI D-PHY                      1.2 V
    - ✧ Core, MIPI D-PHY and eDP-PHY              1.1 V
    - ✧ eDP-PHY:                      1.8 V
    - ✧ I/O:                      1.8 V or 3.3 V (all IO pins must be same power level)
    - ✧ HPD Output Pad              1.8 V or 3.3 V
  - Power Consumption (Typical Condition)
    - ✧ 126 mW
      - Condition: Input 5.4 Gbps eDP 1 lane, Output DSI port 4 data lane, Full HD@60fps resolution, 24 bpp
  - Packaging
    - ✧ 65-pin FBGA Package with 0.5 mm ball pitch
    - ✧ 5 x 5 mm<sup>2</sup>

## Table of content

REFERENCES.....	6
1. Introduction.....	7
2. Features .....	9
3. External Pins .....	11
3.1. Pinout Description .....	11
3.2. Pin Layout.....	13
4. Package .....	14
5. Electrical characteristics.....	15
5.1. Absolute Maximum Ratings.....	15
5.2. Operating Conditions.....	15
5.3. DC Electrical Specification .....	16
5.3.1. Normal CMOS I/Os DC Specifications .....	16
5.3.2. MIPI DSI I/Os DC Specifications .....	17
6. Revision History .....	18
RESTRICTIONS ON PRODUCT USE.....	19

## Table of Figures

Figure 1.1 TC358860XBG in System Application.....	8
Figure 1.2 TC358860XBG Block Diagram and Functional.....	8
Figure 3.1 TC358860XBG Chip Pin Layout (Top view).....	13
Figure 4.1 Package Dimension.....	14
Figure 5.1 Signaling and voltage levels .....	17

## List of Tables

Table 3.1 TC358860XBG Functional Signal List.....	11
Table 3.2 Pin Count Summary .....	12
Table 4.1 Package Details .....	14
Table 5.1 Absolute Maximum Ratings .....	15
Table 5.2 Recommended Operating Conditions.....	15
Table 5.3 Normal CMOS IOs DC Specifications .....	16
Table 5.4 MIPI HSTX and LPTX DC specifications .....	17
Table 5.5 LPRX DC Specification .....	17
Table 6.1 Revision History .....	18

- MIPI is registered trademark of MIPI Alliance, Inc.
- VESA, VESA logo and the DisplayPort Icon are trademarks of the Video Electronics Standards Association.

Copyright © 2005-2010 MIPI Alliance, Inc. All rights reserved.

MIPI Alliance Member Confidential.

All rights reserved. This material is reprinted with the permission of the MIPI Alliance, Inc. No part(s) of this document may be disclosed, reproduced or used for any purpose other than as needed to support the use of the products of Toshiba Cooperation and its subsidiaries and its affiliates.

**NOTICE OF DISCLAIMER**

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI. The material contained herein is provided on an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and cannot be used without its express prior written permission.

ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with the contents of this Document. The use or implementation of the contents of this Document may involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any IPR or claims of IPR as respects the contents of this Document or otherwise.

Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

MIPI Alliance, Inc.  
c/o IEEE-ISTO  
445 Hoes Lane  
Piscataway, NJ 08854  
Attn: Board Secretary

This Notice of Disclaimer applies to all DSI input and processing paths related descriptions throughout this document.

## REFERENCES

1. MIPI D-PHY, "MIPI Alliance Specification for D-PHY Version 1.00.00 14-May-2009"
2. MIPI Alliance Standard for DSI Version 1.02.00 – 28 June 2010
3. VESA DisplayPort Standard (Version 1, Revision 2a May 23, 2012)
4. VESA Embedded DisplayPort (eDP) Standard (Version 1.4 February 28, 2013)
5. I<sup>2</sup>C bus specification, version 2.1, January 2000, Philips Semiconductor

## 1. Introduction

This Functional Specification defines operation of TC358860XBG chip, which converts an Embedded Display Port (eDP) video stream into an MIPI DSI stream. There are four eDP main link lanes in TC358860XBG, they can toggle at either 1.62, 2.16, 2.7, 3.24, 4.32 or 5.4 Gbps/link to receive up to 17.28 Gbps (5.4 Gbps \* 0.8 \* 4) of video stream. The 4-data lanes dual link DSI Tx can transmit up to 8 Gbps (1 Gbps \* 4 \* 2) of video stream.

For input video stream with bandwidth (BW) < 4 Gbps, TC358860XBG can output the video data either with a single DSI link or performs left-right line split to output the video data stream with dual DSI links. For input video stream with BW requirements between 4 Gbps and 8 Gbps, left-right line split and dual DSI links usage is necessary.

TC358860XBG provides a compression engine which compress video data with 2-to-1 ratio. This enables TC358860XBG to receive 4K @60fps video streams at eDP Rx, compress and send out to a dual DSI link 4K panel for display. A de-compress engine is expected in the DSI panel.

Host/eDPTx controls/configures TC358860XBG chip by using its AUX channel (I<sup>2</sup>C over AUX). TC358860XBG provides mail box register/command queue for host to control/configure/command DSI panels, too. After host writes to the command queue, TC358860XBG starts DSI “command packets” to communicate with the DSI panels.

Alternatively, an external I<sup>2</sup>C master can configure TC358860XBG via I<sup>2</sup>C bus. Command queue address can also be access via I<sup>2</sup>C bus, which means Host can use I<sup>2</sup>C to access command queue, which in turn, controls DSI panel parameters.

Please note that host can not use both AUX ch. and I<sup>2</sup>C bus for register setting simultaneously.

The target system diagram and TC358860XBG block diagram are shown in Figure 1.1 and Figure 1.2, respectively.

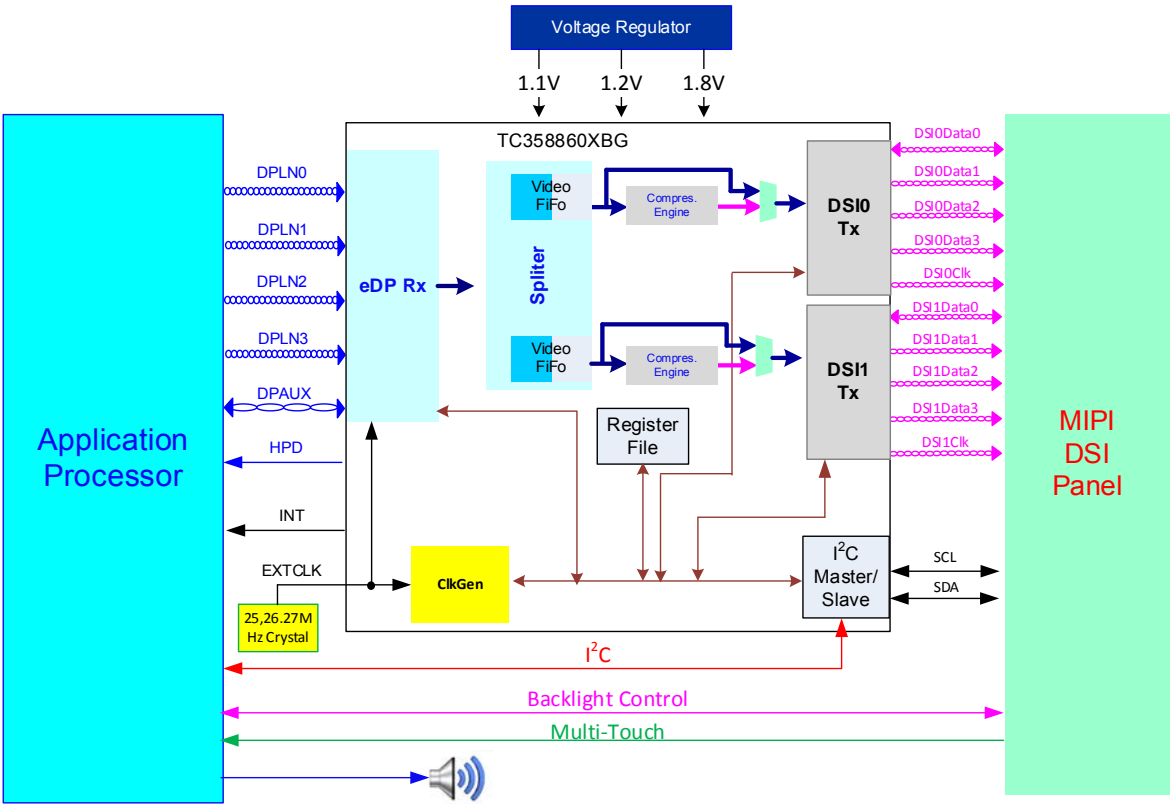


Figure 1.1 TC358860XBG in System Application

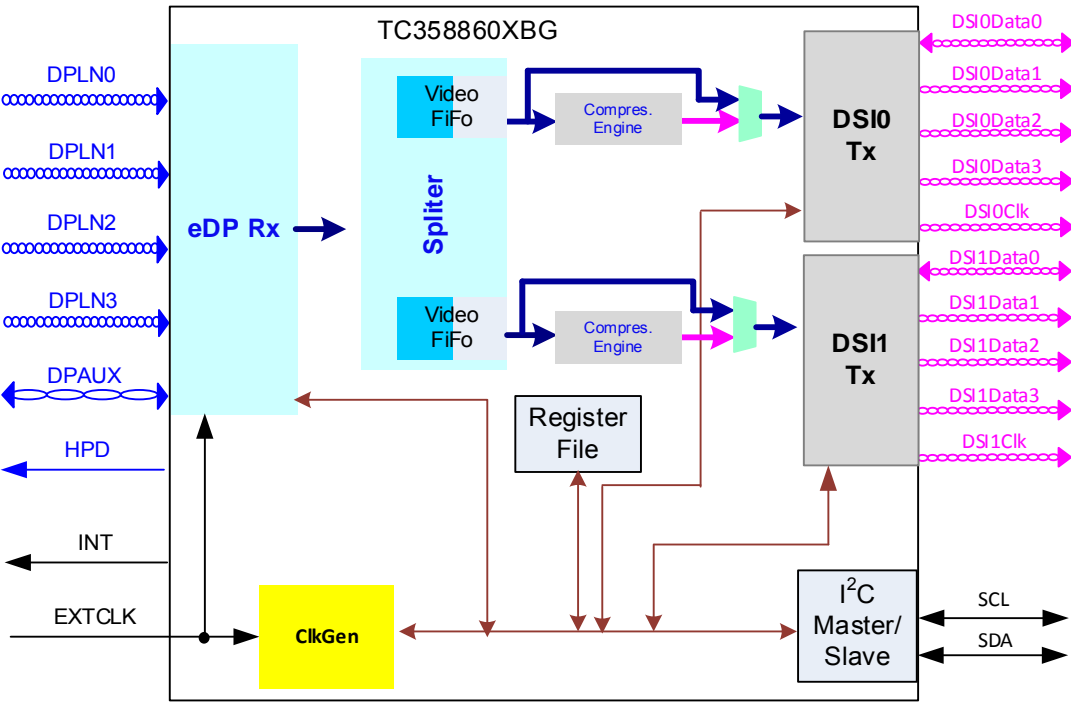


Figure 1.2 TC358860XBG Block Diagram and Functional

## 2. Features

- TC358860XBG follows the following standards:
  - ✧ MIPI Alliance Specification for Display Serial Interface (DSI) version 1.1, Nov 22 2011
  - ✧ MIPI Alliance Specification for D-PHY Version 1.1, Nov 7 2011
  - ✧ VESA DisplayPort Standard version 1.2a, May 23 2012.
  - ✧ VESA Embedded DisplayPort Standard version 1.4 Feb. 28 2013
- eDP Sink (Receiver)
  - ✧ Bit Rate @ 1.62, 2.16, 2.7, 3.24, 4.32 or 5.4Gbps, Voltage Swing @0.2 to 1.2 V, Pre-Emphasis Level @3.5dB.
  - ✧ There are four lanes available in eDP main Link, which can operate in 1-, 2- or 4-lane configuration.
  - ✧ Support Single-Stream Transport (SST), not multi-Stream Transport (MST)
  - ✧ Capable of Full and Fast Link Training
  - ✧ AUX channel with nominal bit rate at 1 Mbps.
  - ✧ Video input data formats supported: RGB666 and RGB888
  - ✧ Absolute maximum pixel rate is 600Mpixel/s.
  - ✧ Does not support HDCP encryption, Alternate Scrambler Seed Reset (ASSR) is used for content protection.
    - System designer can connect ASSR\_Disable Pad to GND, which prevents eDPTx (Source device) to disable ASSR mode TC358860XBG.
    - In other words, when ASSR\_Disable Pad is grounded, the Source device cannot clear the ALTERNATE\_SCRAMBER\_RESET\_ENABLE bit of the eDP\_CONFIGURATION\_SET register (DPCD Address 0010Ah, bit 0) to 0.
  - ✧ No audio SDP, Multi-touch and Backlight DPCD registers support
  - ✧ Support REFCLK from 24, 25, 26 and 27 MHz.
- DSI Transmitter
  - ✧ Dual 4-Data Lane DSI Links with Bi-direction support at Data Lane 0. Each link can be used in 1-, 2-, 3- or 4-data lane configuration. Maximum speed at 1.0 Gbps/lane.
  - ✧ No deep color support, Video input data formats: RGB666 and RGB888
    - TC358860XBG performs dithering for RGB888 video stream to RGB666 panel
    - TC358860XBG appends MSB bits of RGB666 video stream (RGB[5:0] → {RGB[5:0], RGB[5:4]}) to RGB888 panel
  - ✧ Interlaced video mode is not supported.
  - ✧ Dual links with Left-Right split: DSI0 carries the left half data of eDP Rx video stream and DSI1 carries the right one
    - DSI0 can be assigned/programmed to either DSITx port.
    - The maximum length of each half is limited to 2048-pixel plus up to 32-pixel overlap.
    - The skew (DSI1 delay w.r.t. to DSI0) between DSI0 and DSI1 can be programmed by register
  - ✧ Provide path for eDP host/transmitter to control TC358860XBG and its attached panel.
  - ✧ Built in Color Bar Generator to verify Dual DSI link without eDPRx input.
  - ✧ DSITx operates in video mode when video stream is continuously received at eDPRx port.



- Video function
  - ✧ Compression engine : 2 to 1 compression
  - ✧ Magic square
  - ✧ Color bar output for debug
- I<sup>2</sup>C Slave Port
  - ✧ Support for normal (100 kHz), fast (400 kHz or 1 MHz, if SysClk is running at 25 MHz) modes.
  - ✧ External I<sup>2</sup>C master can access TC358860XBG internal and DPCD registers and read/write DSI panel register (via DSI link).
  - ✧ Address auto increment is supported.
  - ✧ TC358860XBG Slave Port address is 0x68, (binary 1101\_000x) where x = 1 for read and x = 0 for write. The slave address can be changed to 0x0E (binary 0001\_110x) by a weak pull up to pin GPIO0 during boot time.
- Power Supply
 

✧ MIPI D-PHY	1.2 V
✧ Core, MIPI D-PHY and eDP-PHY	1.1 V
✧ eDP-PHY:	1.8 V
✧ I/O:	1.8 V or 3.3 V (all IO pins must be same power level)
✧ HPD Output Pad	1.8 V or 3.3 V
- Power Consumption (Typical Condition)
  - ✧ 126 mW
    - Condition: Input 5.4 Gbps eDP 1 lane, Output DSI port 4 data lane, Full HD@60fps resolution, 24 bpp
- Packaging
  - ✧ 65-pin FBGA Package with 0.5 mm ball pitch
  - ✧ 5 x 5 mm<sup>2</sup>

## 3. External Pins

### 3.1. Pinout Description

The following table gives the signals of TC358860XBG and their function.

**Table 3.1 TC358860XBG Functional Signal List**

Group	Pin Name	I/O	Type	Initial	Function	Power Supply
System (8)	RESET_N	I	SCH	I	System Reset – active Low	VDDIO
	EXTCLK	I	SCH	I	Ref Clock : 24,25,26,27 MHz	VDDIO
	DIS_ASSR	I	Normal	I	1: Source device can Disable ASSR 0: Source device cannot Disable ASSR	VDDIO
	INT	O	Normal	O(L)	Interrupt	VDDIO
	GPIO[3:0]	I/O	Normal	I(PD)	GPIO	VDDIO
DSI0Tx (10)	DSI0CP	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Clock Lane Positive	1.2 V
	DSI0CM	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Clock Lane Negative	1.2 V
	DSI0DP_0	I/O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane0 Positive	1.2 V
	DSI0DM_0	I/O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane0 Negative	1.2 V
	DSI0DP_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane Positive	1.2 V
	DSI0DM_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane Negative	1.2 V
DSI1Tx (10)	DSI1CP	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Clock Lane Positive	1.2 V
	DSI1CM	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Clock Lane Negative	1.2 V
	DSI1DP_0	I/O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane0 Positive	1.2 V
	DSI1DM_0	I/O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane0 Negative	1.2 V
	DSI1DP_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane Positive	1.2 V
	DSI1DM_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane Negative	1.2 V
eDP Rx (11)	DPLNP_3,2,1,0	I	eDP-PHY	I	eDP Output Main Link Positive	1.8 V
	DPLNM_3,2,1,0	I	eDP-PHY	I	eDP Output Main Link Negative	1.8 V
	DPAUXP	I/O	eDP-PHY	I	eDP Output AUX Channel Positive	1.8 V
	DPAUXM	I/O	eDP-PHY	I	eDP Output AUX Channel Negative	1.8 V
	HPD	O	Normal	O(L)	eDP Rx INT/Detected Output	VDDIO
I2C (2)	I2C_SCL	I/O	FS/SCH	I	I <sup>2</sup> C Clock	VDDIO
	I2C_SDA	I/O	FS/SCH	I	I <sup>2</sup> C Data	VDDIO
Test(4)	TM	I	Normal	I(PD)	Test Pins, tie to GND	VDDIO
	TEST1	I	-	I	Test Pins, tie to GND	1.8 V
	TEST2	O	Analog	O(L)	Analog TEST , Open	-
	TEST3	I	Normal	I	Test Pins, connect to Pull-Up 1kΩ	1.1 V
Power (10)	VDDC (2)	-	-	-	VDD for internal Core	1.1 V
	VDDIO(1)	-	-	-	VDD for I/O voltage	1.8 or 3.3 V
	VDDP2(1)	-	-	-	VDD for PLL	1.1 V
	VDD_DP18(2)	-	-	-	VDD for DP PHY	1.8 V
	VDD_DP11(2)	-	-	-	VDD for DP PHY	1.1 V
	VDD_DSI0(1)	-	-	-	VDD for MIPI DPHY	1.2 V
	VDD_DSI1(1)	-	-	-	VDD for MIPI DPHY	1.2 V
Ground(10)	VSS(10)	-	-	-	VSS for internal core/I/O, DPHY	-

Normal: Normal IO (Programmable Output Drive Strength 2,4,8 and 12 mA)  
 OD: Pseudo open-drain output, schmidt input  
 FS/SCH: Fail Safe schmidt input buffer  
 MIPI-PHY: Front-end analog IO for MIPI  
 eDP-PHY: Front-end analog IO for eDP RX  
 PD Pull Down

Table 3.2 Pin Count Summary

Group Name	Pin Count	Notes
System	8	-
DSI0Tx, DSI1Tx	20	CLK + Data 4 lane x 2 port
eDP Rx	11	Data 4 lane + AUX 1 lane+ HPD
I2C	2	-
Test	4	-
Power	10	-
Ground	10	-
Total	65	-

3.2. Pin Layout

The mapping of TC358860XBG signals to the external pins is shown in the figure below.

		DSI1						
A1	A2	A3	A4	A5	A6	A7	A8	A9
VDD_DSI0	VDD_DSI1	DSI1DP_3	DSI1DP_2	DSI1CP	DSI1DP_1	DSI1DP_0	VDDC	VDDIO
B1	B2	B3	B4	B5	B6	B7	B8	B9
DSI0DP_0	DSI0DM_0	DSI1DM_3	DSI1DM_2	DSI1CM	DSI1DM_1	DSI1DM_0	RESET_N	DIS_ASSR
C1	C2	C3	C4	C5	C6	C7	C8	C9
DSI0DP_1	DSI0DM_1	no-ball	no-ball	no-ball	no-ball	no-ball	I2C_SDA	I2C_SCL
D1	D2	D3	D4	D5	D6	D7	D8	D9
DSI0CP	DSI0CM	no-ball	VSS	VSS	TEST1	no-ball	GPIO2	GPIO3
E1	E2	E3	E4	E5	E6	E7	E8	E9
DSI0DP_2	DSI0DM_2	no-ball	VSS	VSS	TM	no-ball	GPIO0	GPIO1
F1	F2	F3	F4	F5	F6	F7	F8	F9
DSI0DP_3	DSI0DM_3	no-ball	VSS	TEST2	TEST3	no-ball	INT	EXTCLK
G1	G2	G3	G4	G5	G6	G7	G8	G9
VDDC	VSS	no-ball	no-ball	no-ball	no-ball	no-ball	HPD	VDDP2
H1	H2	H3	H4	H5	H6	H7	H8	H9
VSS	DPLNM_3	VSS	DPLNM_2	VSS	DPLNM_1	VSS	DPLNM_0	DPAUXM
J1	J2	J3	J4	J5	J6	J7	J8	J9
VDD_DP11	DPLNP_3	VDD_DP18	DPLNP_2	VDD_DP11	DPLNP_1	VDD_DP18	DPLNP_0	DPAUXP

Figure 3.1 TC358860XBG Chip Pin Layout (Top view)

- Signal(VDDIO)
- Differential signal
- Analog signal
- Power
- GND
- No-ball or Reserved ball



## 5. Electrical characteristics

### 5.1. Absolute Maximum Ratings

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

**Table 5.1 Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V – Digital IO) (3.3V – Digital IO)	VDDIO	-0.3 to +1.96 -0.3 to +3.63	V
Supply voltage (1.1V – Digital Core)	VDDC	-0.3 to +1.54	V
Supply voltage (1.2V – MIPI DSI PHY)	VDD_MIPI	-0.3 to +1.54	V
Supply voltage (1.8V – eDP PHY)	VDD_DP18	-0.3 to +1.98	V
Supply voltage (1.1V – eDP PHY)	VDD_DP11	-0.3 to +1.54	V
Input voltage (DSI I/O)	V <sub>IN_DSI</sub>	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI I/O)	V <sub>OUT_DSI</sub>	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V <sub>IN_IO</sub>	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V <sub>OUT_IO</sub>	-0.3 to VDDIO+0.3	V
Input current	I <sub>in</sub>	-10 to +10	mA
Junction temperature	T <sub>j</sub>	125	°C
Storage temperature	T <sub>stg</sub>	-40 to +125	°C

### 5.2. Operating Conditions

**Table 5.2 Operating Conditions**

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	1.62	1.8	1.98	V
Supply voltage (3.3 V – Digital IO)	VDDIO	2.97	3.3	3.63	V
Supply voltage (1.1V – PLL)	VDDP2	1.04	1.10	1.16	V
Supply voltage (1.1 V – Digital Core)	VDDC	1.04	1.10	1.16	V
Supply voltage (1.1 V – eDP PHY)	VDD_DP11	1.04	1.10	1.16	V
Supply voltage (1.8 V – eDP PHY)	VDD_DP18	1.71	1.8	1.89	V
Supply voltage (1.2 V – MIPI-DPHY)	VDD_MIPI0	1.1	1.2	1.25	V
	VDD_MIPI1				
Operating internal frequency	f <sub>opr</sub>	-	-	300	MHz
Operating temperature (ambient temperature with voltage applied)	T <sub>a</sub>	-30	+25	+85	°C
Supply noise voltage	V <sub>SN</sub>	-	-	100	mV <sub>pp</sub>

## 5.3. DC Electrical Specification

All typical values are at normal operating conditions unless otherwise specified.

### 5.3.1. Normal CMOS I/Os DC Specifications

**Table 5.3 Normal CMOS IOs DC Specifications**

Parameter – CMOS I/Os	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage, High level Input Note1	$V_{IH}$	--	0.7 VDDIO	--	VDDIO +0.3V	V
Input voltage, Low level Input Note1	$V_{IL}$	--	VSS - 0.3V	--	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note 1,2	$V_{IHS}$	--	0.7 VDDIO	--	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note 1,2	$V_{ILS}$	--	0	--	0.3 VDDIO	V
Output voltage, High level Note1, 2	$V_{OH}$	$I_{OH} = 1 \text{ mA}$	VDDIO - 0.4V	--	VDDIO	V
Output voltage, Low level Note1, 2	$V_{OL}$	$I_{OL} = 2 \text{ mA}$	--	--	0.4	V
Input leakage current, High level without Pull-down I/O pin	$I_{ILH1}$	$V_{IN} = +VDDIO$ , VDDIO = 3.6 V	--	--	10	$\mu\text{A}$
Input leakage current, Low level	$I_{ILL}$	$V_{IN} = 0 \text{ V}$ , VDDIO = 3.6 V	--	--	10	$\mu\text{A}$

Note1: Each power source is operating within recommended operating condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

### 5.3.2. MIPI DSI I/Os DC Specifications

Timing specification below has been ported from MIPI Alliance specification for D-PHY version 01-00-00. Timing defined in MIPI Alliance specification for D-PHY version 01-00-00 has precedence over timing described in the sections below.

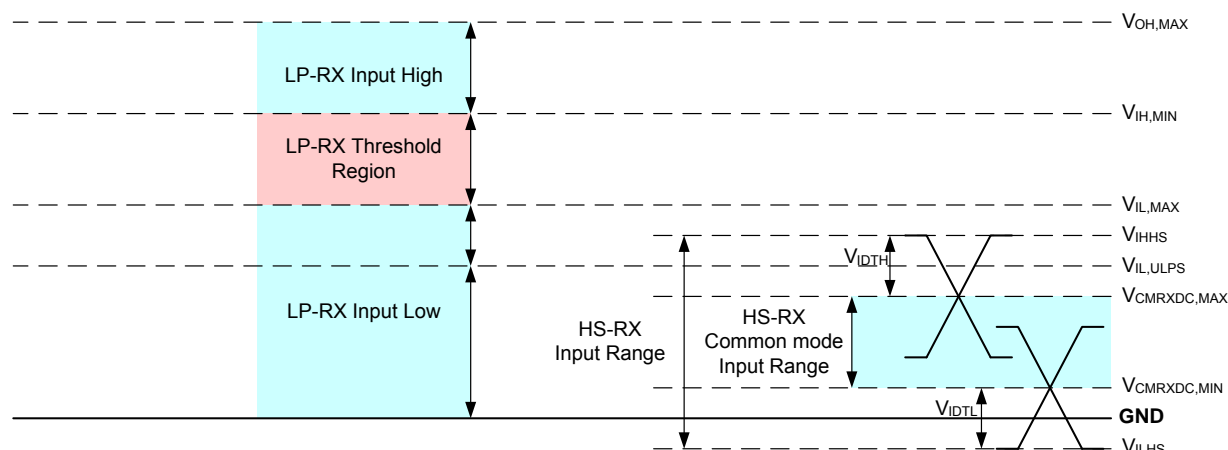


Figure 5.1 Signaling and voltage levels

Table 5.4 MIPI HSTX and LPTX DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
HS mode						
VCMTX	HS transmit static common mode voltage	150	200	250	mV	1
$ \Delta VCMTX(1,0) $	VCMTX mismatch when output is Differential-1 or Differential-0	-	-	5	mV	2
$ VOD $	HS transmit differential voltage	140	200	270	mV	1
$ \Delta VOD $	VOD mismatch when output is Differential-1 or Differential-0	-	-	14	mV	2
VOHHS	HS output high voltage	-	-	360	mV	-
ZOS	Single ended output impedance	40	50	62.5	$\Omega$	-
$\Delta ZOS$	Single ended output impedance mismatch	-	-	10	%	-
LP Mode						
VOH	Thevenin output high level	1.1	1.2	1.25	V	-
VOL	Thevenin output low level	-50	-	50	mV	-
ZOLP	Output impedance of LP transmitter	110	-	-	$\Omega$	3

Notes:

1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended the implementer minimize  $\Delta VOD$  and  $\Delta VCMTX(1,0)$  in order to minimize radiation and optimize signal integrity.
3. Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the TRLP/TFLP specification is met.

Table 5.5 LPRX DC Specification

Parameter	Description	Remarks	Min	Typ.	Max	Unit
$V_{IL}$	Input low threshold	Not in ULPS	-	-	550	mV
$V_{IL-ULPS}$	Input low threshold in ULPS	-	-	-	300	mV
$V_{IH}$	Output high threshold	-	880	-	-	mV
$V_{HYST}$	Input hysteresis	-	25	-	-	mV



## 6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.1	2014-09-29	Newly released
1.8	2016-05-16	<p>Modified Figure1.1 , and 1.2. (block diagram) and Table 3.1 (function signal list)</p> <p>Modified typo</p> <ul style="list-style-type: none"> <li>● Package weight</li> <li>● Remove 4.86, 2.43Gbps spec of video stream.</li> <li>● REFCLK Frequency: 24,25,26 and 27MHz</li> <li>● Operating temperature in Table 5.2</li> <li>● Output voltage, High/Low Level in Table 5.3</li> <li>● Pin name enabled to change the slave address : HPD -&gt; GPIO0</li> <li>● Power consumption : 130mW -&gt; 126mW</li> </ul>
2.0a	2017-07-01	<p>Modified values in Table 5.2.</p> <p>Added description in section 3.1.</p> <p>Changed header, footer and the last page.</p> <p>Changed corporate name.</p>

## RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**