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REVISION HISTORY

5/13—Rev. 0 to Rev. A

Changed Voltage Rating from 6.3 V to 35 V in Bootstrap
Capacitors Section..... 17

2/12—Revision 0: Initial Version

The diagram illustrates the internal architecture of the SSM3302 audio processor. It features two parallel processing channels: a Mono channel at the top and a Stereo channel at the bottom. Each channel starts with an input (INR+/- for Mono, INL+/- for Stereo) passing through 40kΩ resistors to a GAIN CONTROL block. The Mono channel's gain control is also influenced by the SDNR input. Both channels then feed into a MODULATOR (Σ-Δ) block, which is biased by a BIAS input. The modulators output to FET DRIVER blocks, which are also biased by a BIAS input. The Mono channel's FET driver output is connected to the EDGE CONTROL block. The final outputs are BOOTR+/- for Mono and BOOTL+/- for Stereo. The entire circuit is powered by PVDD and AGND, with a VREG (AVDD) block for the mono channel and a REGEN block for the stereo channel. A THERM input is also present at the top right.

Figure 1.

SPECIFICATIONS

PVDD = 12 V, T_A = 25°C, R_L = 8 Ω + 64 μH, EDGE = AGND, gain = 9 dB, VREG = off, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power/Channel	P _O	R _L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		12 ¹		W
		R _L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		8		W
		R _L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		2.7		W
		R _L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		15 ¹		W
		R _L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		10		W
		R _L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		3.2		W
		R _L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		20 ¹		W
		R _L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		13 ¹		W
		R _L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		4.8		W
		R _L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		24 ¹		W
		R _L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		16 ¹		W
		R _L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		5.7		W
		R _L = 2 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 12 V (mono mode)		29 ²		W
		R _L = 2 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 7 V (mono mode)		9.4 ²		W
		R _L = 2 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 12 V (mono mode)		36.6 ²		W
		R _L = 2 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 7 V (mono mode)		12.7 ²		W
Efficiency	η	P _O = 7 W, 8 Ω, PVDD = 12 V, EDGE = low (normal operation)		91.5		%
		P _O = 7 W, 8 Ω, PVDD = 12 V, EDGE = AVDD (ultralow EMI mode)		82		%
Total Harmonic Distortion + Noise	THD + N	P _O = 5 W into 8 Ω, f = 1 kHz, PVDD = 12 V		0.01		%
Input Common-Mode Voltage Range	V _{CM}		1.0		AVDD – 1	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = 2.5 V ± 100 mV at 1 kHz, output referred		43		dB
Channel Separation	X _{TALK}	P _O = 0.5 W, f = 1 kHz		80		dB
Average Switching Frequency	f _{SW}			300		kHz
Differential Output Offset Voltage	V _{OOS}	Gain = 9 dB			3.0	mV
POWER SUPPLY						
Supply Voltage Range	PVDD	Guaranteed from PSRR test	7		18	V
Power Supply Rejection Ratio	PSRR _{DC}	PVDD = 7 V to 15 V, dc input floating		70		dB
Supply Current (Stereo)	PSRR _{AC}	V _{RIPPLE} = 100 mV at 1 kHz, inputs are ac grounded, C _{IN} = 0.1 μF		80		dB
	I _{SY} PVDD	V _{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 15 V, V _{REGEN} = AVDD (internal V _{REG} active)		12.2		mA
		V _{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 15 V, V _{REGEN} = AGND (internal V _{REG} disabled)		6.2		mA
		V _{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 12 V, V _{REGEN} = AGND (internal V _{REG} disabled)		5		mA
		V _{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 7 V, V _{REGEN} = AGND (internal V _{REG} disabled)		3		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Shutdown Current	I _{SVAVDD}	V _{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 15 V, V _{REGEN} = AGND (internal V _{REG} disabled)		5.85		mA
		V _{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 12 V, V _{REGEN} = AGND (internal V _{REG} disabled)		5.8		mA
		V _{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 7 V, V _{REGEN} = AGND (internal V _{REG} disabled)		5.6		mA
	I _{SD}	$\overline{SD}$ = AGND		10		μA
ANALOG SUPPLY						
External Supply Voltage	AVDD	Permissible range for external AVDD, V _{REGEN} = AGND	4.5		5.5	V
On-Board Regulator	V _{VREG}		5			V
Regulator Current	I _{VREG}		20			mA
Regulator Power Supply Rejection	PSRR _{VREG}		70			dB
GAIN CONTROL						
Closed-Loop Voltage Gain	A _V	See Table 5 for gain options	9		24	dB
Input Impedance	Z _{IN}		40			kΩ
SHUTDOWN CONTROL						
Input Voltage High	V _{IH}	$\overline{SD}$ rising edge from AGND to AVDD $\overline{SD}$ falling edge from AVDD to AGND $\overline{SD}$ = GND	1.35			V
Input Voltage Low	V _{IL}				0.35	V
Turn-On Time	t _{WU}		40			ms
Turn-Off Time	t _{SD}		500			μs
Output Impedance	Z _{OUT}		56			kΩ
AMPLIFIER PROTECTION						
Overcurrent Threshold	I _{OC}			6		A
Overtemperature Warning	T _{WARN}		120			°C
Overtemperature Shutdown	T _{SD}		145			°C
Recovery Temperature	T _{REC}		85			°C
NOISE PERFORMANCE						
Output Voltage Noise	e _n	PVDD = 12 V, f = 20 Hz to 20 kHz, inputs are ac grounded, gain = 9 dB, A-weighted		100		μV rms
Signal-to-Noise Ratio	SNR	P _O = 10 W, R _L = 8 Ω		98		dB

¹ Although the SSM3302 has good audio quality above $2 \times 10\text{ W}$ into $4\ \Omega$, continuous output power beyond $2 \times 10\text{ W}$ into $4\ \Omega$ must be avoided due to device packaging limitations.

² Mono mode. Output power beyond 20 W needs special care for thermally considered printed circuit board (PCB) design.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Power Supply Voltage (PVDD)	−0.3 V to +25 V
Analog Supply Voltage (AVDD)	−0.3 V to +6 V
Input Voltage	−0.3 V to +6 V
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JA} and θ_{JC} are determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling.

Table 3. Thermal Resistance

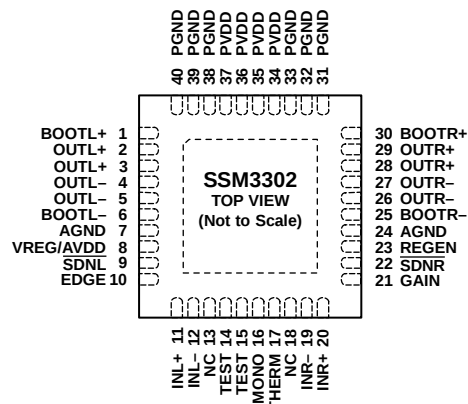
Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead, 6 mm × 6 mm LFCSP	31	2.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. USE MULTIPLE VIAS TO CONNECT THE EXPOSED PAD TO THE GROUND PLANE.
2. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

10198-002

Figure 2. Pin Configuration (Top Side View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BOOTL+	Bootstrap Input/Output for Left Channel, Noninverting Output.
2, 3	OUTL+	Noninverting Output for Left Channel.
4, 5	OUTL-	Inverting Output for Left Channel.
6	BOOTL-	Bootstrap Input/Output for Left Channel, Inverting Output.
7	AGND	Analog Ground.
8	VREG/AVDD	5 V Regulator Output (if REGEN = high)/AVDD Input (if REGEN = low).
9	SDNL	Shutdown, Left Channel. Active low digital input.
10	EDGE	Edge Control (Low Emission Mode). Active high digital input.
11	INL+	Noninverting Input for Left Channel.
12	INL-	Inverting Input for Left Channel.
13, 18	NC	This pin is not connected internally (see Figure 2).
14, 15	TEST	Test Pins. Tie to AGND.
16	MONO	Mono Output Mode Enable.
17	THERM	Overtemperature Warning (Open Collector).
19	INR-	Inverting Input for Right Channel.
20	INR+	Noninverting Input for Right Channel.
21	GAIN	Gain Select from 9 dB to 24 dB.
22	SDNR	Shutdown, Right Channel. Active low digital input.
23	REGEN	5 V Regulator Enable, Active High.
24	AGND	Analog Ground.
25	BOOTR-	Bootstrap Input/Output for Right Channel, Inverting Output.
26, 27	OUTR-	Inverting Output for Right Channel.
28, 29	OUTR+	Noninverting Output for Right Channel.
30	BOOTR+	Bootstrap Input/Output for Right Channel, Noninverting Output.
31, 32, 33, 38, 39, 40	PGND	Power Stage Ground.
34, 35, 36, 37	PVDD	Power Stage Power Supply.
	Exposed Pad	Thermal Exposed Pad. Use multiple vias to connect this pad to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise stated, all data at PVDD = 12 V, EDGE = low, MONO = low, REGEN = high, and GAIN = 9 dB.

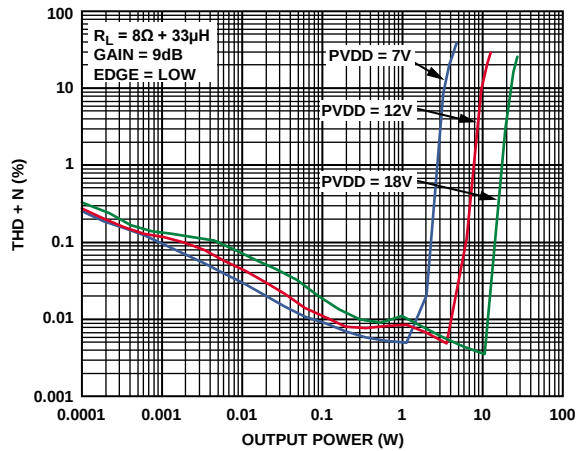


Figure 3. THD + N vs. Output Power into 8 Ω;
PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

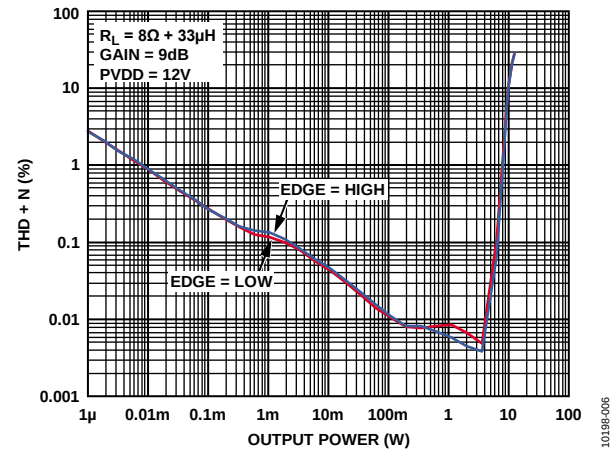


Figure 6. THD + N vs. Output Power into 8 Ω;
EDGE = High, EDGE = Low

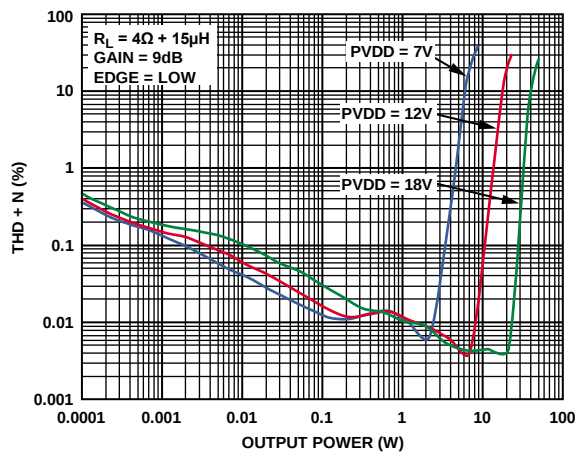


Figure 4. THD + N vs. Output Power into 4 Ω;
PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

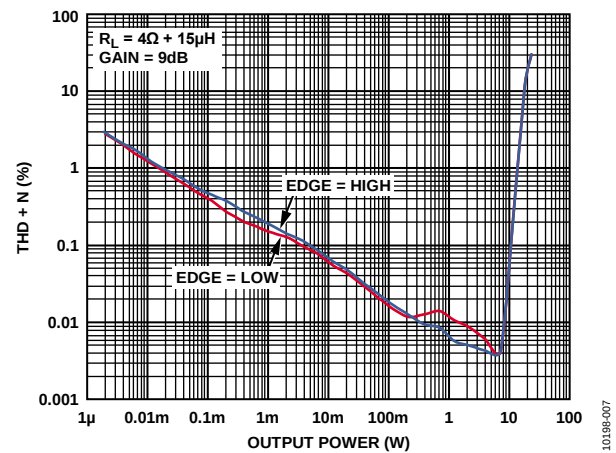


Figure 7. THD + N vs. Output Power into 4 Ω;
EDGE = High, EDGE = Low

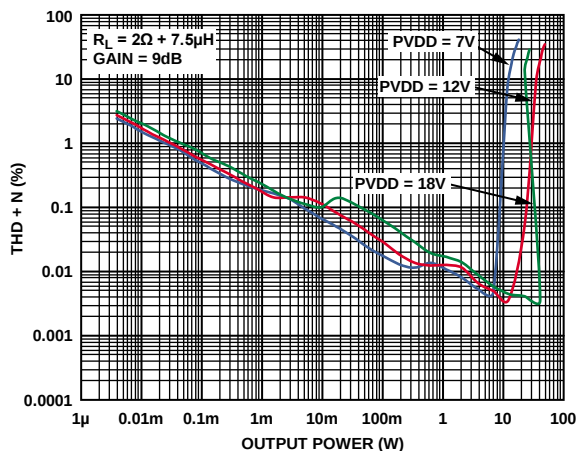


Figure 5. THD + N vs. Output Power into 2 Ω;
Mono Mode; Gain = 9 dB; PVDD = 7 V, PVDD = 12 V, 1 PVDD = 8 V

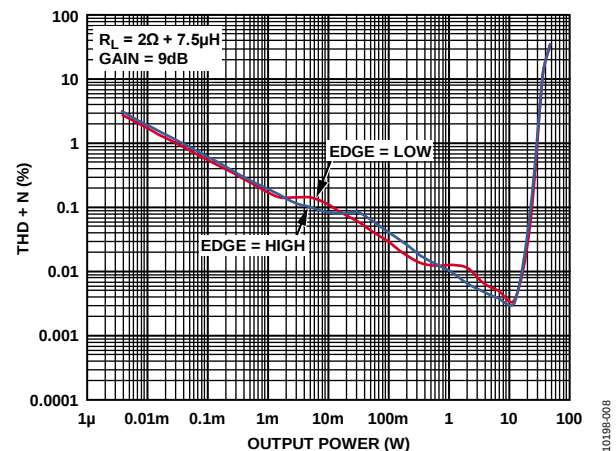
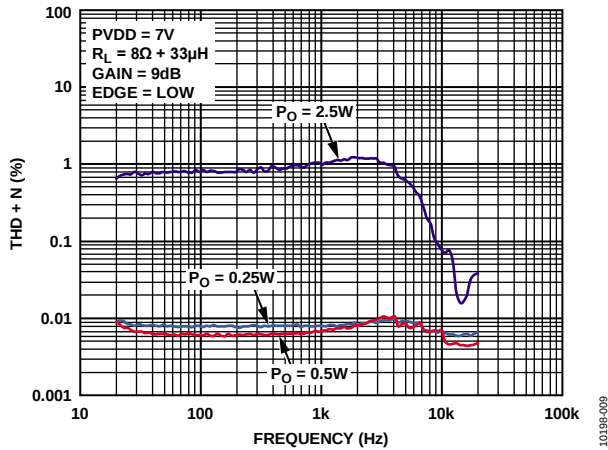
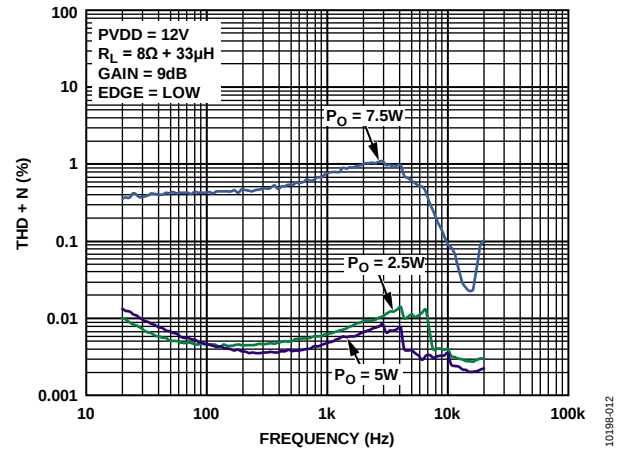


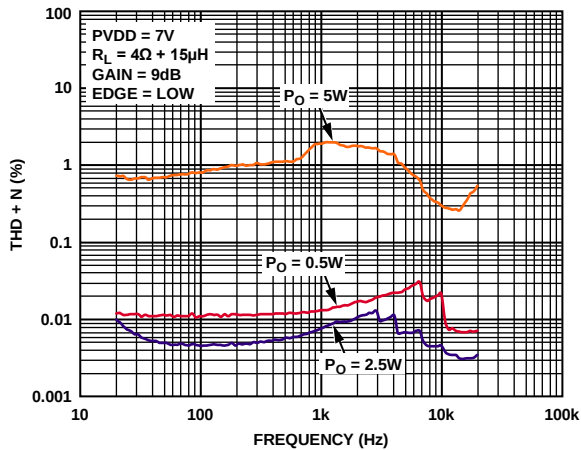
Figure 8. THD + N vs. Output Power into 2 Ω;
EDGE = High, EDGE = Low



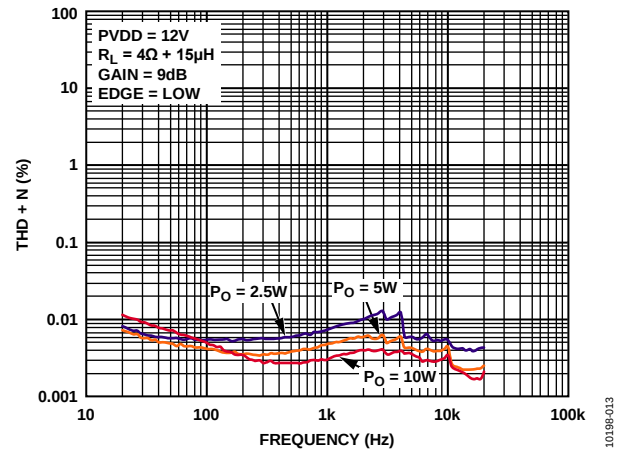
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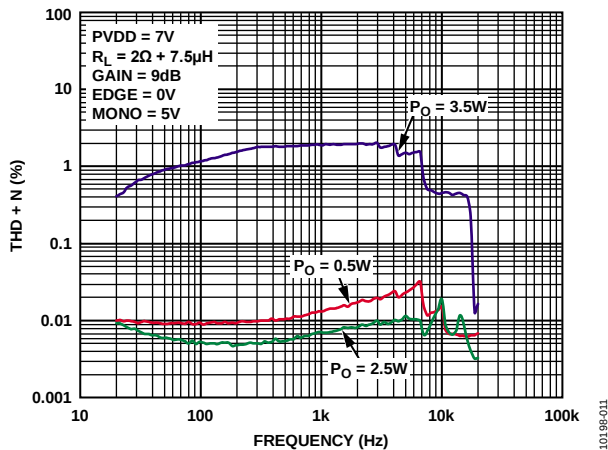
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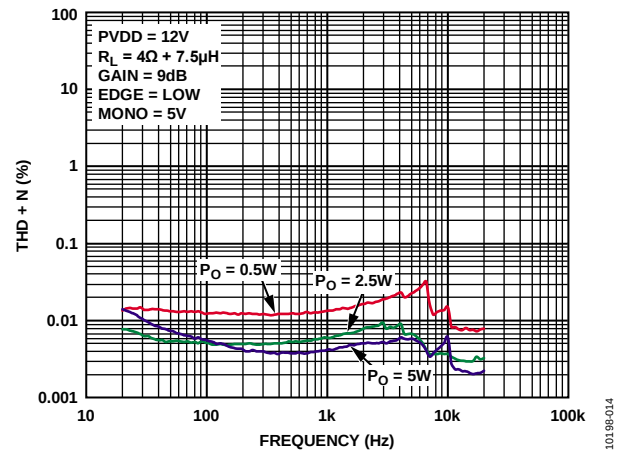
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10198-013



10198-011



10198-014

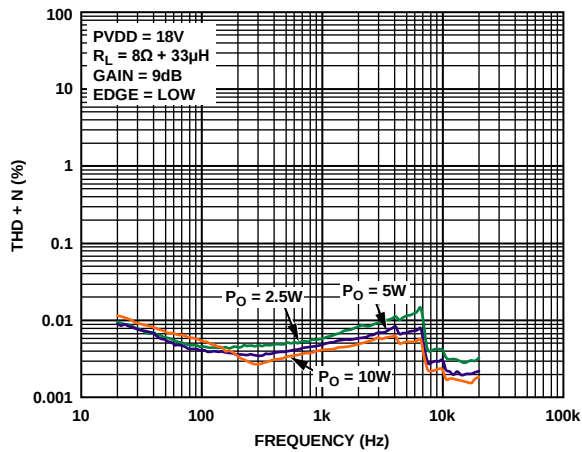


Figure 15. THD + N vs. Frequency;
 $R_L = 8\Omega$; $PVDD = 18V$; $P_O = 2.5W$, $P_O = 5W$, $P_O = 10W$

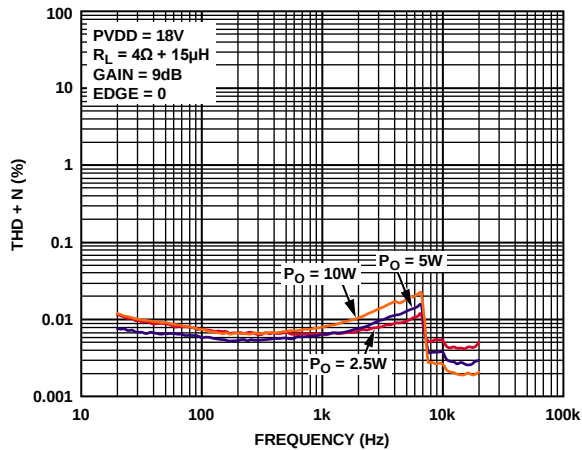


Figure 16. THD + N vs. Frequency;
 $R_L = 4\Omega$; $PVDD = 18V$; $P_O = 2.5W$, $P_O = 5W$, $P_O = 10W$

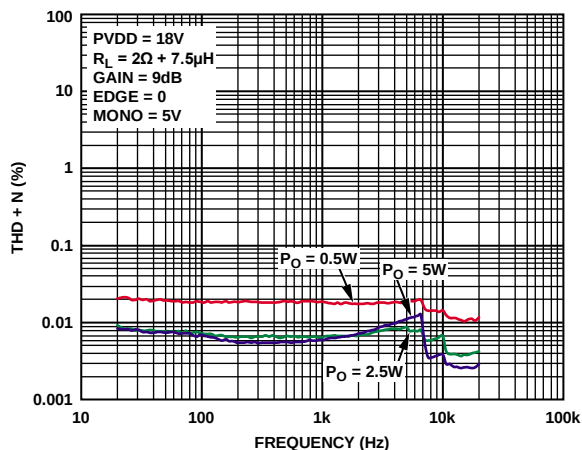


Figure 17. THD + N vs. Frequency;
 $R_L = 2\Omega$; Mono Mode; $PVDD = 18V$; $P_O = 0.5W$, $P_O = 2.5W$, $P_O = 5W$

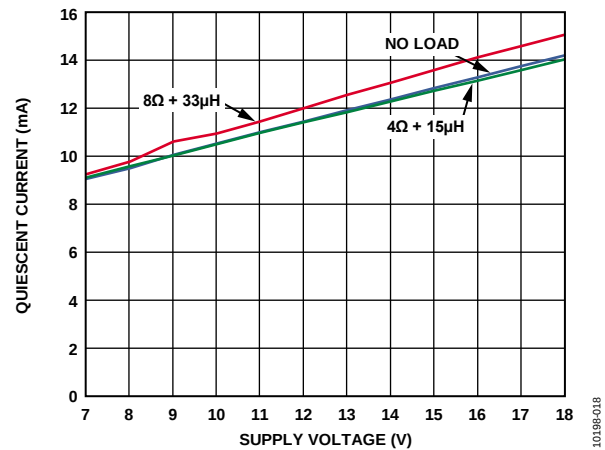


Figure 18. Quiescent Current vs. Supply Voltage,
 $R_L = 8\Omega + 33\mu H$, No Load, $R_L = 4\Omega + 15\mu H$

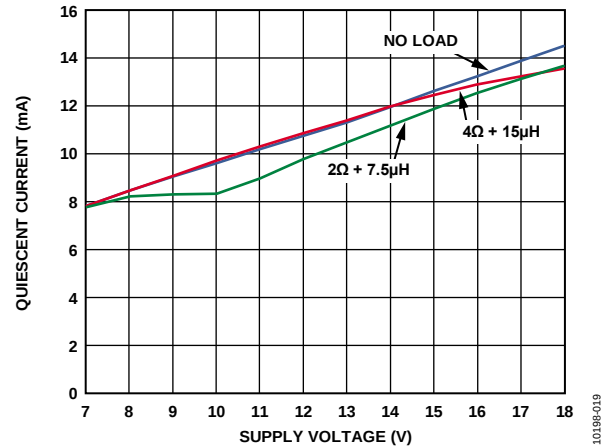


Figure 19. Quiescent Current vs. Supply Voltage,
Mono Mode, No Load, $R_L = 4\Omega + 15\mu H$, $R_L = 2\Omega + 7.5\mu H$

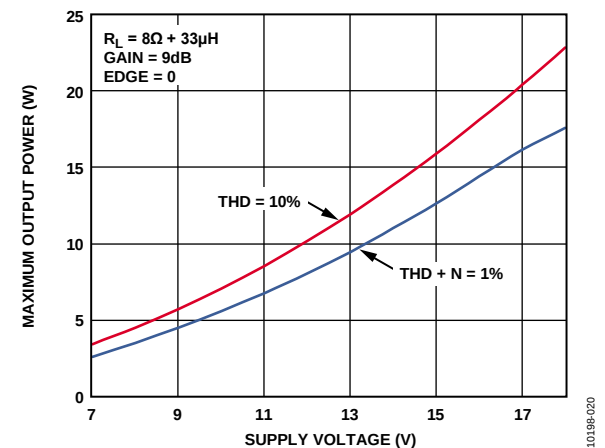


Figure 20. Maximum Output Power vs. Supply Voltage;
 $R_L = 8\Omega$; $THD + N = 1\%$, $THD + N = 10\%$

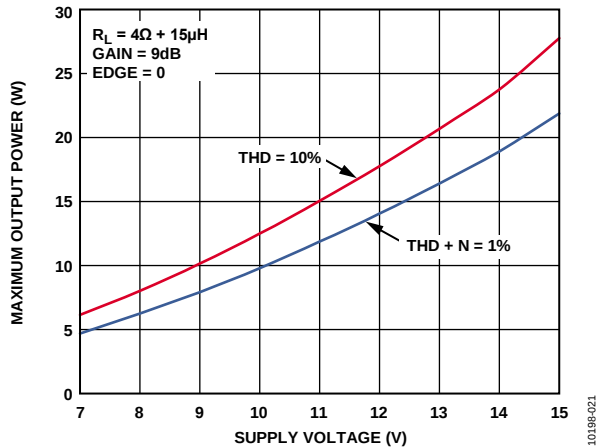


Figure 21. Maximum Output Power vs. Supply Voltage;
 $R_L = 4\Omega$; THD + N = 1%, THD + N = 10%

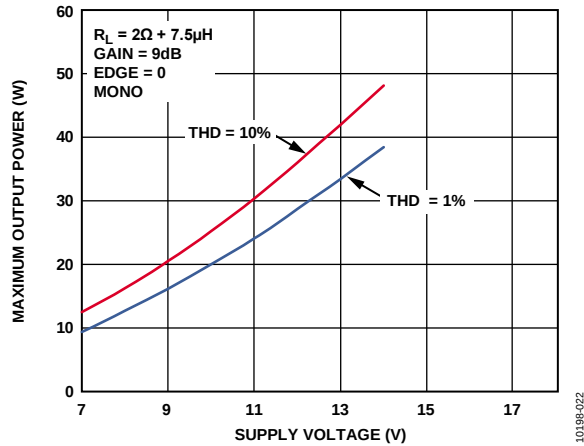


Figure 22. Maximum Output Power vs. Supply Voltage;
 $R_L = 2\Omega$; Mono Mode; THD + N = 1%, THD + N = 10%

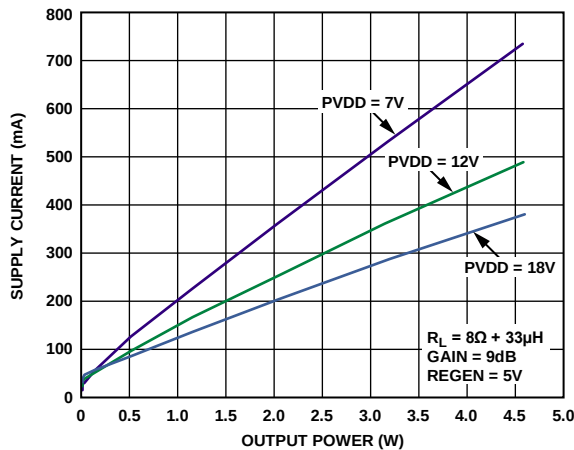


Figure 23. Supply Current vs. Output Power into 8Ω;
 PVDD = 7V, PVDD = 12V, PVDD = 18V

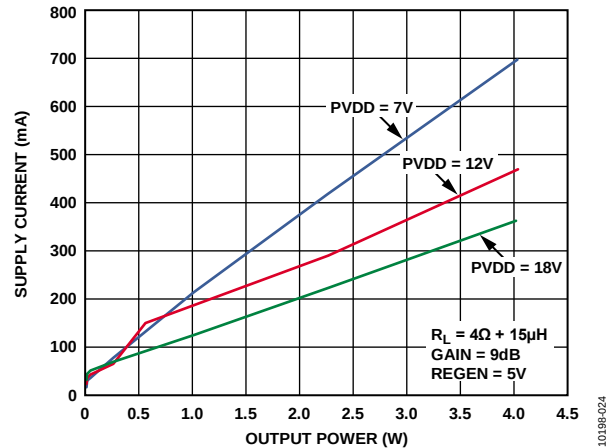


Figure 24. Supply Current vs. Output Power into 4Ω;
 PVDD = 7V, PVDD = 12V, PVDD = 18V

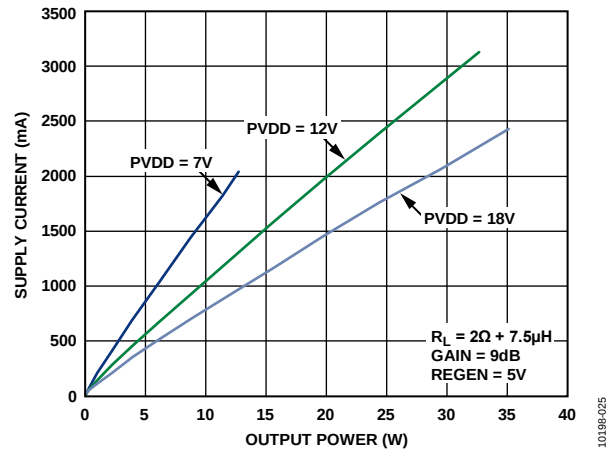


Figure 25. Supply Current vs. Output Power into 2Ω;
 Mono Mode; PVDD = 7V, PVDD = 12V, PVDD = 18V

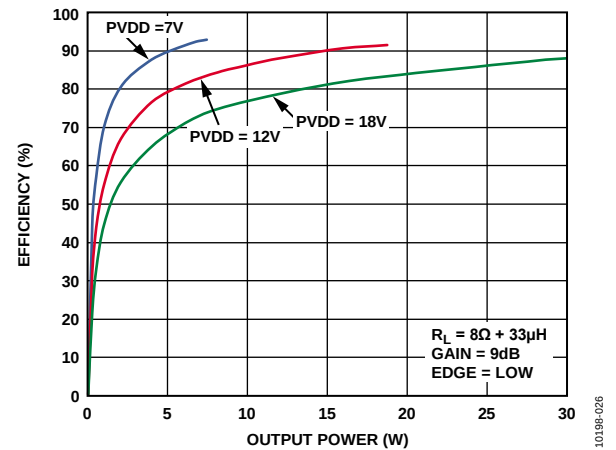


Figure 26. Efficiency vs. Output Power into 8Ω;
 PVDD = 7V, PVDD = 12V, PVDD = 18V

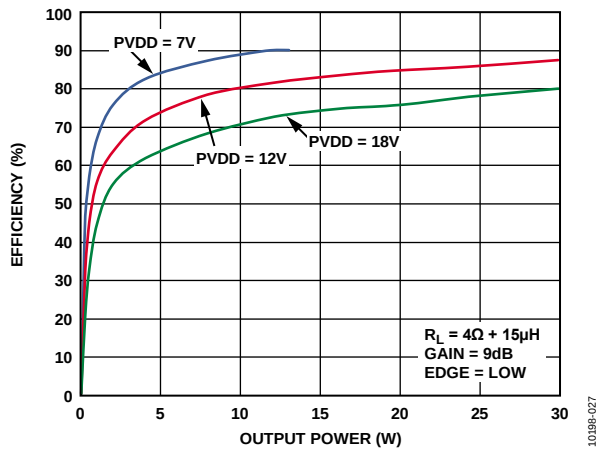


Figure 27. Efficiency vs. Output Power into 4Ω;
PVDD = 7V, PVDD = 12V, PVDD = 18V

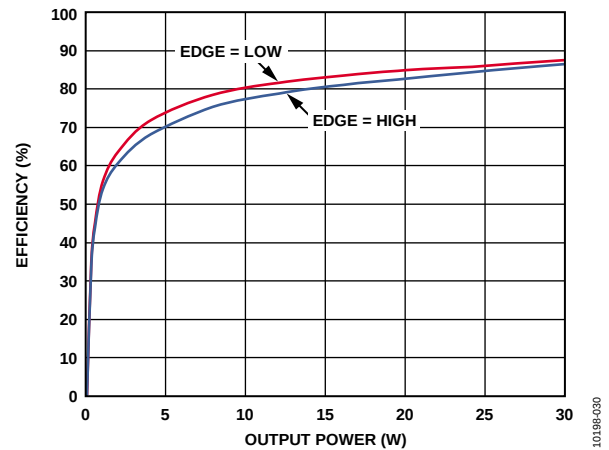


Figure 30. Efficiency vs. Output Power into 4Ω;
PVDD = 12V; EDGE = High, EDGE = Low

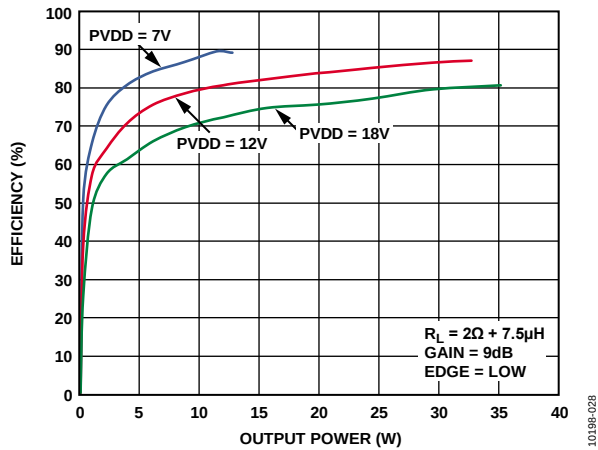


Figure 28. Efficiency vs. Output Power into 2Ω;
Mono Mode; PVDD = 7V, PVDD = 12V, PVDD = 18V

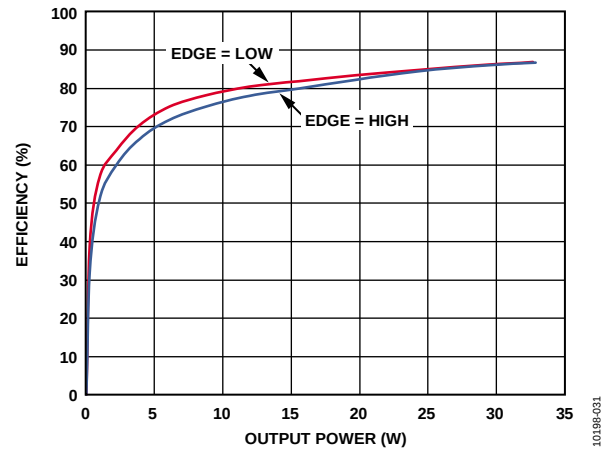


Figure 31. Efficiency vs. Output Power into 2Ω;
Mono Mode; PVDD = 12V; EDGE = High, EDGE = Low

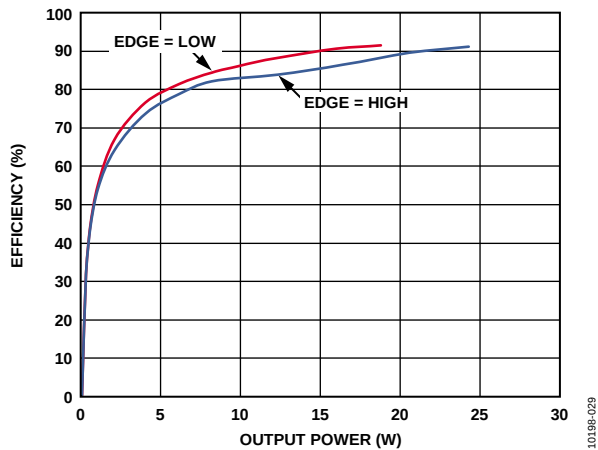


Figure 29. Efficiency vs. Output Power into 8Ω;
PVDD = 12V; EDGE = High, EDGE = Low

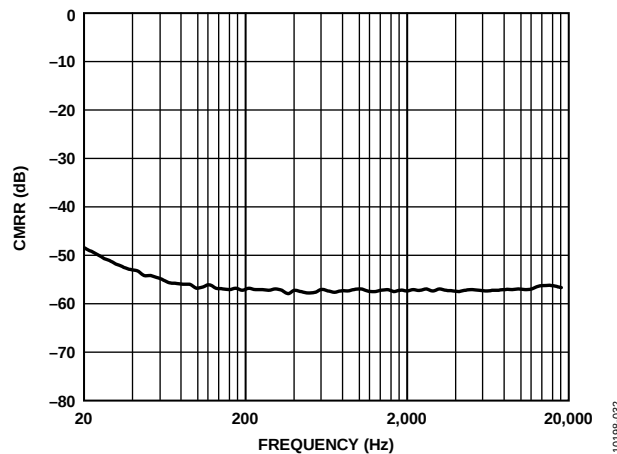


Figure 32. CMRR vs. Frequency, $V_{RIPPLE} = 100\text{ mV rms}$, AC-Coupled

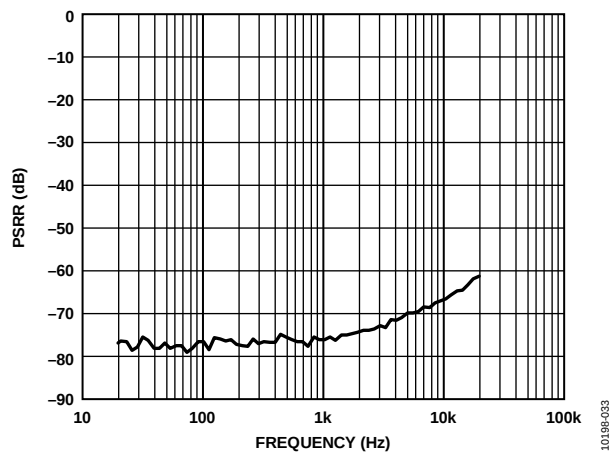


Figure 33. PSRR vs. Frequency, $V_{\text{RIPPLE}} = 100 \text{ mV rms}$

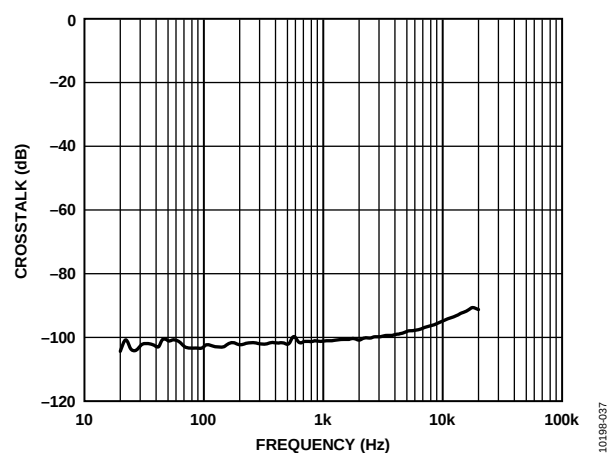


Figure 34. Crosstalk vs. Frequency,
 $P_O = 0.5 \text{ W}$, $R_L = 8 \Omega$

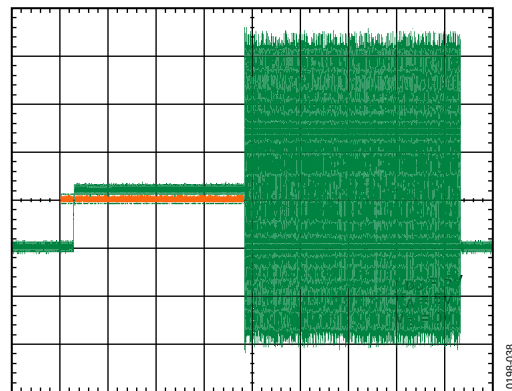


Figure 35. Turn-On Response
(Showing SDNL Pin or SDNR Pin Rising Edge and Output)

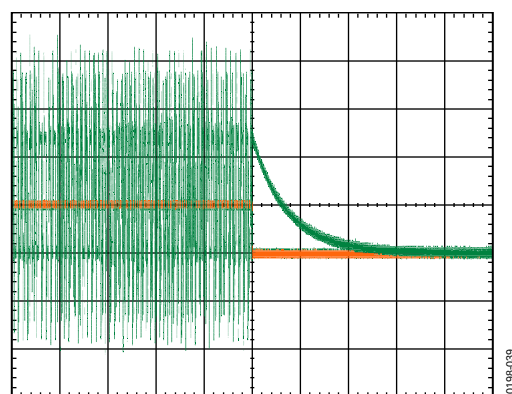


Figure 36. Turn-Off Response
(Showing SDNL Pin or SDNR Pin Falling Edge and Output)

TYPICAL APPLICATION CIRCUITS

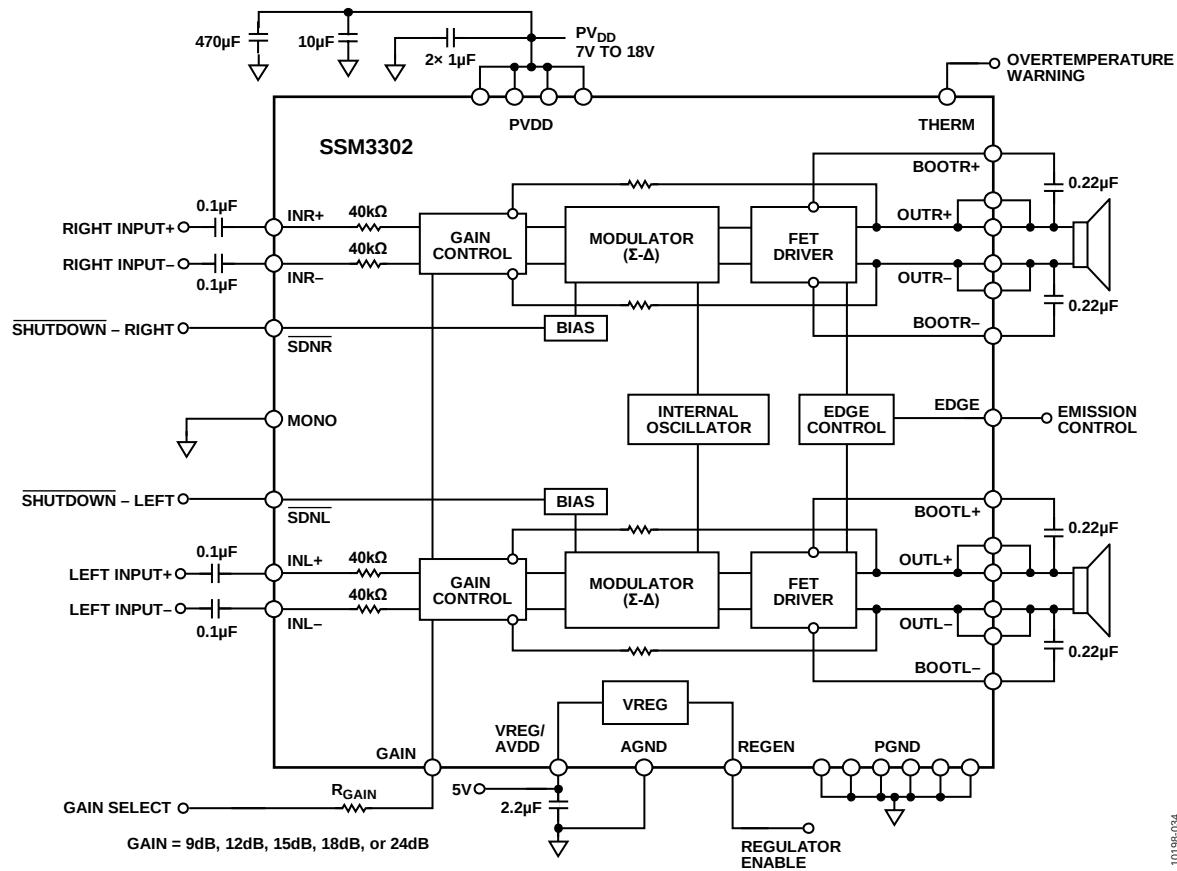


Figure 37. Stereo Mode Configuration

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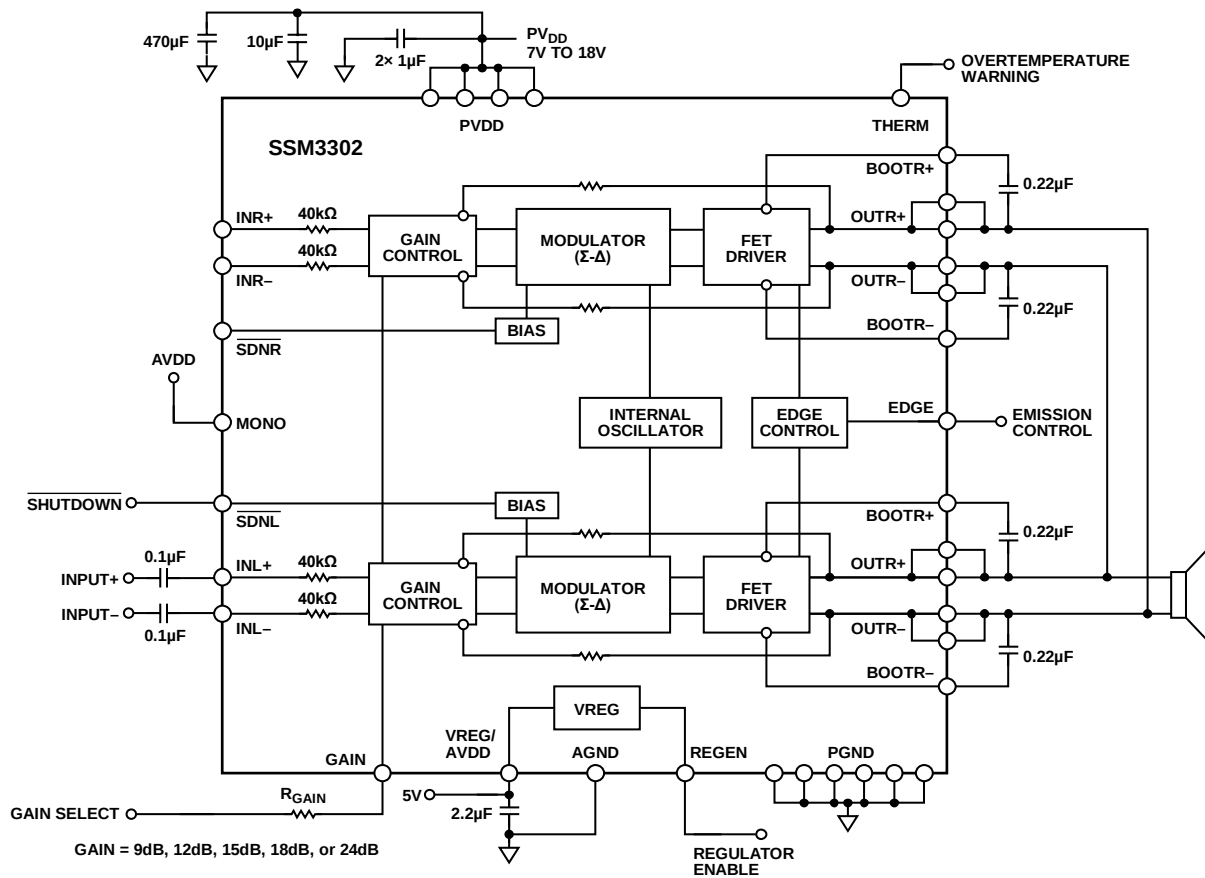


Figure 38. Mono Mode Configuration

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APPLICATIONS INFORMATION

OVERVIEW

The [SSM3302](#) stereo Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and reducing system cost. The [SSM3302](#) does not require an output filter; it relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to recover the audio component of the square wave output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the [SSM3302](#) uses Σ - Δ modulation to determine the switching pattern of the output devices, resulting in several important benefits. Unlike pulse-width modulators, Σ - Δ modulators do not produce a sharp peak with many harmonics in the AM broadcast band. In addition, Σ - Δ modulation reduces the amplitude of spectral components at high frequencies, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. Due to the inherent spread spectrum nature of Σ - Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple [SSM3302](#) amplifiers.

The [SSM3302](#) also integrates overcurrent and overtemperature protection, as well as an overtemperature warning indicator pin.

ANALOG SUPPLY

The [SSM3302](#) includes an integrated low dropout (LDO) linear regulator to generate a 5 V supply for the input stage. This regulator can be enabled using the REGEN pin. This analog supply voltage is available at the VREG/AVDD pin. Connect a 2.2 μ F decoupling capacitor from this pin to the AGND pin.

Alternatively, an external 5 V analog supply can be connected to the AVDD pin. In this case, tie REGEN low to disable the internal regulator.

The internal 5 V regulator can supply up to 20 mA of current to the VREG pin if other analog circuits use the same supply. The regulator includes short-circuit protection, but no current limiter or other protection is provided.

GAIN SELECTION

The preset gain of [SSM3302](#) can be selected between 9 dB and 24 dB with one external resistor and no change to the input impedance. Gain can be further adjusted to a user-defined setting by inserting series external resistors at the inputs. A major benefit of fixed input impedance is that there is no need to recalculate the input corner frequency (f_c) when gain is adjusted. The same input coupling components can be used for all gain settings.

Table 5. Gain Function Descriptions

Gain Setting (dB)	GAIN Pin Configuration
24	Tie to AVDD
18	Tie to AVDD through 47 k Ω
15	Open
12	Tie to AGND through 47 k Ω
9	Tie to AGND

AMPLIFIER PROTECTION

The [SSM3302](#) includes protection circuitry to prevent damage in case of overcurrent and overtemperature conditions. Shorts across the output terminals, or between either terminal and PVDD or PGND, are also detected; in this case, the output transistors do not switch until the fault is removed.

If the temperature exceeds the threshold temperature (approximately 145°C), the chip is disabled until the temperature drops below the recovery threshold (85°C). This hysteresis prevents rapid cycling of the output at high temperatures.

Additionally, a temperature warning signal is available on the THERM pin. If the die temperature rises above 120°C, a logic high is output on this pin.

POP-AND-CLICK SUPPRESSION

Voltage transients at the outputs of the audio amplifiers may occur when shutdown is activated or deactivated. Voltage transients as small as 10 mV can be heard as an audible pop in the speaker. Clicks and pops are defined as undesirable audible transients generated by the amplifier system that do not come from the system input signal.

Such transients may be generated when the amplifier system changes its operating mode. For example, system power-up and power-down can be sources of audible transients.

The [SSM3302](#) has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

EMI NOISE

The [SSM3302](#) uses a proprietary modulation and spread spectrum technology to minimize EMI emissions from the device. The [SSM3302](#) can pass FCC Class-B emissions testing with unshielded 20 inch cable using ferrite bead-based filtering. For applications that have difficulty passing FCC Class-B emission tests, the [SSM3302](#) includes a modulation select pin (ultralow EMI emission mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. Note that reducing the supply voltage greatly reduces radiated emissions.

MONO MODE

The [SSM3302](#) can also be configured to stack its stereo outputs into a monaural amplifier configuration by enabling the mono output mode using the MONO pin. The user can drive a load as small as 2 Ω up to 20 W continuous output power—a particularly useful feature for driving the subwoofer in a 2.1 audio system.

To activate this operation, pull up the MONO pin to the level of VREG/AVDD. In mono mode, OUTL+ and OUTR+ (Pin 2/Pin 3 and Pin 28/Pin 29) provide the noninverting output, and OUTL– and OUTR– (Pin 4/Pin 5 and Pin 26/Pin 27) provide the inverting output. While the device is in mono mode, audio input is taken only from the left channel set of inputs: INL+ and INL– (Pin 11 and Pin 12).

Because the mono mode uses output sense circuitry attached to the left channel outputs, run PCB traces directly from the speaker to the left channel outputs and then extend the PCB traces to the right channel outputs.

OUTPUT MODULATION DESCRIPTION

The [SSM3302](#) uses three-level, Σ - Δ output modulation. Each output can swing from PGND to PVDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, however, there are always noise sources present.

Due to this constant presence of noise, a differential pulse is occasionally generated in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated. However, most of the time, the output differential voltage is 0 V. This feature ensures that the current flowing through the inductive load is small.

When the user sends an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 39 depicts three-level, Σ - Δ output modulation with and without input stimulus.

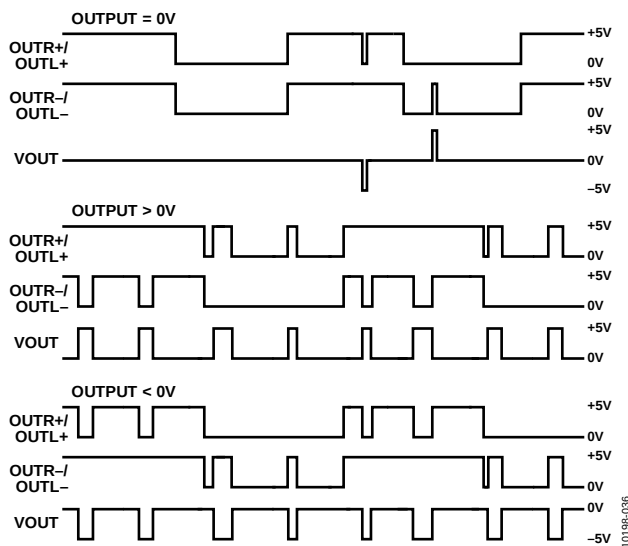


Figure 39. Three-Level, Σ - Δ Output Modulation With and Without Input Stimulus

LAYOUT

As output power increases, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply; a poor layout increases voltage drops, consequently decreasing efficiency. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. For lowest DCR

and minimum inductance, ensure that track widths are at least 200 mil for every inch of length and use 1 oz. or 2 oz. copper. Use large traces for the power supply inputs and amplifier outputs. Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal.

To maintain high output swing and high peak output power, ensure that the PCB traces that connect the output pins to the load and supply pins are as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances. In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate ground planes for small signal and high power connections, there should be no overlap between these planes. Stitch the power plane to the [SSM3302](#) exposed pad using multiple vias. Proper layout improves heat conduction into the board, allowing operation at larger output power levels without overtemperature issues.

INPUT CAPACITOR SELECTION

Input capacitors are required if the input signal is not biased within the recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the [SSM3302](#) form a high-pass filter with a corner frequency determined by the following equation:

$$f_c = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Failure to use input capacitors degrades the output offset of the amplifier.

BOOTSTRAP CAPACITORS

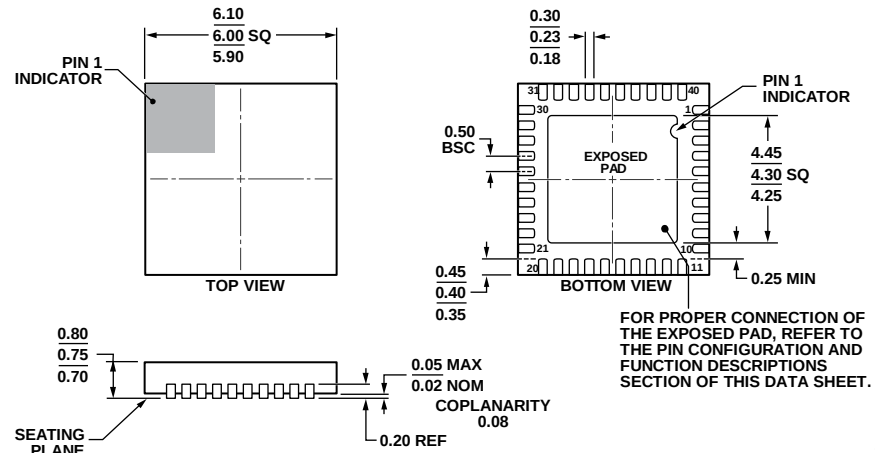
The output stage of the [SSM3302](#) uses a high-side NMOS driver, rather than PMOS driver. To generate the gate drive voltage for the high-side NMOS driver, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Using 0.22 μ F ceramic capacitors with a voltage rating of 35 V or greater is recommended.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion, and high power supply rejection ratio, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. Decouple the power supply input with a good quality, low ESL, low ESR bulk capacitor larger than 220 μF . This capacitor bypasses low frequency noises to the ground plane.

For high frequency transient noises, place two separate 1 μF capacitors as close as possible to the PVDD pins of the device. Connect one of the 1 μF capacitors between the left-side PVDD terminals and PGND terminals, and connect the other 1 μF capacitor between the right-side PVDD terminals and PGND terminals. Placing the decoupling capacitor as close as possible to the [SSM3302](#) helps to achieve the best performance.

OUTLINE DIMENSIONS



ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
SSM3302ACPZ	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP_WQ]	CP-40-10
SSM3302ACPZ-RL	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP_WQ]	CP-40-10
SSM3302ACPZ-R7	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP_WQ]	CP-40-10
EVAL-SSM3302Z		Evaluation Board	

¹ Z = RoHS Compliant Part.

NOTES