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10/02—Rev. A to Rev. B

5/02—Rev. 0 to Rev. A

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω, C_B = 0.1 μF, V_{CM} = V_{DD}/2, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL CHARACTERISTICS						
Differential Output Offset Voltage	V_{OOS}	A_{VD} = 2, −40°C ≤ T_A ≤ +85°C		4	50	mV
Output Impedance	Z_{OUT}			0.1		Ω
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} = <100 mA	3.0			V
Input Voltage Low	V_{IL}	I_{SY} = normal			1.3	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.75 V to 5.25 V		66		dB
Supply Current	I_{SY}	$V_{OUT}A$ = $V_{OUT}B$ = 2.5 V, −40°C ≤ T_A ≤ +85°C		9.5	20	mA
Supply Current, Shutdown Mode	I_{SD}	Pin 1 = V_{DD} (see Figure 32), −40°C ≤ T_A ≤ +85°C		0.1	1	μA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$Φ_M$			86		Degrees
AUDIO PERFORMANCE						
Total Harmonic Distortion	THD + N	P = 0.5 W into 8 Ω, f = 1 kHz		0.15		%
Total Harmonic Distortion	THD + N	P = 1.0 W into 8 Ω, f = 1 kHz		0.2		%
Voltage Noise Density	e_n	f = 1 kHz		85		nV√Hz

V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω, C_B = 0.1 μF, V_{CM} = V_{DD}/2, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL CHARACTERISTICS						
Differential Output Offset Voltage	V_{OOS}	A_{VD} = 2, −40°C ≤ T_A ≤ +85°C		5	50	mV
Output Impedance	Z_{OUT}			0.1		Ω
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} = <100 μA	1.7			V
Input Voltage Low	V_{IL}	I_{SY} = normal			1	V
POWER SUPPLY						
Supply Current	I_{SY}	$V_{OUT}A$ = $V_{OUT}B$ = 1.65 V, −40°C ≤ T_A ≤ +85°C		5.2	20	mA
Supply Current, Shutdown Mode	I_{SD}	Pin 1 = V_{DD} (see Figure 32), −40°C ≤ T_A ≤ +85°C		0.1	1	μA
AUDIO PERFORMANCE						
Total Harmonic Distortion	THD + N	P = 0.35 W into 8 Ω, f = 1 kHz		0.1		%

V_{DD} = 2.7 V, T_A = 25°C, R_L = 8 Ω, C_B = 0.1 µF, V_{CM} = V_{DD}/2, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL CHARACTERISTICS						
Differential Output Offset Voltage	V_{OOS}	A_{VD} = 2		5	50	mV
Output Impedance	Z_{OUT}			0.1		Ω
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} = <100 mA	1.5			V
Input Voltage Low	V_{IL}	I_{SY} = normal			0.8	V
POWER SUPPLY						
Supply Current	I_{SY}	$V_{OUT}A$ = $V_{OUT}B$ = 1.35 V, −40°C ≤ T_A ≤ +85°C		4.2	20	mA
Supply Current, Shutdown Mode	I_{SD}	Pin 1 = V_{DD} (see Figure 32), −40°C ≤ T_A ≤ +85°C		0.1	1	µA
AUDIO PERFORMANCE						
Total Harmonic Distortion	THD + N	P = 0.25 W into 8 Ω, f = 1 kHz		0.1		%

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
ESD Susceptibility	2000 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

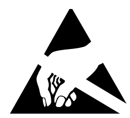
θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP (CP-Suffix)[1]	50	75	°C/W
8-Lead SOIC_N (S-Suffix)[2]	121	43	°C/W

[1] For the LFCSP, θ_{JA} is measured with exposed lead frame soldered to the PCB.
[2] For the SOIC_N, θ_{JA} is measured with the device soldered to a 4-layer PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

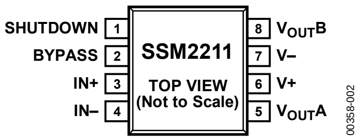


Figure 2. 8-Lead SOIC_N Pin Configuration (R-8)

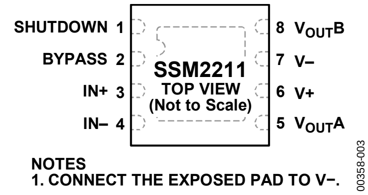


Figure 3. 8-Lead LFCSP Pin Configuration (CP-8-13)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SHUTDOWN	Shutdown Enable.
2	BYPASS	Bypass Capacitor.
3	IN+	Noninverting Input.
4	IN–	Inverting Input.
5	$V_{OUT}A$	Output A.
6	V+	Positive Supply.
7	V–	Negative Supply.
8	$V_{OUT}B$	Output B.
	EPAD	Exposed Pad. Connect the exposed pad to V–.

TYPICAL PERFORMANCE CHARACTERISTICS

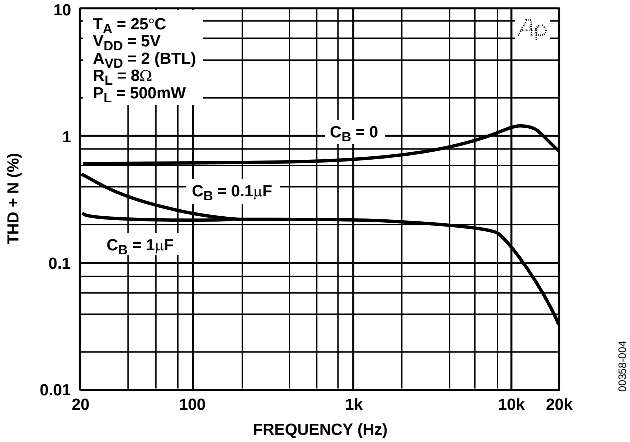


Figure 4. THD + N vs. Frequency

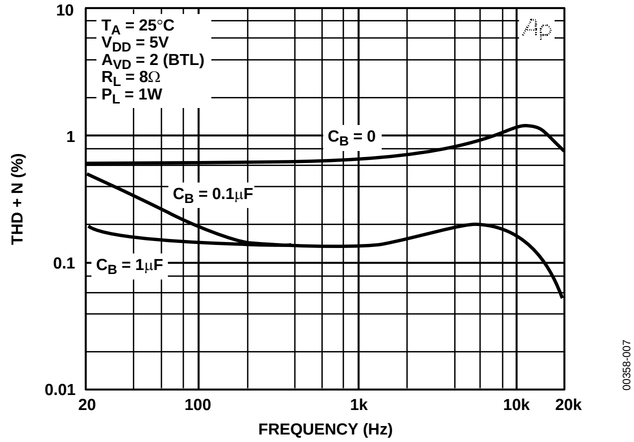


Figure 7. THD + N vs. Frequency

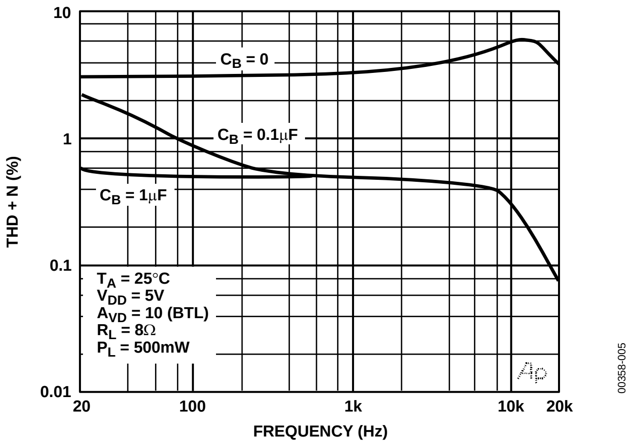


Figure 5. THD + N vs. Frequency

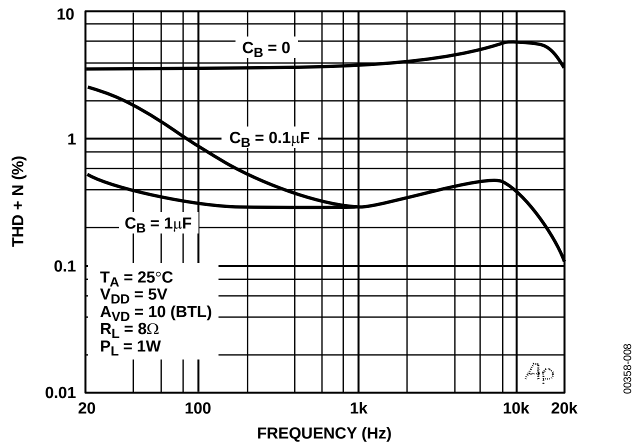


Figure 8. THD + N vs. Frequency

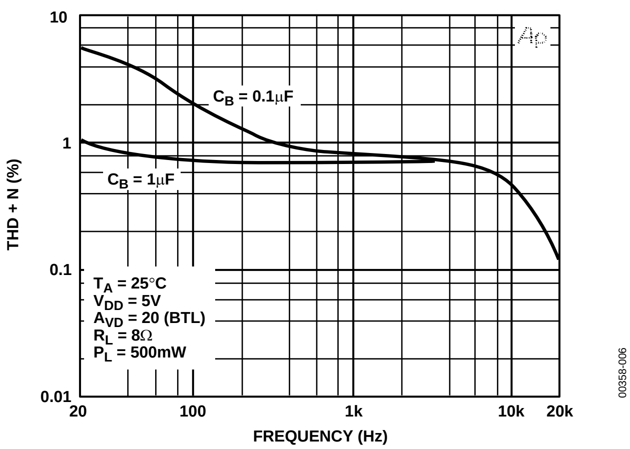


Figure 6. THD + N vs. Frequency

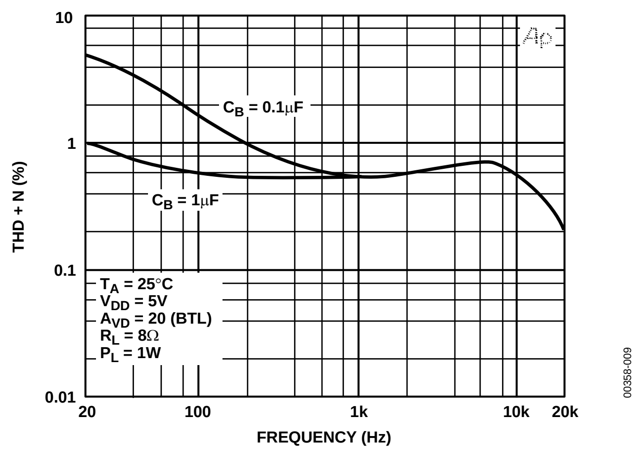


Figure 9. THD + N vs. Frequency

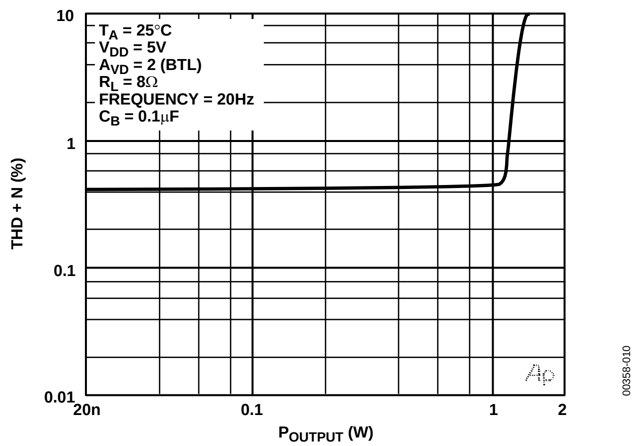


Figure 10. THD + N vs. P_{OUTPUT}

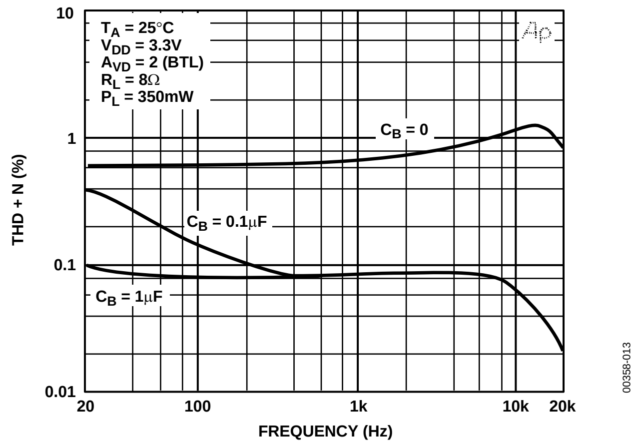


Figure 13. THD + N vs. Frequency

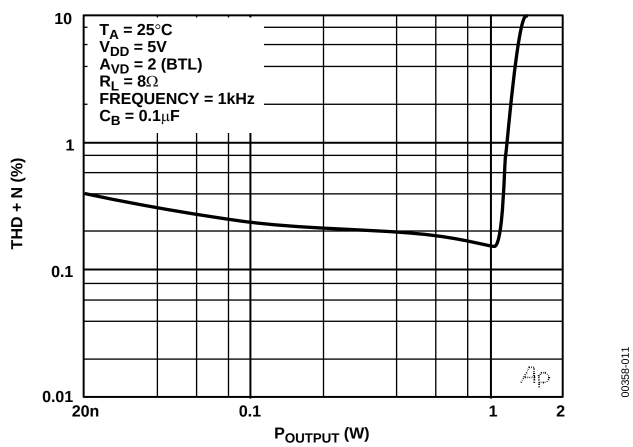


Figure 11. THD + N vs. P_{OUTPUT}

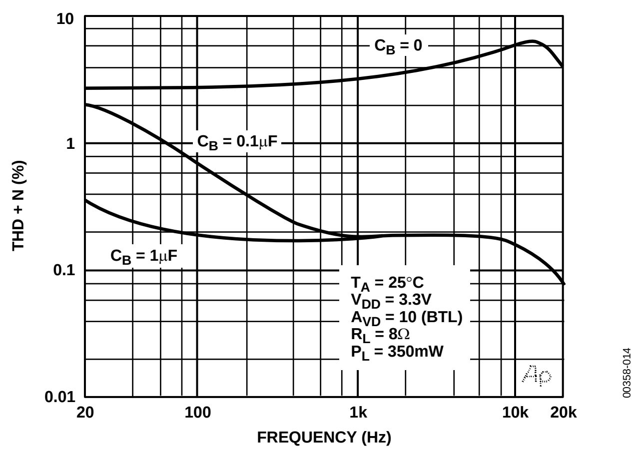


Figure 14. THD + N vs. Frequency

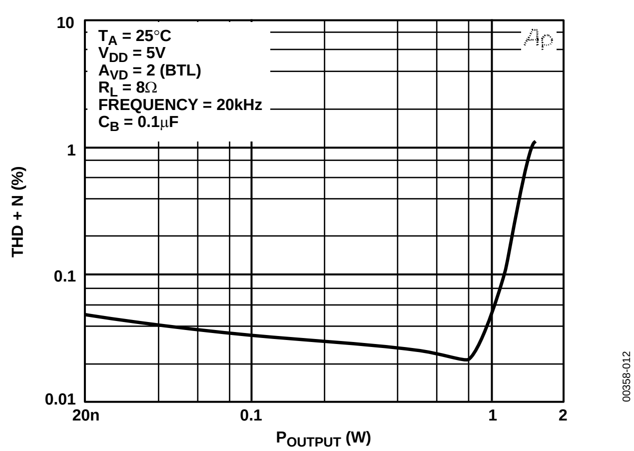


Figure 12. THD + N vs. P_{OUTPUT}

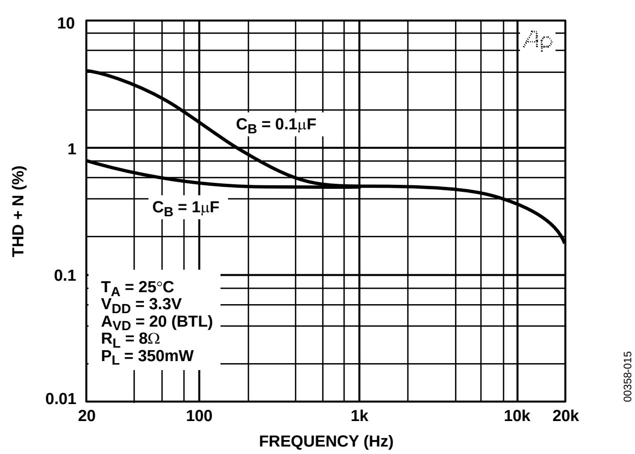


Figure 15. THD + N vs. Frequency

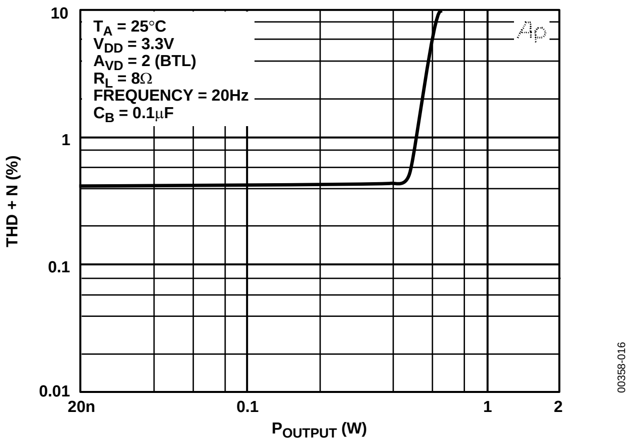


Figure 16. THD + N vs. P_{OUTPUT}

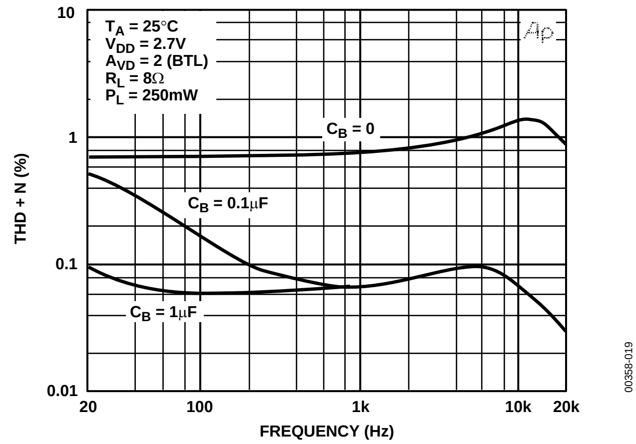


Figure 19. THD + N vs. Frequency

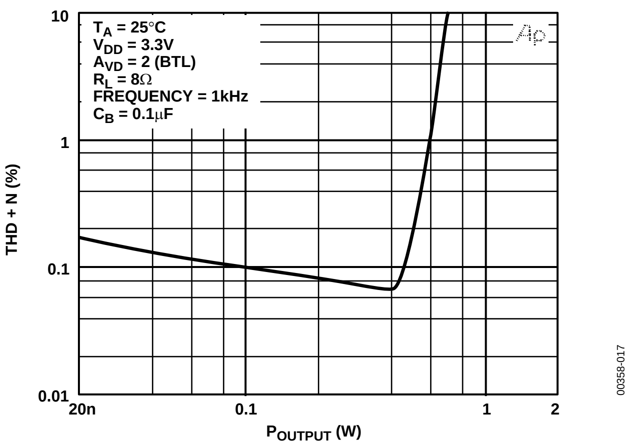


Figure 17. THD + N vs. P_{OUTPUT}

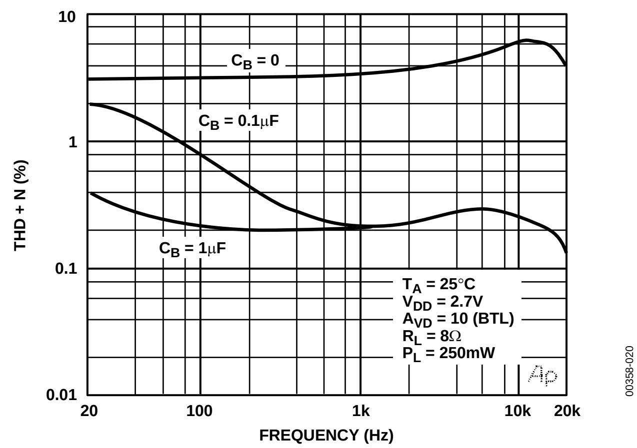


Figure 20. THD + N vs. Frequency

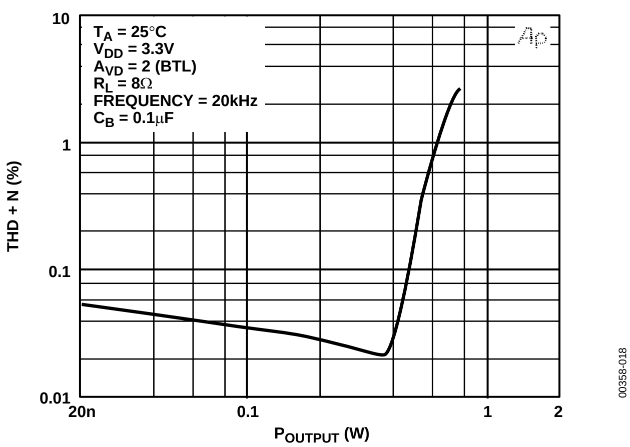


Figure 18. THD + N vs. P_{OUTPUT}

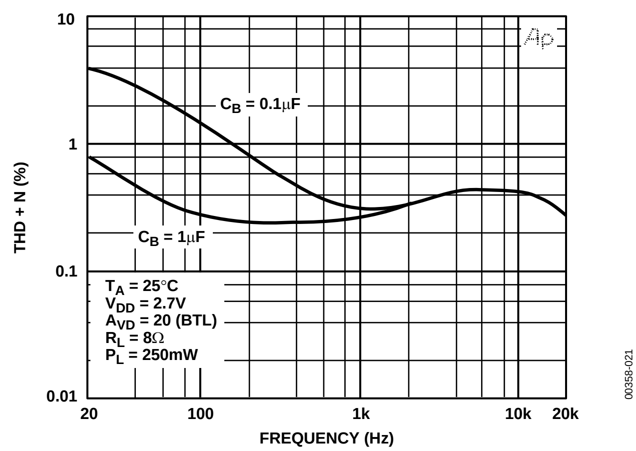


Figure 21. THD + N vs. Frequency

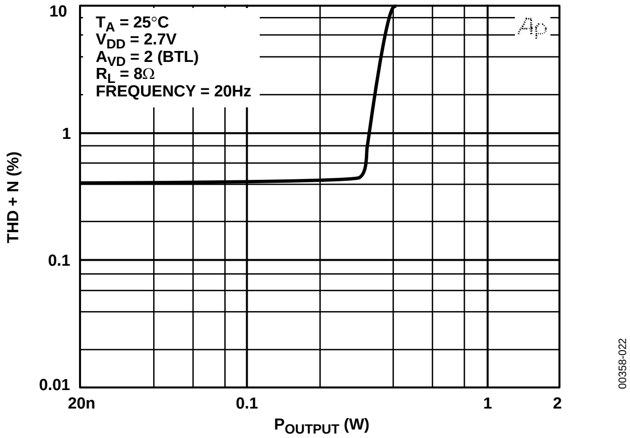


Figure 22. THD + N vs. P_{OUTPUT}

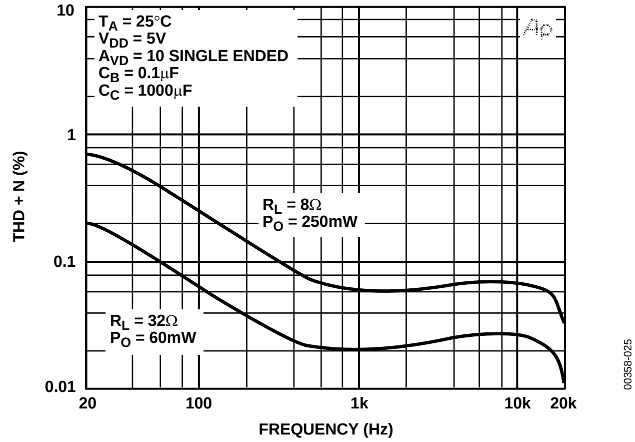


Figure 25. THD + N vs. Frequency

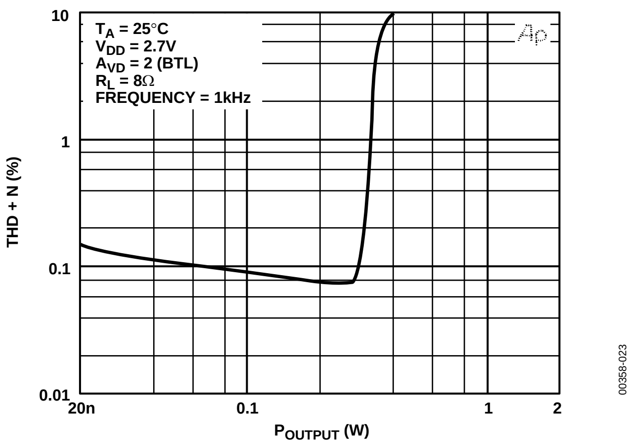


Figure 23. THD + N vs. P_{OUTPUT}

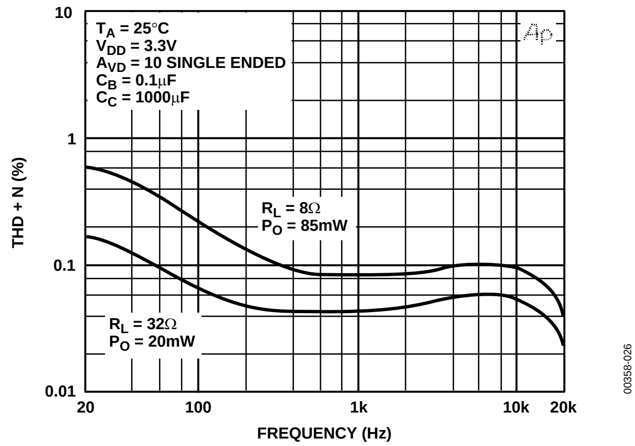


Figure 26. THD + N vs. Frequency

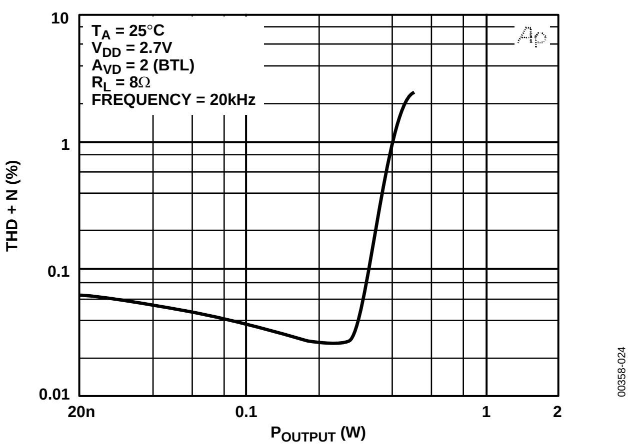


Figure 24. THD + N vs. P_{OUTPUT}

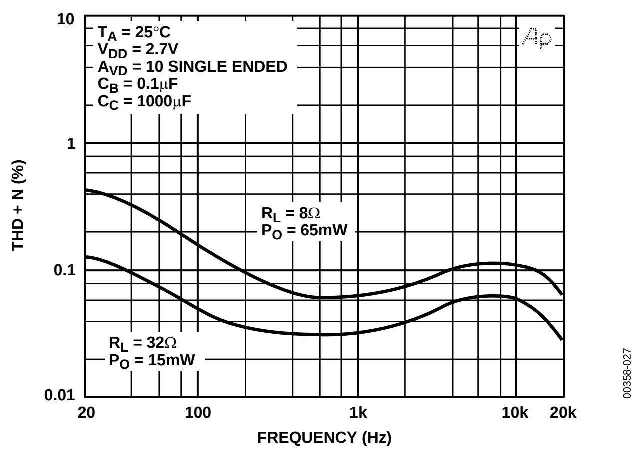


Figure 27. THD + N vs. Frequency

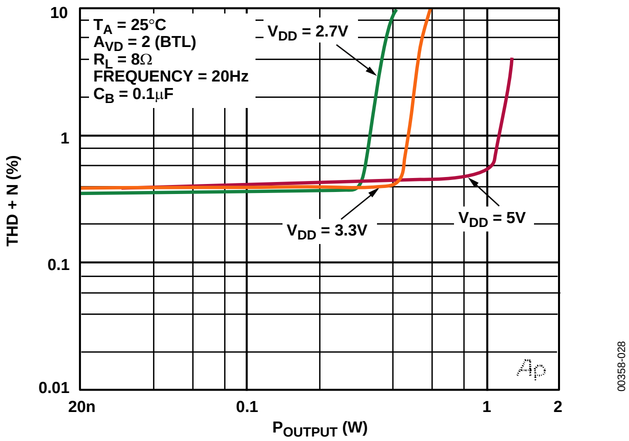


Figure 28. THD + N vs. P_{OUTPUT}

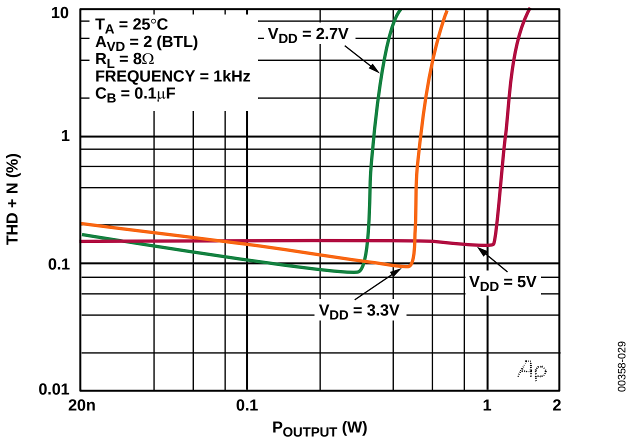


Figure 29. THD + N vs. P_{OUTPUT}

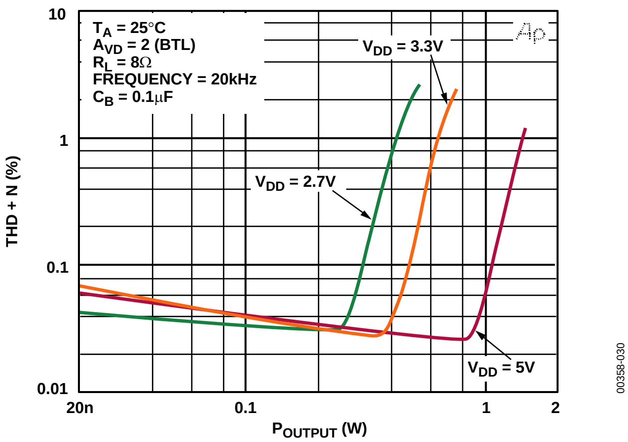


Figure 30. THD + N vs. P_{OUTPUT}

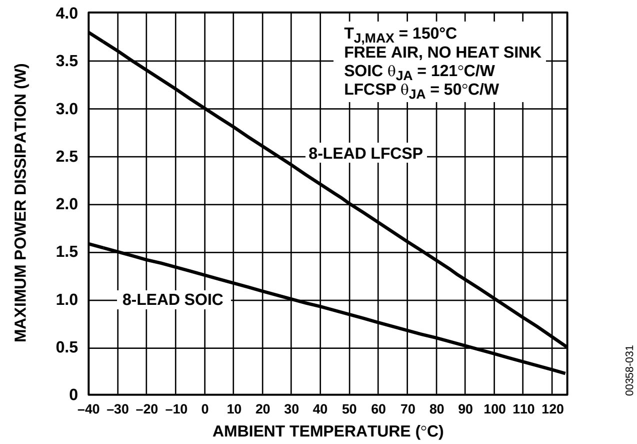


Figure 31. Maximum Power Dissipation vs. Ambient Temperature

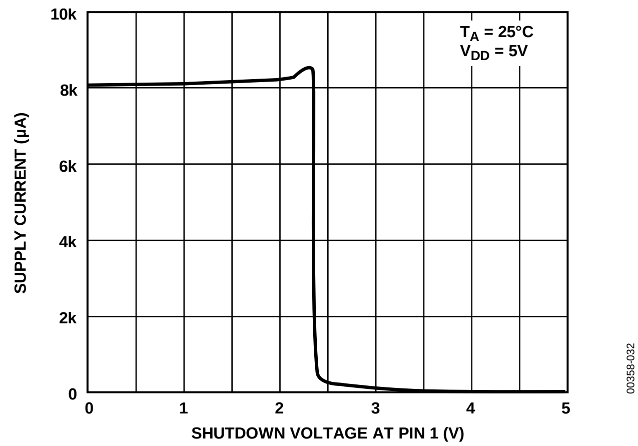


Figure 32. Supply Current vs. Shutdown Voltage at Pin 1

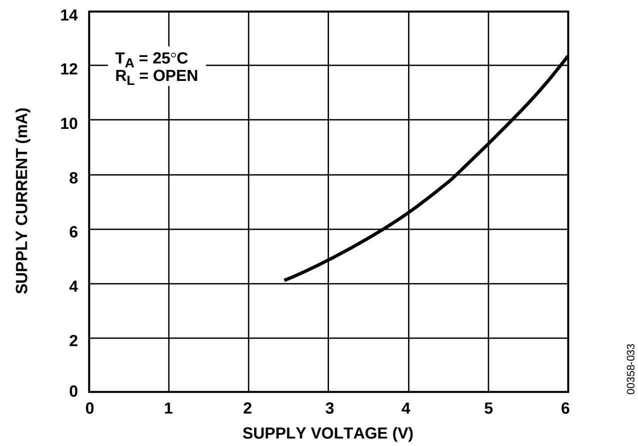


Figure 33. Supply Current vs. Supply Voltage

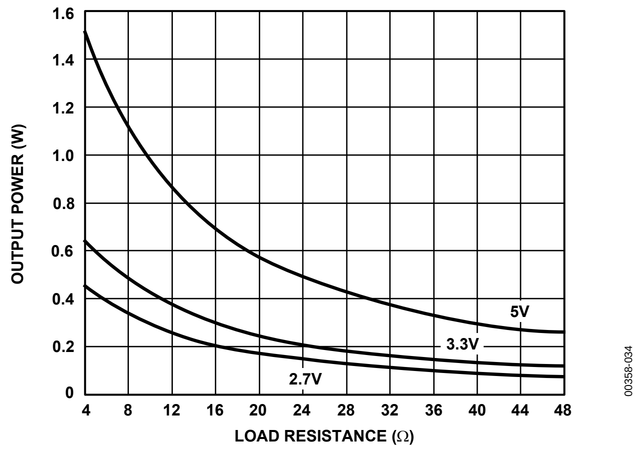


Figure 34. P_{OUTPUT} vs. Load Resistance

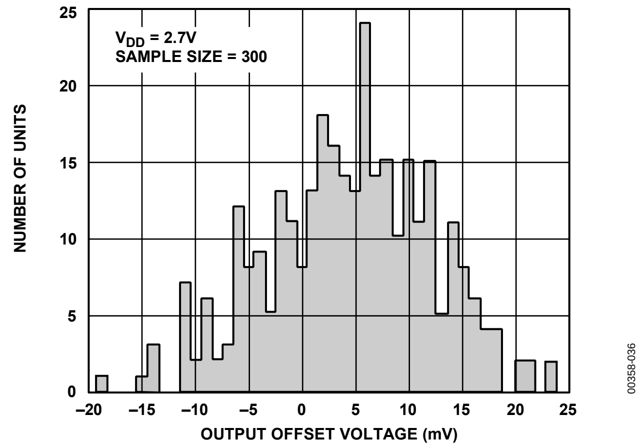


Figure 36. Output Offset Voltage Distribution

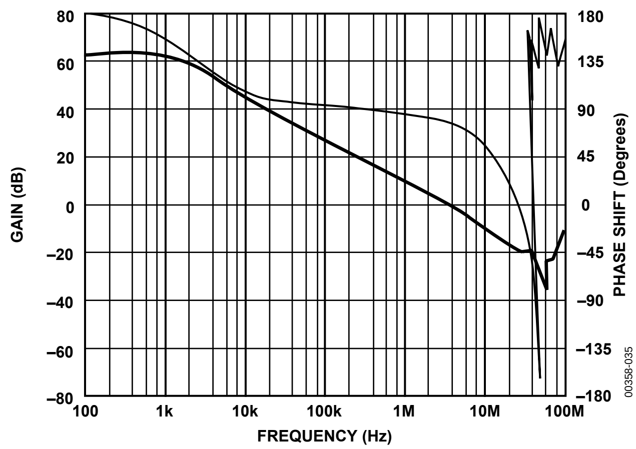


Figure 35. Gain and Phase Shift vs. Frequency (Single Amplifier)

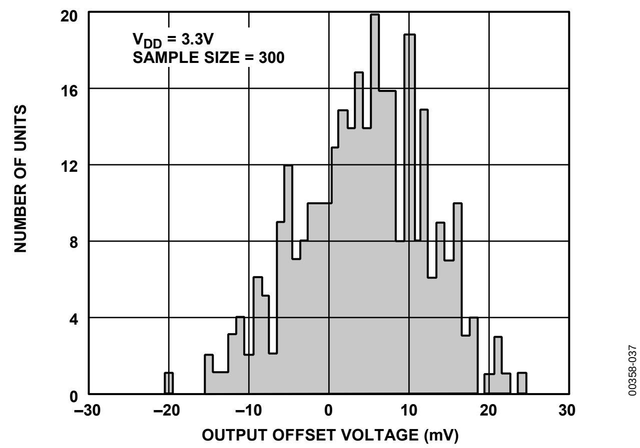


Figure 37. Output Offset Voltage Distribution

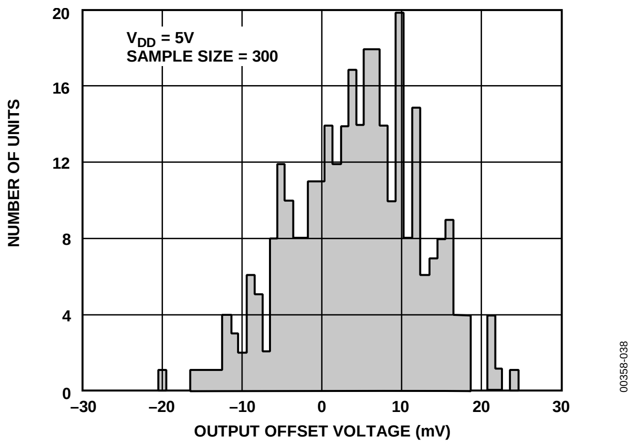


Figure 38. Output Offset Voltage Distribution

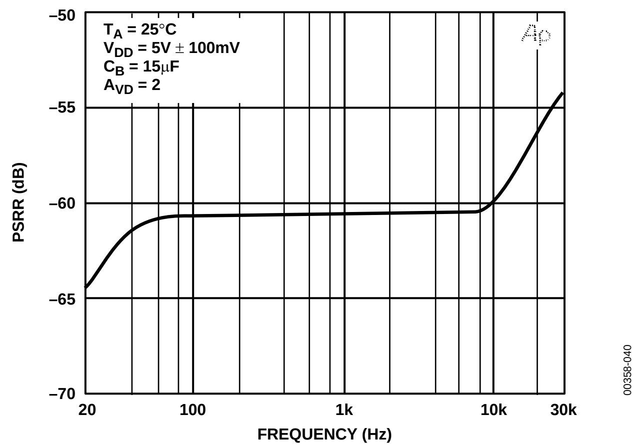


Figure 40. PSRR vs. Frequency

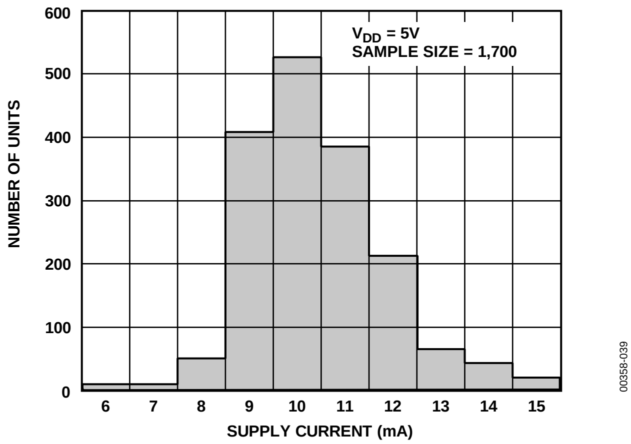


Figure 39. Supply Current Distribution

THEORY OF OPERATION

The SSM2211 is a low distortion speaker amplifier that can run from a 2.7 V to 5.5 V supply. It consists of a rail-to-rail input and a differential output that can be driven within 400 mV of either supply rail while supplying a sustained output current of 350 mA. The SSM2211 is unity-gain stable, requiring no external compensation capacitors, and can be configured for gains of up to 40 dB. Figure 41 shows the simplified schematic.

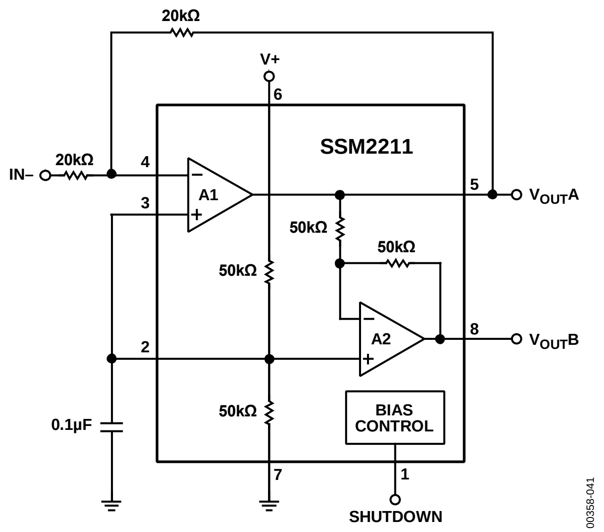


Figure 41. Simplified Schematic

Pin 4 and Pin 3 are the inverting and noninverting terminals to A1. An offset voltage is provided at Pin 2, which must be connected to Pin 3 for use in single-supply applications. The output of A1 appears at Pin 5. A second operational amplifier, A2, is configured with a fixed gain of $A_V = -1$ and produces an inverted replica of Pin 5 at Pin 8. The SSM2211 outputs at Pin 5 and Pin 8 produce a bridged configuration output to which a speaker can be connected. This bridge configuration offers the advantage of a more efficient power transfer from the input to the speaker. Because both outputs are symmetric, the dc bias at Pin 5 and Pin 8 are exactly equal, resulting in zero dc differential voltage across the outputs. This configuration eliminates the need for a coupling capacitor at the output.

THERMAL PERFORMANCE—LFCSP

The LFCSP offers the SSM2211 user even greater choices when considering thermal performance criteria. For the 8-lead, 3 mm × 3 mm LFCSP, the θ_{JA} is 50°C/W. This rating is a significant performance improvement over most other packaging options.

APPLICATIONS INFORMATION

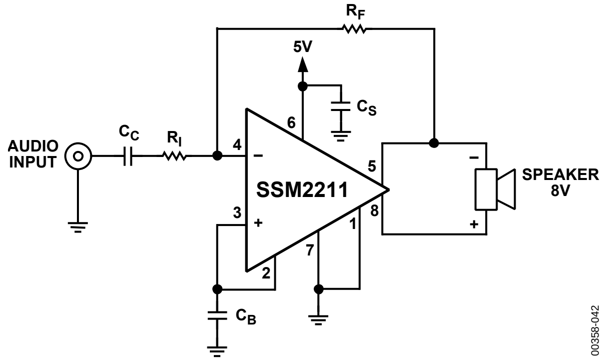


Figure 42. Typical Configuration

Figure 42 shows how the SSM2211 is connected in a typical application. The SSM2211 can be configured for gain much like a standard operational amplifier. The gain from the audio input to the speaker is

$$A_V = 2 \times \frac{R_F}{R_I} \quad (1)$$

The 2× factor results from Pin 8 having an opposite polarity of Pin 5, providing twice the voltage swing to the speaker from the bridged-output (BTL) configuration.

C_S is a supply bypass capacitor used to provide power supply filtering. Pin 2 is connected to Pin 3 to provide an offset voltage for single-supply use, with C_B providing a low ac impedance to ground to enhance power-supply rejection. Because Pin 4 is a virtual ac ground, the input impedance is equal to R_I. C_C is the input coupling capacitor, which also creates a high-pass filter with a corner frequency of

$$f_{HP} = \frac{1}{2\pi R_I \times C_C} \quad (2)$$

Because the SSM2211 has an excellent phase margin, a feedback capacitor in parallel with R_F to band limit the amplifier is not required, as it is in some competitor products.

BRIDGED OUTPUT VS. SINGLE-ENDED OUTPUT CONFIGURATIONS

The power delivered to a load with a sinusoidal signal can be expressed in terms of the peak voltage of the signal and the resistance of the load as

$$P_L = \frac{V_{PK}^2}{2 \times R_L} \quad (3)$$

By driving a load from a BTL configuration, the voltage swing across the load doubles. Therefore, an advantage in using a BTL configuration becomes apparent from Equation 3, as doubling the peak voltage results in four times the power delivered to the load. In a typical application operating from a 5 V supply, the maximum power that can be delivered by the SSM2211 to an 8 Ω speaker in a single-ended configuration is 250 mW. By driving this speaker with a bridged output, 1 W of power can be delivered. This power translates to a 12 dB increase in sound pressure level from the speaker.

Driving a speaker differentially from a BTL offers another advantage in that it eliminates the need for an output coupling capacitor to the load. In a single-supply application, the quiescent voltage at the output is half of the supply voltage. If a speaker is connected in a single-ended configuration, a coupling capacitor is needed to prevent dc current from flowing through the speaker. This capacitor also must be large enough to prevent low frequency roll-off. The corner frequency is given by

$$f_{-3dB} = \frac{1}{2\pi R_L \times C_C} \quad (4)$$

where R_L is the speaker resistance and C_C is the coupling capacitance.

For an 8 Ω speaker and a corner frequency of 20 Hz, a 1000 µF capacitor is needed, which is physically large and costly. By connecting a speaker in a BTL configuration, the quiescent differential voltage across the speaker becomes nearly zero, eliminating the need for the coupling capacitor.

SPEAKER EFFICIENCY AND LOUDNESS

The effective loudness of 1 W of power delivered into an 8 Ω speaker is a function of speaker efficiency. The efficiency is typically rated as the sound pressure level (SPL) at 1 meter in front of the speaker with 1 W of power applied to the speaker. Most speakers are between 85 dB and 95 dB SPL at 1 meter at 1 W. Table 7 shows a comparison of the relative loudness of different sounds.

Table 7. Typical Sound Pressure Levels (SPLs)

Source of Sound	SPL (dB)
Threshold of Pain	120
Heavy Street Traffic	95
Cabin of Jet Aircraft	80
Average Conversation	65
Average Home at Night	50
Quiet Recording Studio	30
Threshold of Hearing	0

Consequently, Table 7 demonstrates that 1 W of power into a speaker can produce quite a bit of acoustic energy.

POWER DISSIPATION

Another important advantage in using a BTL configuration is the fact that bridged-output amplifiers are more efficient than single-ended amplifiers in delivering power to a load. Efficiency is defined as the ratio of the power from the power supply to the power delivered to the load.

$$\eta = \frac{P_L}{P_{SY}}$$

An amplifier with a higher efficiency has less internal power dissipation, which results in a lower die-to-case junction temperature compared with an amplifier that is less efficient. Efficiency is important when considering the amplifier maximum power dissipation rating vs. ambient temperature. An internal power dissipation vs. output power equation can be derived to fully understand efficiency of amplifier.

The internal power dissipation of the amplifier is the internal voltage drop multiplied by the average value of the supply current. An easier way to find internal power dissipation is to measure the difference between the power delivered by the supply voltage source and the power delivered into the load. The waveform of the supply current for a bridged-output amplifier is shown in Figure 43.

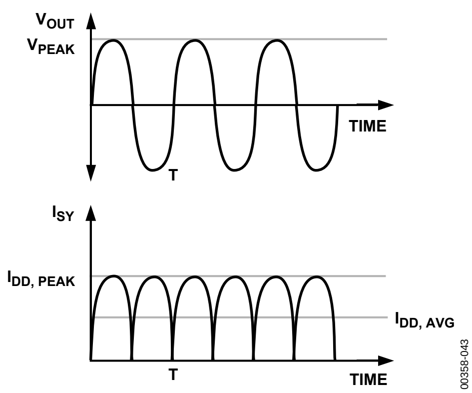


Figure 43. Bridged Amplifier Output Voltage and Supply Current vs. Time

By integrating the supply current over a period, T, and then dividing the result by T, the $I_{DD,AVG}$ can be found. Expressed in terms of peak output voltage and load resistance

$$I_{DD,AVG} = \frac{2V_{PEAK}}{\pi R_L} \quad (5)$$

Therefore, power delivered by the supply, neglecting the bias current for the device, is

$$P_{SY} = \frac{2\,V_{DD} \times V_{PEAK}}{\pi R_L} \quad (6)$$

The power dissipated internally by the amplifier is simply the difference between Equation 6 and Equation 3. The equation for internal power dissipated, P_{DISS}, expressed in terms of power delivered to the load and load resistance, is

$$P_{DISS} = \frac{2\sqrt{2}\,V_{DD}}{\pi\sqrt{R_L}} \times \sqrt{P_L} - P_L \quad (7)$$

The graph of this equation is shown in Figure 44.

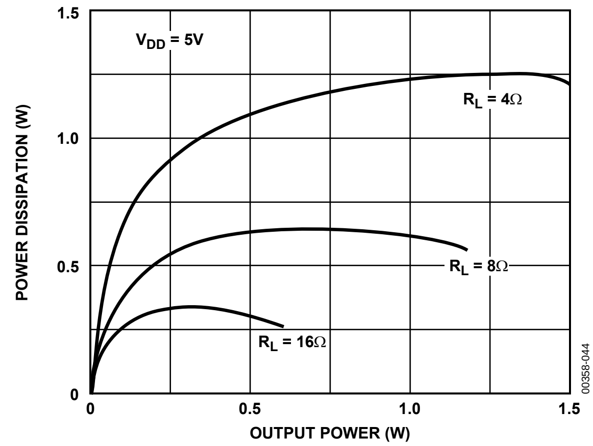


Figure 44. Power Dissipation vs. Output Power with V_{DD} = 5 V

Because the efficiency of a bridged-output amplifier (Equation 3 divided by Equation 6) increases with the square root of P_L, the power dissipated internally by the device stays relatively flat and actually decreases with higher output power. The maximum power dissipation of the device can be found by differentiating Equation 7 with respect to load power and setting the derivative equal to zero, which yields

$$\frac{\partial P_{DISS}}{\partial P_L} = \frac{\sqrt{2}\,V_{DD}}{\pi\sqrt{R_L}} \times \frac{1}{\sqrt{P_L}} - 1 = 0 \quad (8)$$

and occurs when

$$P_{DISS,MAX} = \frac{2\,V_{DD}^2}{\pi^2 R_L} \quad (9)$$

Using Equation 9 and the power derating curve in Figure 31, the maximum ambient temperature can be found easily. This ensures that the SSM2211 does not exceed its maximum junction temperature of 150°C. The power dissipation for a single-ended output application where the load is capacitively coupled is given by

$$P_{DISS} = \frac{2\sqrt{2}\,V_{DD}}{\pi\sqrt{R_L}} \times \sqrt{P_L} - P_L \quad (10)$$

The graph of Equation 10 is shown in Figure 45.

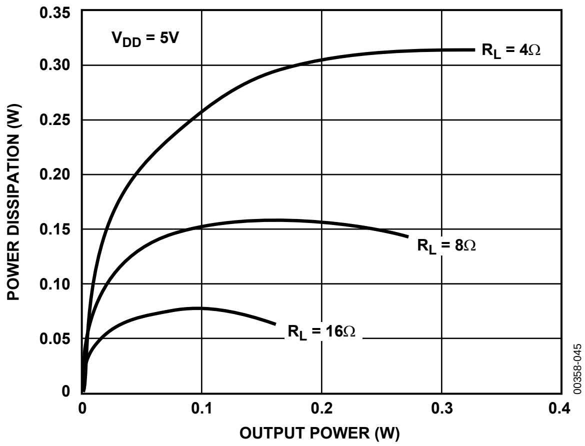


Figure 45. Power Dissipation vs. Single-Ended Output Power with V_{DD} = 5 V

The maximum power dissipation for a single-ended output is

$$P_{DISS,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \qquad (11)$$

OUTPUT VOLTAGE HEADROOM

The outputs of both amplifiers in the SSM2211 can come within 400 mV of either supply rail while driving an 8 Ω load. As compared with equivalent competitor products, the SSM2211 has a higher output voltage headroom. This means that the SSM2211 can deliver an equivalent maximum output power while running from a lower supply voltage. By running at a lower supply voltage, the internal power dissipation of the device is reduced, as shown in Equation 9. This extended output headroom, along with the LFCSP, allows the SSM2211 to operate in higher ambient temperatures than competitor devices.

The SSM2211 is also capable of providing amplification even at supply voltages as low as 2.7 V. The maximum power available at the output is a function of the supply voltage. Therefore, as the supply voltage decreases, so does the maximum power output from the device. The maximum output power vs. supply voltage at various BTL resistances is shown in Figure 46. The maximum output power is defined as the point at which the output has 1% total harmonic distortion (THD + N).

To find the minimum supply voltage needed to achieve a specified maximum undistorted output power use Figure 46.

For example, an application requires only 500 mW to be output for an 8 Ω speaker. With the speaker connected in a bridged-output configuration, the minimum supply voltage required is 3.3 V.

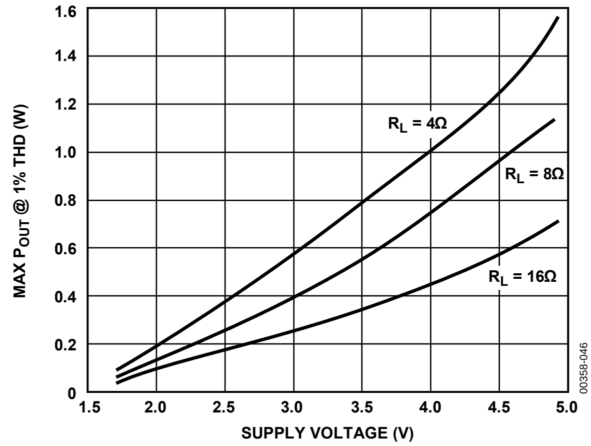


Figure 46. Maximum Output Power vs. V_{SY}

Shutdown Feature

The SSM2211 can be put into a low power consumption shutdown mode by connecting Pin 1 to 5 V. In shutdown mode, the SSM2211 has an extremely low supply current of less than 10 nA, which makes the SSM2211 ideal for battery-powered applications.

Connect Pin 1 to ground for normal operation. Connecting Pin 1 to V_{DD} mutes the outputs and puts the device into shutdown mode. A pull-up or pull-down resistor is not required. Pin 1 must always be connected to a fixed potential, either V_{DD} or ground, and never be left floating. Leaving Pin 1 unconnected can produce unpredictable results.

AUTOMATIC SHUTDOWN-SENSING CIRCUIT

Figure 47 shows a circuit that can be used to take the SSM2211 in and out of shutdown mode automatically. This circuit can be set to turn the SSM2211 on when an input signal of a certain amplitude is detected. The circuit also puts the device into low power shutdown mode if an input signal is not sensed within a certain amount of time. Shutdown mode can be useful in a variety of portable radio applications, where power conservation is critical.

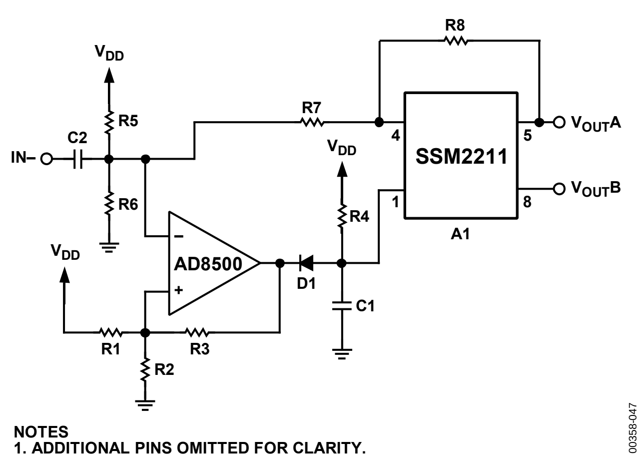


Figure 47. Automatic Shutdown Circuit

The input signal to the SSM2211 is also connected to the non-inverting terminal of A2. R1, R2, and R3 set the threshold voltage at which the SSM2211 is to be taken out of shutdown mode. The diode, D1, half-wave rectifies the output of A2, discharging C1 to ground when an input signal greater than the set threshold voltage is detected. R4 controls the charge time of C1, which sets the time until the SSM2211 is put back into shutdown mode after the input signal is no longer detected.

R5 and R6 establish a voltage reference point equal to half of the supply voltage. R7 and R8 set the gain of the SSM2211. A 1N914 or equivalent diode is required for D1, and A2 must be a rail-to-rail output amplifier, such as the AD8500 or equivalent. This ensures that C1 discharges sufficiently to bring the SSM2211 out of shutdown mode.

To find the appropriate component values, the gain of A2 must be determined by

$$A_{V,MIN} = \frac{V_{SY}}{V_{THS}} \tag{12}$$

where:
V_{SY} is the single supply voltage.
V_{THS} is the threshold voltage.
A_V must be set to a minimum of 2 for the circuit to work properly.

Next, choose R1 and set R2 to

$$R2 = R1\left(1 - \frac{2}{A_V}\right) \tag{13}$$

Find R3 as

$$R3 = \frac{R1 \times R2}{R2 + R2}\left(A_V - 1\right) \tag{14}$$

C1 can be arbitrarily set but must be small enough to prevent A2 from becoming capacitively overloaded. R4 and C1 control the shutdown rate. To prevent intermittent shutdown with low frequency input signals, the minimum time constant must be

$$R4 \times C1 \geq \frac{10}{f_{LOW}} \tag{15}$$

where f_{LOW} is the lowest input frequency expected.

SHUTDOWN-CIRCUIT DESIGN EXAMPLE

In this example, a portable radio application requires the SSM2211 to be turned on when an input signal greater than 50 mV is detected. The device must return to shutdown mode within 500 ms after the input signal is no longer detected. The lowest frequency of interest is 200 Hz, and a 5 V supply is used.

The minimum gain of the shutdown circuit, from Equation 12, is $A_V = 100$. R1 is set to 100 kΩ. Using Equation 13 and Equation 14, R2 = 98 kΩ and R3 = 4.9 MΩ. C1 is set to 0.01 μF, and based on Equation 15, R4 is set to 10 MΩ. To minimize power supply current, R5 and R6 are set to 10 MΩ. The previous procedure provides an adequate starting point for the shutdown circuit. Some component values may need to be adjusted empirically to optimize performance.

START-UP POPPING NOISE

During power-up or release from shutdown mode, the midrail bypass capacitor, C_B, determines the rate at which the SSM2211 starts up. By adjusting the charging time constant of C_B, the start-up pop noise can be pushed into the subaudible range, greatly reducing start-up popping noise. On power-up, the midrail bypass capacitor is charged through an effective resistance of 25 kΩ. To minimize start-up popping, the charging time constant for C_B must be greater than the charging time constant for the input coupling capacitor, C_C.

$$C_B \times 25\ \text{k}\Omega > C_C \times R1 \tag{16}$$

For an application where R1 = 10 kΩ and C_C = 0.22 μF, C_B must be at least 0.1 μF to minimize start-up popping noise.

SSM2211 Amplifier Design Example

Maximum output power: 1 W
Input impedance: 20 kΩ
Load impedance: 8 Ω
Input level: 1 V rms
Bandwidth: 20 Hz – 20 kHz ± 0.25 dB

The configuration shown in Figure 42 is used. The first thing to determine is the minimum supply rail necessary to obtain the specified maximum output power. From Figure 46, for 1 W of output power into an 8 Ω load, the supply voltage must be at least 4.6 V. A supply rail of 5 V can be easily obtained from a voltage reference. The extra supply voltage also allows the SSM2211 to reproduce peaks in excess of 1 W without clipping the signal. With V_{DD} = 5 V and R_L = 8 Ω, Equation 9 shows that the maximum power dissipation for the SSM2211 is 633 mW. From the power derating curve in Figure 31, the ambient temperature must be less than 50°C for the SOIC and 121°C for the LFCSP.

The required gain of the amplifier can be determined from Equation 17 as

$$A_V = \frac{\sqrt{P_L \times R_L}}{V_{IN,\ rms}} = 2.8 \tag{17}$$

From Equation 1,

$$\frac{R_F}{R_I} = \frac{A_V}{2}$$

or $R_F = 1.4 \times R_I$. Because the desired input impedance is 20 kΩ, R_I = 20 kΩ and R2 = 28 kΩ.

The final design step is to select the input capacitor. When adding an input capacitor, C_C, to create a high-pass filter, the corner frequency must be far enough away for the design to meet the bandwidth criteria. For a first-order filter to achieve a pass-band response within 0.25 dB, the corner frequency must be at least 4.14× away from the pass-band frequency. Therefore, $(4.14 \times f_{HP}) < 20$ Hz. Using Equation 2, the minimum size of an input capacitor can be found.

$$C_C > \frac{1}{2\pi \times 20\,\text{k}\Omega \left(\frac{20\ \text{Hz}}{4.14}\right)} \quad (18)$$

Therefore, $C_C > 1.65$ µF. Using a 2.2 µF is a practical choice for C_C.

The gain bandwidth product for each internal amplifier in the SSM2211 is 4 MHz. Because 4 MHz is much greater than 4.14 × 20 kHz, the design meets the upper frequency bandwidth criteria. The SSM2211 can also be configured for higher differential gains without running into bandwidth limitations. Equation 16 shows an appropriate value for C_B to reduce start-up popping noise.

$$C_B > \frac{(2.2\ \mu\text{F})(20\ \text{k}\Omega)}{25\ \text{k}\Omega} = 1.76\ \mu\text{F} \quad (19)$$

Selecting C_B to be 2.2 µF for a practical value of capacitor minimizes start-up popping noise.

To summarize the final design,

- $V_{DD} = 5$ V
- R1 = 20 kΩ
- $R_F = 28$ kΩ
- $C_C = 2.2$ µF
- $C_B = 2.2$ µF
- $T_{A,\ MAX} = 85$°C

SINGLE-ENDED APPLICATIONS

There are applications in which driving a speaker differentially is not practical, for example, a pair of stereo speakers where the negative terminal of both speakers is connected to ground. Figure 48 shows how this application can be accomplished.

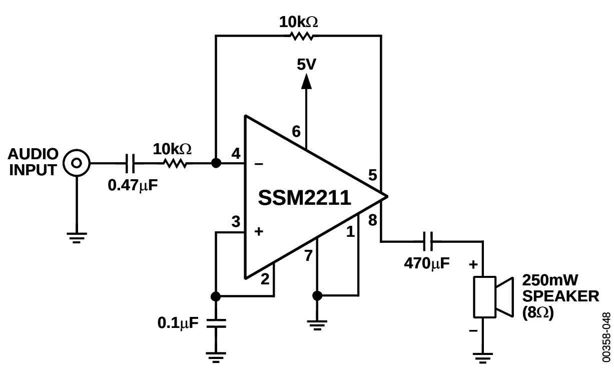


Figure 48. Single-Ended Output Application

It is not necessary to connect a dummy load to the unused output to help stabilize the output. The 470 µF coupling capacitor creates a high-pass frequency cutoff of 42 Hz, as given in Equation 4, which is acceptable for most computer speaker applications. The overall gain for a single-ended output configuration is $A_V = R_F/R_1$, which for this example is equal to 1.

DRIVING TWO SPEAKERS SINGLE-ENDEDLY

It is possible to drive two speakers single-endedly with both outputs of the SSM2211.

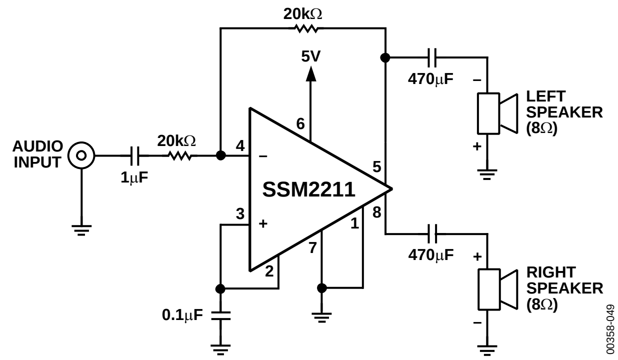


Figure 49. SSM2211 Used as a Dual-Speaker Amplifier

Each speaker is driven by a single-ended output. The trade-off is that only 250 mW of sustained power can be put into each speaker. In addition, a coupling capacitor must be connected in series with each of the speakers to prevent large dc currents from flowing through the 8 Ω speakers. These coupling capacitors produce a high-pass filter with a corner frequency given by Equation 4. For a speaker load of 8 Ω and a coupling capacitor of 470 µF, this results in a −3 dB frequency of 42 Hz.

Because the power of a single-ended output is one-quarter that of a BTL, both speakers together are still half as loud (−6 dB SPL) as a single speaker driven with a BTL.

The polarity of the speakers is important because each output is 180° out of phase with the other. By connecting the negative terminal of Speaker 1 to Pin 5 and the positive terminal of Speaker 2 to Pin 8, proper speaker phase can be established.

The maximum power dissipation of the device, assuming both loads are equal, can be found by doubling Equation 11. If the loads are different, use Equation 11 to find the power dissipation caused by each load, and then take the sum to find the total power dissipated by the SSM2211.

LFCSP PCB CONSIDERATIONS

The LFCSP is a plastic encapsulated package with a copper lead frame substrate. The LFCSP is a leadless package with solder lands on the bottom surface of the package, instead of conventional formed perimeter leads. A key feature that allows the user to reach the quoted θ_{JA} performance is the exposed die attach paddle (DAP) on the bottom surface of the package. When soldered to the PCB, the DAP can provide efficient conduction of heat from the die to the PCB. To achieve optimum package performance, consideration must be given to the PCB pad design for both the solder lands and the DAP. For further information, see the AN-772 Application Note.

OUTLINE DIMENSIONS

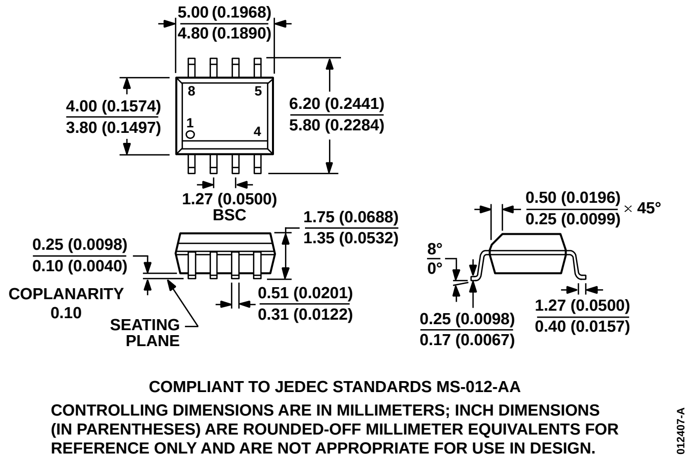


Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body, S-Suffix
(R-8)
Dimensions shown in millimeters and (inches)

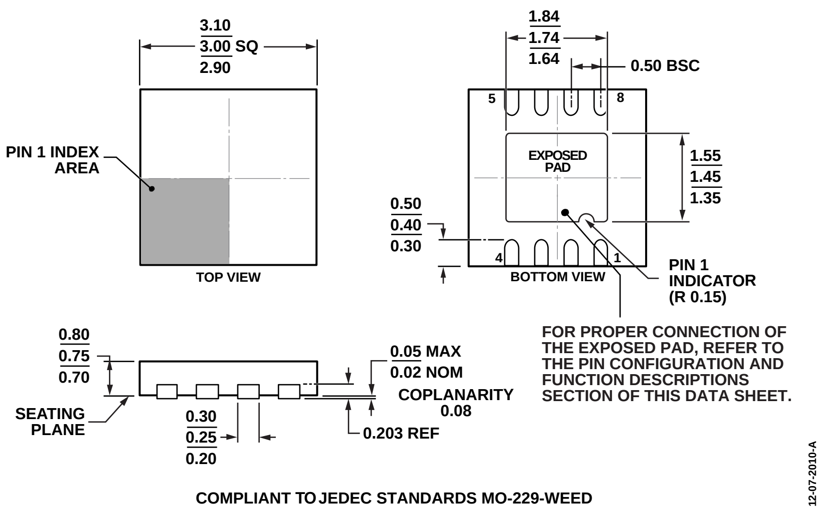


Figure 51. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
SSM2211CPZ-REEL	−40°C to +85°C	8-Lead LFCSP	CP-8-13	B5A#
SSM2211CPZ-REEL7	−40°C to +85°C	8-Lead LFCSP	CP-8-13	B5A#
SSM2211SZ	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)	
SSM2211SZ-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)	
SSM2211SZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)	

[1] Z = RoHS Compliant Part; # denotes RoHS compliant product may be top or bottom marked.

NOTES

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