# 1 Overview

## 1.1 Device comparison

**Table 1. MPC5645S device comparison**

| Feature | MPC5645S | | |
|---|---|---|---|
| Package | 176 LQFP | 208 LQFP | 416 TEPBGA |
| CPU | e200z4d<br>4 KB Instruction-Cache<br>16-entry Memory Management Unit (MMU)<br>Floating Point Unit (FPU)<br>Signal Processing Extension (SPE) | | |
| Execution speed | Static–125 MHz | | |
| Flash memory (ECC) | 2 MB | | |
| RAM (ECC) | 64 KB | | |
| On-chip graphics RAM (no ECC) | 1 MB | | |
| MPU | 16 entry | | |
| eDMA | 16 channels | | |
| DRAM controller | No | | Yes |
| OpenVG Graphics Accelerator (GFX2D) | Yes (OpenVG 1.1) | | |
| Display Control Unit (DCU3) | Yes | | |
| Display Control Unit Lite (DCULite) | No | Yes | |
| Timing Controller (TCON) and RSDS interface | No | Yes | |
| Video Input Unit (VIU2) | Yes | | |
| QuadSPI serial flash interface | Yes | | |
| Stepper Motor Controller (SMC) | 4 motors | 6 motors | |
| Stepper Stall Detect (SSD) | Yes | | |
| Sound Generator Module (SGM) | Yes | | |
| 32 kHz external crystal oscillator | Yes | | |
| Real Time Counter and Autonomous Periodic Interrupt (RTC/API) | Yes | | |
| Periodic interrupt timer (PIT) | 8 ch, 32-bit | | |
| Software Watchdog Timer (SWT) | Yes | | |
| System Timer Module (STM) | 4 ch, 32-bit | | |
| Timed I/O[1] | 20 ch, 16-bit: IC / OC / OPWM<br>8 ch, 16-bit: IC / OC<br>4 ch, 16-bit: IC / OC / OPWM / QDEC | | |
| Analog-to-Digital Converter (ADC)[2] | 16 channels, 10-bit | 20 channels, 10-bit | |

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NXP Semiconductors

**Table 1. MPC5645S device comparison (continued)**

| Feature | MPC5645S | | |
|---|---|---|---|
| Package | 176 LQFP | 208 LQFP | 416 TEPBGA |
| CAN (64 mailboxes) | 3 × FlexCAN | | |
| CAN sampler | Yes | | |
| Serial communication interface | 3 × LINFlex | 4 × LINFlex | |
| SPI | 2 × DSPI | 3 × DSPI | |
| I$^2$C | 4 | | |
| GPIO | 128 | 150 | 177[3] |
| Debug | Nexus Class 3 (4×MDO)[4] | | Nexus Class 3 (12×MDO) |

[1]  IC-Input Capture, OC-Output Compare, OPWM-Output Pulse Width Modulation, QDEC- Quadrature Decode Mode

[2]  Support for external multiplexer enabling up to 8 channels

[3]  The 416-pin GPIO count does not include the DRAM interface, which is dedicated to DRAM only.

[4]  Nexus pins are multiplexed with other functional pins on 176 LQFP and 208 LQFP package options.
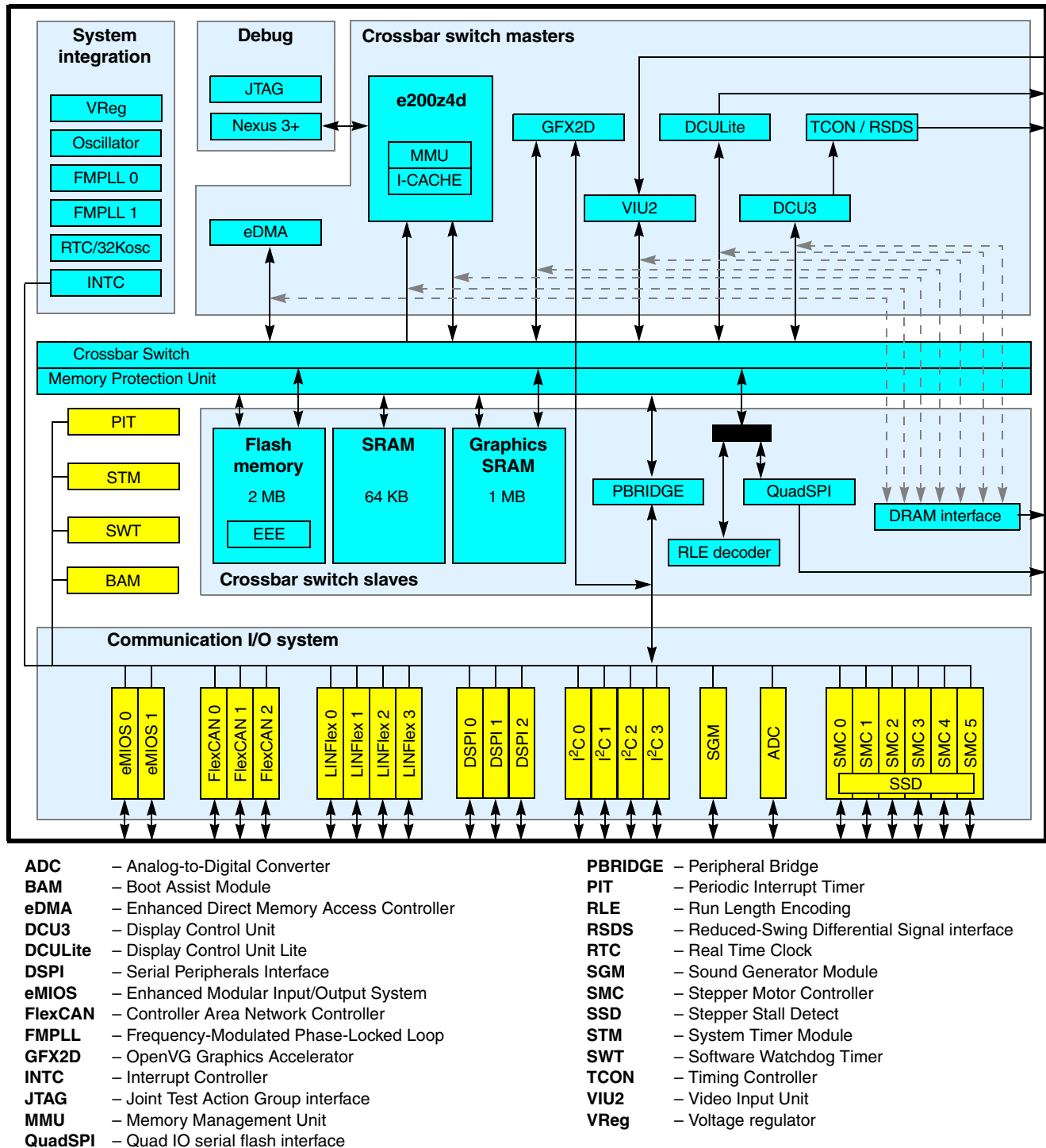
# 1.2     Block diagram



| | |
|---|---|
| **ADC** – Analog-to-Digital Converter | **PBRIDGE** – Peripheral Bridge |
| **BAM** – Boot Assist Module | **PIT** – Periodic Interrupt Timer |
| **eDMA** – Enhanced Direct Memory Access Controller | **RLE** – Run Length Encoding |
| **DCU3** – Display Control Unit | **RSDS** – Reduced-Swing Differential Signal interface |
| **DCULite** – Display Control Unit Lite | **RTC** – Real Time Clock |
| **DSPI** – Serial Peripherals Interface | **SGM** – Sound Generator Module |
| **eMIOS** – Enhanced Modular Input/Output System | **SMC** – Stepper Motor Controller |
| **FlexCAN** – Controller Area Network Controller | **SSD** – Stepper Stall Detect |
| **FMPLL** – Frequency-Modulated Phase-Locked Loop | **STM** – System Timer Module |
| **GFX2D** – OpenVG Graphics Accelerator | **SWT** – Software Watchdog Timer |
| **INTC** – Interrupt Controller | **TCON** – Timing Controller |
| **JTAG** – Joint Test Action Group interface | **VIU2** – Video Input Unit |
| **MMU** – Memory Management Unit | **VReg** – Voltage regulator |
| **QuadSPI** – Quad IO serial flash interface | |

**Figure 1. MPC5645S block diagram**

## 1.3    Feature list

- Dual-issue, 32-bit Power Architecture Book E compliant CPU core complex (e200z4d)
  — Memory Management Unit (MMU)
  — 4 KB, 2/4-way instruction cache
- 2 MB on-chip ECC flash memory with:
  — Flash memory controller
  — Prefetch buffers
- 64 KB on-chip ECC SRAM
- 1 MB on-chip non-ECC graphics SRAM with two-port graphics SRAM controller
- Memory Protection Unit (MPU) with up to 16 region descriptors and 32-byte region granularity to provide basic memory access permission and ensure separation between different codes and data
- Interrupt Controller (INTC) with 163 peripheral interrupt sources and eight software interrupts
- Two Frequency-Modulated Phase-Locked Loops (FMPLLs)
  — Primary FMPLL (FMPLL0) provides a system clock up to 125 MHz
  — Auxiliary FMPLL (FMPLL1) is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules, QuadSPI and as alternate clock to the DCU and DCU-Lite for pixel clock generation
- Crossbar switch architecture enables concurrent access of peripherals, flash memory or RAM from multiple bus masters
- 16-channel Enhanced Direct Memory Access controller (eDMA) with multiple transfer request sources using a DMA channel multiplexer
- Boot Assist Module (BAM) with 8 KB dedicated ROM for embedded boot code supports boot options including download of boot code via a serial link (CAN or SCI)
- Two Display Control Units (DCU3 and DCULite) for direct drive of up to two TFT LCD displays up to XGA resolution
- Timing Controller (TCON) and RSDS interface for the DCU3 module
- 2D OpenVG 1.1 and raster graphics accelerator (GFX2D)
- Video Input Unit (VIU2) supporting 8/10-bit ITU656 video input, YUV to RGB conversion, video down-scaling, de-interlacing, contrast adjustment and brightness adjustment.
- DRAM controller supporting DDR1, DDR2, and LPDDR1 DRAMs
- Stepper Motor Controller (SMC)
  — High-current drivers for up to six instrument cluster gauges driven in full dual H-bridge configuration
  — Stepper motor return-to-zero and stall detection module
  — Stepper motor short circuit detection
- Sound Generator Module (SGM)
  — 4-channel mixer
  — Supports PCM wave playback and synthesized tones
  — Optional PWM or I$^2$S outputs
- Two 16-channel Enhanced Modular Input Output System (eMIOS) modules
  — Support a range of 16-bit Input Capture, Output Compare, Pulse Width Modulation and Quadrature Decode functions
- 10-bit Analog-to-Digital Converter (ADC) with a maximum conversion time of 1 µs
  — Up to 20 internal channels
  — Up to 8 external channels
- Three Deserial Serial Peripheral Interface (DSPI) modules for full-duplex, synchronous, communications with external devices
- QuadSPI serial flash memory controller

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- — Supports single, dual and quad IO serial flash memory
- — Interfaces to external, memory-mapped serial flash memories
- — Supports simultaneous addressing of 2 external serial flashes to achieve up 80 MB/s read bandwidth
- RLE decoder supporting memory to memory decoding of RLE data in conjunction with eDMA
- Four local interconnect network (LINFlex) controller modules
  - — Capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support
  - — Compliant with LIN protocol rev 2.1
- Three controller-area network (FlexCAN) modules
  - — Compliant with the CAN protocol version 2.0 C
  - — 64 configurable buffers
  - — Programmable bit rate of up to 1 Mb/s
- Four Inter-Integrated Circuit ($I^2C$) internal bus controllers with master/slave bus interface
- Low-power loop controlled pierce crystal oscillator supporting 4–16MHz external crystal or resonator
- Real Time Counter (RTC) with clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wake-up with 1 ms resolution with maximum timeout of 2 seconds
  - — Support for real time counter (RTC) with clock source from external 32 KHz crystal oscillator, supporting wake-up with 1 s resolution and maximum timeout of one hour
  - — RTC optionally clocked by fast 4–16 MHz external oscillator
- System timers:
  - — Four-channel 32-bit System Timer Module (STM)
  - — Eight-channel 32-bit Periodic Interrupt Timer (PIT) module (including ADC trigger)
  - — Software Watchdog Timer (SWT)
- System Integration Unit Lite (SIUL) module to manage external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM)
  - — Provides information for identification of the device, last boot mode, or debug status
  - — Provides an entry point for the censorship password mechanism
- Clock Generation Module (MC_CGM) to generate system clock sources and provide a unified register interface, enabling access to all clock sources
- Clock Monitor Unit (CMU)
  - — Monitors the integrity of the fast (4–16 MHz) external crystal oscillator and the primary FMPLL (FMPLL0)
  - — Acts as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- Mode Entry Module (MC_ME)
  - — Controls the device power mode, i.e., RUN, HALT, STOP, or STANDBY
  - — Controls mode transition sequences
  - — Manages the power control, voltage regulator, clock generation and clock management modules
- Power Control Unit (MC_PCU) to implement standby mode entry/exit and control connections to power domains
- Reset Generation Module (MC_RGM) to manage reset assertion and release to the device at initial power-up
- Nexus Development Interface (NDI) per IEEE-ISTO 5001-2008 Class 3 standard with additional Class 4 features:
  - — Watchpoint Triggering
  - — Processor Overrun Control
- Device/board boundary-scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating the 3.3–5 V supply voltage down to 1.2 V for core logic (requires external ballast transistor)
- Package:[1]
  - — 176 LQFP, 0.5 mm pitch, 24 mm × 24 mm outline

— 208 LQFP, 0.5 mm pitch, 28 mm × 28 mm outline

— 416 TEPBGA, 1mm ball pitch, 27 mm × 27 mm outline

## 1.4 Feature details

### 1.4.1 Low-power operation

The MPC5645S is designed for optimized low-power operation and dynamic power management of the CPU and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are three low-power modes:

- STANDBY
- STOP
- HALT

and five dynamic power modes — RUN[0..3] and DRUN. All low-power modes use clock gating to halt the clock for all or part of the device.

STANDBY mode turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be awakened from STANDBY mode via from any of up to 23 I/O pins, a reset or from a periodic wake-up using a low power oscillator. If required, it is possible to enable the internal 16 MHz oscillator, the external 4–16 MHz oscillator, and the external 32 KHz oscillator.

In STANDBY mode the contents of the CPU, on-chip peripheral registers, and potentially some of the volatile memory are lost. The two possible configurations in STANDBY mode are:

- The device retains 64 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.
- The device retains 8 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest-power STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the CPU and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

RUN modes are the main operating modes where the entire device can be powered and clocked and from which most processing activity is done. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed, and system clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the CPU system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

The following table summarizes the operating modes of the MPC5645S.

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1. See the device comparison table for package offerings for each device in the family.

## Table 2. Operating mode summary

| Operating mode | SoC features | | | | | | Clock sources | | | | | | Periodic Wake-up | Wake-up input | VREG mode | Wake-up time[1] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CPU | GFX accelerator DRAM controller Peripherals | Flash | SRAM | Graphics RAM | Primary PLL | Auxiliary PLL | 16MHz IRC | 4-16MHz OSC | 128KHz IRC | 32KHz X OSC | | | | VREG start-up | IRC Wake-up | Flash Recovery | OSC Stabilization | PLL Lock | S/W Reconfig | Mode switch over |
| RUN | On | OP | OP | OP[2] | On | OP | OP | On | OP | On | OP | — | — | FP | — | — | — | — | — | — | — |
| HALT | CG | OP | OP | OP[2] | On | OP | OP | On | OP | On | OP | OP | OP | FP | — | — | — | — | — | — | 30 µs [3] |
| STOP | CG | CG | CG | OP[2] | CG | CG | CG | OP | OP | On | OP | OP | OP | LP | 350 µs | 4 µs | 20 µs | 1 ms | 200 µs | — | 30 µs [3] |
| STANDBY | Off | Off | Off | 64K[4] | Off | Off | Off | OP | OP | On | OP | OP | OP | LP | 350 µs | 8 µs | 100 µs | 1 ms | 200 µs | Var | 28 µs |
| | Off | Off | Off | 8K[5] | Off | Off | Off | OP | OP | On | OP | OP | OP | LP | 200 µs | 8 µs | 100 µs | 1 ms | 200 µs | Var | 28 µs |
| POR | | | | | | | | | | | | | | | 500 µs | 8 µs | 100 µs | 1 ms | 200 µs | | BAM[6] |

Table key:
- On — Powered and clocked
- OP — Optionally configurable to be enabled or disabled (clock gated)
- CG — Clock Gated, Powered but clock stopped
- Off — Powered off and clock gated
- FP — VREG Full Performance mode
- LP — VREG Low Power mode, reduced output capability of VREG but lower power consumption
- Var — Variable duration, based on the required reconfiguration and execution clock speed
- BAM — Boot Assist Module Software and Hardware used for device start-up and configuration

[1]   A high level summary of some key durations that need to be considered when recovering from low power modes. This does not account for all durations at wake up. Other delays will be necessary to consider including, but not limited to the external supply start-up time.
IRC Wake-up time must not be added to the overall wake-up time as it starts in parallel with the VREG.
All other wake-up times must be added to determine the total start-up time.

[2]   Either 64 KB or 8 KB available.

[3]   Flash configured in disabled mode.

[4]   64 KB of the RAM contents is retained, but not accessible in STANDBY mode.

[5]   8 KB of the RAM contents is retained, but not accessible in STANDBY mode.

[6]   Dependent on boot option after reset.

Additional notes on low power operation:

- Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low power modes
- The 16 MHz internal RC oscillator supports low speed code execution and clocking of peripherals when it is selected as the system clock and can also be used as the PLL input clock source to provide fast start-up without the external oscillator delay
- The device includes an internal voltage regulator that includes the following features:
  - Regulates input to generate all internal supplies
  - Manages power gating
  - External ballast transistor for high power regulator

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— Low-Power and Ultra-Low-Power regulators support operation when in STOP and STANDBY modes, respectively, to minimize power consumption
— Startup on-chip regulators in <350μs for rapid exit of STOP and STANDBY modes
— Low voltage detection on main supply and 1.2 V regulated supplies

## 1.4.2    e200z4d core

The e200z4d Power Architecture® core provides the following features:

- Dual issue, 32-bit *Power Architecture Book E* compliant CPU
- Implements the VLE APU for reduced code footprint
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  — Dedicated branch address calculation adder
  — Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and Flash memory via independent Instruction and Data BIUs.
- Load/store unit
  — 2 cycle load latency
  — Fully pipelined
  — Big and Little endian support
  — Misaligned access support
- 64-bit General Purpose Register file
- Dual AHB 2.v6 64-bit System buses
- Memory Management Unit (MMU) with 16-entry fully-associative TLB and multiple page size support
- 4 KB, 2/4-Way Set Associative Instruction Cache
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Nexus Class 3 real-time Development Unit
- Dynamic power management of execution units, cache and MMU

## 1.4.3    Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between seven master ports and eight slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows concurrent transactions to occur from any master port to any slave port but one of those transfers must be an instruction fetch from internal flash. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters having equal priority are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- Seven master ports:
  — e200z4d core instruction port
  — e200z4d core complex load/store data port

- — eDMA controller
- — DCU
- — DCULite
- — VIU
- — 2D Graphics Accelerator (GFX2D)
- Seven slave ports:
  - — Platform Flash Controller (2 Ports)
  - — Platform SRAM Controller
  - — Graphics SRAM Controller (2 Ports)
  - — QuadSPI serial flash Controller and RLE Decoder
  - — Peripheral Bridge
- 32-bit internal address bus, 64-bit internal data bus
- Programmable Arbitration Priority
  - — Requesting masters can be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access, or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

## 1.4.4 Enhanced Direct Memory Access (eDMA)

The eDMA module is a controller capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- 16 channels support independent 8-, 16-, or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, periodic timer interrupt or eDMA channel request
- Each DMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, QuadSPI, RLE Decoder, DSPIs, $I^2C$, ADC, eMIOS, and General Purpose I/Os (GPIOs)
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with up to a total of 64 potential request sources

## 1.4.5 Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
  — Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources
- External non maskable interrupt directly accessing the main CPU critical interrupt mechanism
- 32 external interrupts

## 1.4.6 QuadSPI serial flash memory controller

The QuadSPI module enables use of external serial flash memories supporting single, dual, and quad modes of operation. It features the following:

- Maximum serial clock frequency 80 MHz
- Memory mapped read access for AHB crossbar switch masters
- Automatic serial flash read command generation by CPU, eDMA, DCU, or DCULite read access on AHB bus
- Supports single, dual, and quad serial flash read commands
- Simultaneous mode:
  — Supports concurrent read of two external serial flashes
  — The quad data streams from the two flashes can be recombined in the QuadSPI to achieve up to 80 MB/s read bandwidth with 80 MHz serial flash
- 16×64-bit buffer with speculative fetch and buffer flush mechanisms to maximize read bandwidth of serial flash
- DMA support
- All Serial Flash program, erase, read, and configuration commands available via IP bus interface

## 1.4.7 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.

The GPIO features the following:

- Up to four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs
- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to up to 24 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset

## 1.4.8    On-chip flash memory with ECC

The MPC5645S microcontroller has the following flash memory features:

- 2 MB of flash memory
  — Typical flash memory access time: 0 wait-state for buffer hits, 3 wait-states for page buffer miss at 125 MHz
  — Two 4×128-bit page buffers with programmable prefetch control
    – One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
    – One set of page buffers allocated to Display Controller Units, Graphics Accelerator, and the eDMA
  — 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Small block flash arrangement to support features such as boot block, EEPROM Emulation, operating system block
  — 8×16 KB
  — 2×64 KB
  — 2×128 KB
  — 6×256 KB
- Hardware managed flash writes, erase and verify sequence
- Censorship protection scheme to prevent Flash content visibility

## 1.4.9    SRAM

The MPC5645S microcontroller has 64 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 1 wait-state for reads and 32-bit writes
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), word (32-bit), and double-word (64-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domains applied to 56 KB and 8 KB SRAM blocks during STANDBY modes to retain contents during low power mode

## 1.4.10    On-chip graphics SRAM

The MPC5645S microcontroller has 1 MB on-chip graphics SRAM with the following features:

- Two crossbar slave ports:
  — One dedicated to the 2D Graphics Accelerator (GFX2D) access
  — One dedicated to all other crossbar masters
- Usable as general purpose SRAM
- Supports byte (8-bit), half word (16-bit), word (32-bit), and double-word (64-bit) writes for optimal use of memory
- RAM controller with hardware RAM fill function supporting all-zeroes or all-ones SRAM initialization
- Independent data buffers (one per AHB port) for maximum system performance
  — Optimized for burst transfers (read + write)
  — Programmable read prefetch capabilities

## 1.4.11    Memory Protection Unit (MPU)

The MPU features the following:

- Sixteen region descriptors for per master protection
- Start and end address defined with 32-byte granularity

- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for 4 concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

## 1.4.12    2D Graphics Accelerator (GFX2D)

- Native vector graphics rendering
  - Compatible with OpenVG1.1
  - Complete hardware OpenVG 1.1 rendering pipeline
  - Both geometry and pixel processing
  - Adaptive processing of Bezier curves and strokes
- 16-sample edge anti-aliasing
  - High image quality, font scalability, etc.
  - 4× Rotated Grid Supersampling (RGSS) AA for Flash
- 3D perspective texturing, reflections, and shadowing
- Shading (linear or radial gradient)
- Separate 2D engine for BitBlt, fill, and ROP operations
- Significant performance improvement when compared to software or 3D GPU-based OpenVG implementations

## 1.4.13    Display Control Unit (DCU3)

The DCU3 is a display controller designed to drive TFT LCD displays up to WVGA resolution using direct blit graphics and video.

The DCU3 generates all the necessary signals required to drive the TFT LCD displays: up to 24-bit RGB data bus, Pixel Clock, Data Enable, Horizontal-Sync, and Vertical-Sync.

The flexible architecture of the DCU3 enables the display of OpenVG-rendered frame buffer content and direct blit rendered graphics simultaneously.

An optional Timing Controller (TCON) and RSDS interface is available to directly drive the row and column drivers of a display panel.

Internal memory resource of the device allows to easily handle complex graphics contents (pictures, icons, languages, fonts).

The DCU3 supports 4-plane blending and 16 graphics layers. Control Descriptors (CDs) associated with each of the 16 layers enable effective merging of different resolutions into one plane to optimize use of internal memory buffers. A layer may be constructed from graphic content of various resolutions including indexed colors of 1, 2, 4, and 8 bpp, direct colors of 16, 24, and 32 bpp, and a YUV 4:2:2 color space. The ability of the DCU3 to handle input data in resolutions as low as 1bpp, 2bpp, and 4bpp enables a highly efficient use of internal memory resources of the MPC5645S. A special tiled mode can be enabled on any of the 16 layers to repeat a pattern optimizing graphic memory usage.

A hardware cursor can be managed independently of the layers at blending level increasing the efficient use of the internal DCU3 resources.

To secure the content of all critical information to be displayed, a safety mode can be activated to check the integrity of critical data along the whole system data path from the memory to the TFT pads.

The DCU3 features the following:

- Display color depth: up to 24 bpp
- Generation of all RGB and control signals for TFT
- Four-plane blending

- Maximum number of Input Layers: 16 (fixed priority)
- Dynamic Look-Up-Table (Color and Gamma Look-Up)
- α–blending range: up to 256 levels
- Transparency Mode
- Gamma Correction
- Tiled mode on all the layers
- Hardware Cursor
- Supports YCrCb 4:2:2 input data format
- RLE decode inline supporting direct read of RLE compressed images from system memory
- Critical display content integrity monitoring for Functional Safety support
- Internal Direct Memory Access (DMA) module to transfer data from internal and / or external memory
- Support displays up to 800 x 480 pixel resolutions

The DCU3 also features a Parallel Data Interface (PDI) to receive external digital video or graphic content into the DCU3. The PDI input is directly injected into the DCU3 background plane FIFO. When the PDI is activated, all the DCU3 synchronization is extracted from the external video stream to guarantee the synchronization of the two video sources.

The PDI can be used to:
- Connect a video camera output directly to the PDI
- Connect a secondary display driver as slave with a minimum of extra cost
- Connect a device gathering various Video sources
- Provide flexibility to allow the DCU to be used in slave mode (external synchronization)

The PDI features the following:
- Supported color modes:
  — 8-bit mono
  — 8-bit color multiplexed
  — RGB565
  — 16-bit/18-bit RAW color
- Supported synchronization modes:
  — embedded ITU-R BT.656-4 (RGB565 mode 2)
  — HSYNC, VSYNC
  — Data Enable
- Direct interface with DCU3 background plane FIFO
- Synchronization generation for the DCU3

## 1.4.14    Display Control Unit Lite (DCULite)

The DCULite is a display controller designed to enable the MPC5645S to drive a second TFT LCD display up to XGA resolution using direct blit graphics and video. The DCULite includes all features of the DCU3, including the PDI with the following exceptions:
- Reduced from 4-plane to 2-plane blending
- Reduced from 16 layers to 4 layers
- Reduced CLUT size

## 1.4.15    Timing Controller (TCON) and RSDS interface

The TCON enables direct drive of the row and column drivers of display panels enabling emulation of TCON ICs used in display panels.

- Programmable Timing Generation unit featuring 12 waveform generators allowing high degree of flexibility in panel waveform generation
- Reduced Swing Differential Signaling (RSDS) interface for RGB data and pixel clock
- Conforms to "RSDS 'Intra Panel' Interface Specification" Rev. 1.0 (National Semiconductor)

## 1.4.16    RLE decoder

The RLE decoder is a crossbar slave sharing a slave port with the QuadSPI module. The platform eDMA is used to stream compressed image data into and extract decompressed data out of the RLE Decoder.

- Lossless decompression
- Pixel formats supported: 8 bpp, 16 bpp, 24 bpp, and 32 bpp
- AHB mapped read and write registers in RLE_DEC to achieve higher throughput
- Programmable fill levels of read and write buffers for initiating burst transfers
- Crop feature: Support for selectively reading out a part of decompressed image data taking complete compressed data for the full image as input

## 1.4.17    DRAM controller

The DRAM controller is a multi-port DRAM controller supporting LPDDR1, DDR-1, and DDR-2 memories. The DRAM controller listens to the incoming requests to the seven buses in parallel and then sends commands to the DRAM from the highest priority bus at the current time

The seven incoming 64-bit buses are:

- DCU3
- DCULite
- e200z4d core — instruction bus
- e200z4d core — data bus
- VIU2
- GFX2D
- eDMA

The DRAM controller features the following:

- Supports CAS latency of 2, 3, and 4 clock cycles
- Master buses
  - 7 incoming master buses
  - Supports 16-byte and 32-byte bursts
  - Supports byte enables
  - Supports 4-bit priority signal for each bus
- Write buffer contains five 32-byte entries
- Supports 16-wide and 32-wide DDR1, DDR2, and LPDDR1 DRAM devices
- Controller supports one chip select, 8-bank DRAM system
- Supports dynamic on-die termination in the host device and in the DRAM
- Supports memory sizes as small as 64 Mbit

## 1.4.18    Video Input Unit (VIU2)

The VIU2 is a crossbar master module accepting an ITU656 compatible video input stream on a parallel interface, converting the pixel data to RGB or YUV format and transferring the video image to internal frame buffer memory or external DRAM if available.

- Supports 8-bit/10-bit ITU656 video input
- Output formats:
  — RGB888
  — RGB565
  — 8-bit monochrome
  — YCrCb 4:2:2
- Video downscaling
- Contrast and Brightness adjustment
- De-interlace for interlaced video image
- Internal DMA engine for data transfer to memory

## 1.4.19    Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by NXP. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via FlexCAN or LINFlex and then executed)
- Booting from external memory

Additionally the BAM:

- Enables and manages the transition of the MCU from reset to user code execution
- Configures device for serial bootload
- Enables multiple bootcode starting locations out of reset through implementation of search for valid Reset Configuration Halfword

## 1.4.20    Enhanced Modular Input/Output System (eMIOS)

This device has two eMIOS modules, each with 16 channels supporting a range of 16-bit Input Capture, Output Compare, Pulse Width Modulation, and Quadrature Decode functions.

- Selectable clock source from primary FMPLL, secondary FMPLL, external 4 - 16 MHz oscillator or 16 MHz Internal RC oscillator on a per module basis
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges
- Edge aligned output pulse width modulation
  — Programmable pulse period and duty cycle
  — Supports 0% and 100% duty cycle
  — Shared or independent time bases
- Programmable phase shift between channels
- 4 channels of Quadrature Decode
- DMA transfer support

## 1.4.21 Analog-to-Digital Converter (ADC)

The ADC features the following:

- 10-bit A/D resolution
- 0–5 V or 0–3.3 V common mode conversion range
- Supports conversions speeds of up to 1μs
- 20 internal and 8 external channels support
- Up to 20 single-ended inputs channels
  — 10 channels configured as input only pins
    – 10-bit ± 2 counts accuracy (TUE)
  — 10 channels configured to have alternate function as general purpose input/output pins
    – 10-bit ± 3 counts accuracy (TUE)
- External multiplexer support to increase up to 27 channels
  — Automatic 1 × 8 multiplexer control
  — External multiplexer connected to a dedicated input channel
  — Shared register between the 8 external channels
- Result register available for every non-multiplexed channel
- Configurable Left or Right aligned result format
- Supports for one-shot, scan, and injection conversion modes
- Injection mode status bit implemented on adjacent 16-bit register for each result
  — Supports Access to Result and injection status with single 32-bit read
- Independently enabling of function for channels:
  — Pre-sampling
  — Offset error cancellation
  — Offset Refresh
- Conversion Triggering support
  — Internal conversion triggering from periodic interrupt timer (PIT)
- Four configurable analog comparator channels offering range comparison with triggered alarm
  — Greater than
  — Less than
  — Out of range
- All unused analog pins available as general purpose input pins
- Selected unused analog pins available as general purpose pins
- Power Down mode
- Optional support for DMA transfer of results

## 1.4.22 Deserial Serial Peripheral Interface (DSPI)

The DSPI modules provide a synchronous serial interface for communication between the MCU and external devices.

The DSPI features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate

- Programmable data frames from 4 to 16 bits
- Up to 3 chip select lines available, depending on package and pin multiplexing, enable 8 external devices to be selected using external muxing from a single DSPI
- Eight clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- General purpose I/O functionality on pins when not used for SPI
- Queueing operation possible through use of eDMA

## 1.4.23    FlexCAN

The MPC5645S includes up to three controller area network (FlexCAN) modules. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

Each FlexCAN module offers the following:

- Compliant with CAN protocol specification, Version 2.0B active
- 64 mailboxes, each configurable as transmit or receive
    — Mailboxes configurable while module remains synchronized to CAN bus
- Transmit features
    — Supports configuration of multiple mailboxes to form message queues of scalable depth
    — Arbitration scheme according to message ID or message buffer number
    — Internal arbitration to guarantee no inner or outer priority inversion
    — Transmit abort procedure and notification
- Receive features
    — Individual programmable filters for each mailbox
    — 8 mailboxes configurable as a 6-entry receive FIFO
    — 8 programmable acceptance filters for receive FIFO
- Programmable clock source
    — System clock
    — Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities
- CAN Sampler
    — Can catch the 1st message sent on the CAN network while the MCU is stopped, which guarantees a clean startup of the system without missing messages on the CAN network
    — The CAN sampler is connected to one of the CAN RX pins

## 1.4.24    Serial communication interface module (LINFlex)

The MPC5645S devices include up to four LINFlex modules and support for LIN Master mode, LIN Slave mode, and UART mode. The modules are LIN state machine compliant to the LIN 1.3, 2.0, and 2.1 Specifications and handle LIN frame transmission and reception without CPU intervention.

Other features include:

- Autonomous LIN frame handling
- Message buffer to store identifier and up to eight data bytes
- Supports message length of up to 64 bytes

- Detection and flagging of LIN errors
- Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
- Classic or extended checksum calculation
- Configurable Break duration of up to 36-bit times
- Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
- Diagnostic features
  — Loop back
  — Self Test
  — LIN bus stuck dominant detection
- Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  — Autonomous LIN header handling
  — Autonomous LIN response handling
  — Discarding of irrelevant LIN responses using up to 16 ID filters
- UART mode
  — Full-duplex operation
  — Standard non return-to-zero (NRZ) mark/space format
  — Data buffers with 4-byte receive, 4-byte transmit
  — Configurable word length (8-bit or 9-bit words)
  — Error detection and flagging
    – Parity, noise, and framing errors
  — Interrupt driven operation with 4 interrupts sources
  — Separate transmitter and receiver CPU interrupt sources
  — 16-bit programmable baud-rate modulus counter and 16-bit fractional
  — Two receiver wakeup methods

## 1.4.25    Inter-Integrated Circuit (I$^2$C) controller modules

The MPC5645S includes four I$^2$C modules. Each module features the following:

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I$^2$C bus standard
- Multi-master operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

## 1.4.26    System clocks and clock generation modules

The system clock on the MPC5645S can be derived from an external oscillator, an on-chip FMPLL, or the internal 16 MHz oscillator.

The source system clock frequency can be changed via an on-chip programmable clock divider (÷1 to ÷32). An additional programmable peripheral bus clock divider (ratios ÷1 to ÷15) is also available.

The MPC5645S has two on-chip FMPLLs (primary and secondary). Each features the following:

- Input clock frequency from 4 MHz to 16 MHz
- Lock detect circuitry continuously monitors lock status
- Loss Of Clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and reduction of number of external components required)
- Support for frequency ramping from PLL

The primary FMPLL module is for use as a system clock source. The secondary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation.

The fast external oscillator provides the following features:

- Input frequency range 4–16 MHz
- Square-wave input mode
- Oscillator input mode 3.3 V (5.0 V)
- Automatic level control
- Low power consumption
- PLL reference

The MPC5645S also includes the following oscillators:

- 32 KHz low power external oscillator for slow execution, low power, and RTC
- Dedicated internal 128 kHz RC oscillator for low power mode operation and self wake-up
  - ±10% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support improved accuracy with in-application calibration
- Dedicated 16 MHz internal RC oscillator
  - Used as default clock source out of reset
  - Provides a clock for rapid start-up from low power modes
  - Provides a back-up clock in the event of PLL or External Oscillator clock failure
  - Offers an independent clock source for the SWT
  - ±5% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support frequency adjustment with in-application calibration

## 1.4.27    Periodic Interrupt Timer (PIT)

The PIT features the following:

- Eight general purpose interrupt timers
- Two dedicated interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency

## 1.4.28    Real Time Counter (RTC)

The Real Timer Counter supports wake-up from Low Power modes or Real Time Clock generation

- Configurable resolution for different timeout periods
  - 1 s resolution for >1 hour period
  - 1 ms resolution for 2 second period

- Selectable clock sources from external 32 KHz crystal, external 4–16 MHz crystal, internal 128 kHz RC oscillator or divided internal 16 MHz RC oscillator

## 1.4.29 System Timer Module (STM)

The STM is a 32-bit timer designed to support commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescale value (1 to 256).

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

## 1.4.30 Software Watchdog Timer (SWT)

The SWT features the following:

- Watchdog supporting software activation or enabled out of Reset
- Supports normal or windowed mode
- Watchdog timer value writable once after reset
- Watchdog supports optional halting during low power modes
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Clock source: 128 kHz RC oscillator

## 1.4.31 Stepper Motor Controller (SMC)

The SMC module is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total) driving up to 6 stepper motors.

The SMC module includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- Left, right, or center aligned PWM
- Output slew rate control
- Output Short Circuit Detection

This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

## 1.4.32 Stepper Stall Detect (SSD)

The SSD module provides a circuit to measure and integrate the induced voltage on the non-driven coil of a stepper motor using full steps when the gauge pointer is returning to zero (RTZ).

The SSD module features the following:

- Programmable full step state
- Programmable integration polarity
- Blanking (recirculation) state
- 16-bit integration accumulator register

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- 16-bit modulus down counter with interrupt

## 1.4.33  Sound Generator Module (SGM)

The SGM features the following:

- 4-channel audio mixer
- Each channel capable of independent Tone generation or Wave playback
- Individual channel volume control (8-bit resolution)
- Tone Mode:
    — Programmable Tone frequency
    — Programmable amplitude envelope: attack, duration, and decay
    — Programmable number of tone pulses and inter-tone duration
- Wave Mode:
    — One FIFO per channel working in conjunction with eDMA
    — Supports standard audio sampling rates (4 kHz, 8 kHz, 11.025 kHz, 16 kHz, 22.050 kHz, 32 kHz, 44.100 kHz, 48 kHz)
    — Same sample rate applies to all channels
    — 8-bit, 12-bit, 16-bit input data formats
    — Programmable wave duration and inter-wave duration
    — Repeat mode with programmable number of wave playbacks
- SGM Output:
    — 16-bit PWM channel
    — Integrated $I^2S$ master interface for connection to external audio DAC

## 1.4.34  IEEE 1149.1 JTAG controller (JTAGC)

JTAGC features the following:

- Backward compatible to standard JTAG IEEE 1149.1-2001 test access port (TAP) interface
- Support for boundary scan testing

## 1.4.35  Nexus Development Interface (NDI)

The Nexus 3 module is compliant with Class 3 of the IEEE-ISTO 5001-2008 standard, with additional Class 4 features available. The following features are implemented:

- Program Trace via Branch Trace Messaging (BTM). Branch trace messaging displays program flow discontinuities (direct and indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus static code may be traced.
- Data Trace via Data Write Messaging (DWM) and Data Read Messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to selected internal memory resources.
- Ownership Trace via Ownership Trace Messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An Ownership Trace Message is transmitted when a new process/task is activated, allowing the development tool to trace ownership flow.
- Run-time access to embedded processor memory map via the JTAG port. This allows for enhanced download/upload capabilities.
- Watchpoint Messaging via the auxiliary pins provides visibility when debugging.
- Watchpoint Trigger enablement of Program and/or Data Trace Messaging enhances debug capability.

- Data Acquisition Messaging (DQM) allows code to be instrumented to export customized information to the Nexus Auxiliary Output Port.
- Address Translation Messaging via program correlation messages displays updates to the TLB for use by the debugger in correlating virtual and physical address information.
- Auxiliary interface for higher data input/output.
- Registers for Program Trace, Data Trace, Ownership Trace, and Watchpoint Trigger.
- All features are controllable and configurable via the JTAG port.
- Nexus Auxiliary port is supported on the 416BGA package.

# 2 Pinout and signal descriptions

## 2.1 176 LQFP package pinout

Figure 2 shows the pinout for the 176-pin LQFP package.



**Figure 2. 176-pin LQFP pinout**

## 2.2    208 LQFP package pinout
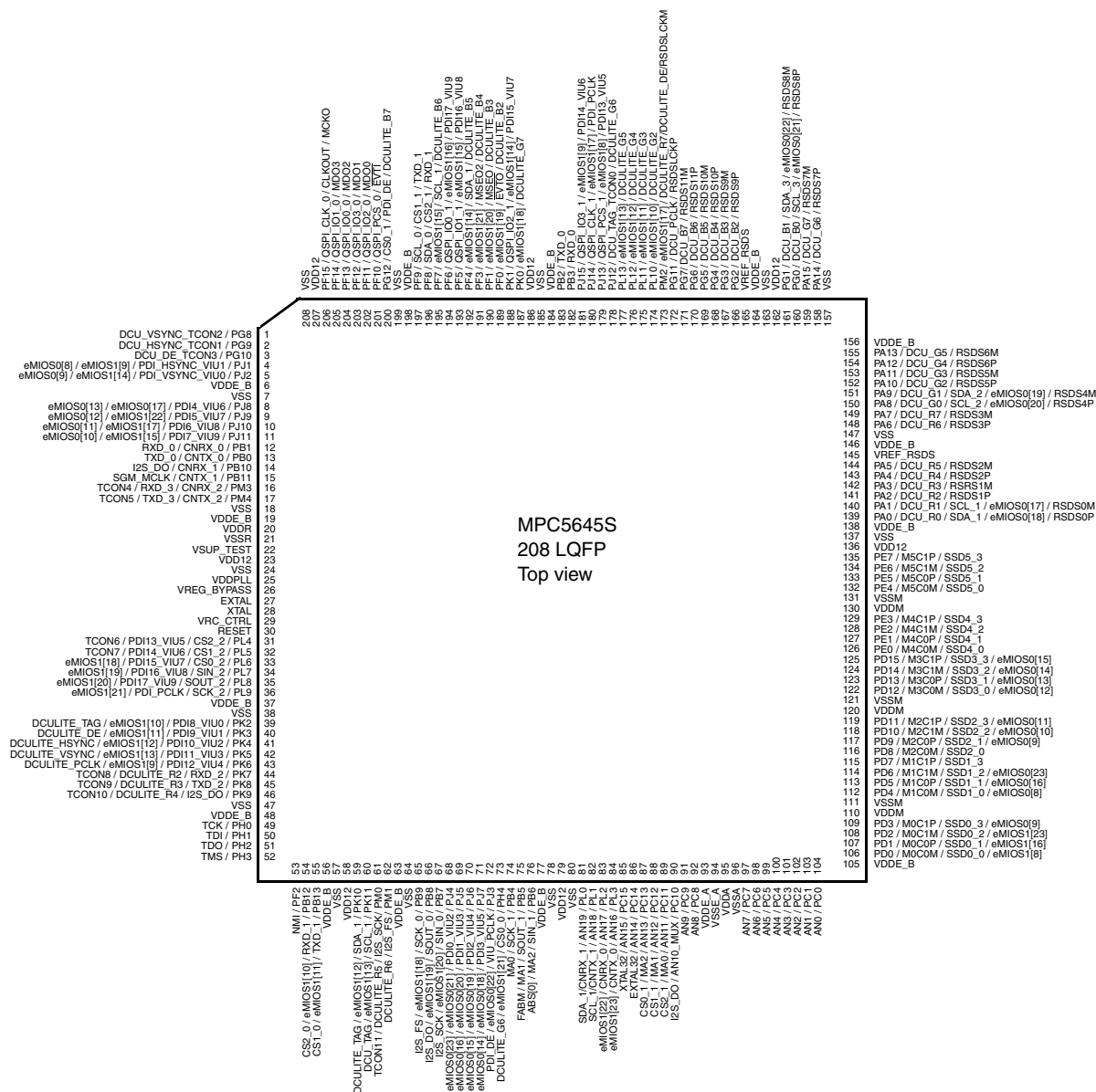
Figure 3 shows the pinout for the 208-pin LQFP package.



**Figure 3. 208-pin LQFP pinout**

## 2.3 416 TEPBGA package pinout

Figure 4 shows the pinout for the 416 TEPBGA package.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | ddr_dq[26] | ddr_dq[27] | ddr_dq[28] | ddr_dq[29] | ddr_dq[30] | ddr_dq[31] | ddr_ba[2] | ddr_ba[0] | ddr_ba[1] | ddr_address[0] | ddr_address[4] | ddr_address[6] | ddr_address[8] | ddr_address[12] | PG12 | PF14 | PF10 | PF8 | PF5 | PF3 | PK0 | PB3 | PI12 | PL11 | PG7 | PG6 |
| B | ddr_dq[25] | VSS | ddr_dqs[3] | ddr_dm[3] | VSS | ddr_cas | ddr_ras | VSS | ddr_web | ddr_address[1] | VSS | ddr_address[7] | ddr_address[9] | VSS | ddr_address[15] | PF13 | VDDE | PF15 | VSS | PF1 | VDDE | PI15 | PL13 | VDDE | VSS | PG5 |
| C | ddr_dq[23] | VDDE_DDR | VSS | ddr_dq[24] | VDDE_DDR | VSS | ddr_dram_clk | VDDE_DDR | VSS | ddr_address[2] | VDDE_DDR | VSS | ddr_address[10] | VSS | VSS | PF12 | VSS | PF7 | VDDE | PF0 | VSS | PI14 | PL12 | PL10 | PG3 | PG4 |
| D | ddr_dq[19] | ddr_dq[20] | ddr_dq[21] | ddr_dq[22] | ddr_odt | VDD33_DDR | ddr_dram_clkb | ddr_cke | ddr_cs | ddr_address[3] | ddr_address[5] | VDD33_DDR | ddr_address[11] | ddr_address[13] | ddr_address[14] | PF11 | PF9 | PF6 | PF4 | PK1 | PB2 | PI13 | PM2 | VREF_RSDS2 | PG2 | PG1 |
| E | ddr_dq[17] | VSS | VDDE_DDR | ddr_dq[18] | | | | | | | | | | | | | | | | | | | PG11 | VSS | VDDE | PG0 |
| F | ddr_dq[16] | MVTT3 | VSS | VDD33_DDR | | | | | | | | | | | | | | | | | | | PA15 | PA14 | PA13 | PA12 |
| G | ddr_dq[15] | ddr_dqs[2] | ddr_dm[2] | ddr_dq[14] | | | | | | | | | | | | | | | | | | | PA11 | PA9 | PA8 | PA7 |
| H | ddr_dq[13] | VSS | VDDE_DDR | ddr_dq[12] | | | | | | | | | | | | | | | | | | | PA10 | VDDE | VSS | VA6 |
| J | ddr_dq[11] | MVTT2 | VSS | MVREF | | | | | | | | | | | | | | | | | | | PA3 | VREF_RSDS1 | PA5 | PA4 |
| K | ddr_dq[9] | ddr_dqs[1] | ddr_dm[1] | ddr_dq[10] | | | | | | VDD12 | VSS | VDD12 | VSS | VSS | VSS | VDD12 | VSS | | | | | | PA2 | VSS | PA1 | PA0 |
| L | ddr_dq[8] | VSS | VDDE_DDR | ddr_dq[7] | | | | | | VSS | VDD12 | VSS | VDD12 | VSS | VDD12 | VSS | VDD12 | | | | | | PM13 | PM12 | VDDE | PI0 |
| M | ddr_dq[5] | MVTT1 | VSS | ddr_dq[6] | | | | | | VDD12 | VSS | VSS | VSS | VSS | VSS | VDD12 | VSS | | | | | | PO7 | PO6 | PO5 | PO4 |
| N | ddr_dq[3] | ddr_dqs[0] | VDDE_DDR | ddr_dq[4] | | | | | | VSS | VDD12 | VSS | VSS | VSS | VSS | VSS | VDD12 | | | | | | PO3 | VDDE | PO2 | PO1 |
| P | ddr_dq[1] | VSS | ddr_dm[0] | ddr_dq[2] | | | | | | VDD12 | VSS | VSS | VSS | VSS | VSS | VDD12 | VSS | | | | | | PO0 | PN15 | VSS | PN14 |
| R | ddr_dq[0] | MVTT0 | VSS | VDD33_DDR | | | | | | VSS | VDD12 | VSS | VSS | VDD12 | VSS | VSS | VDD12 | | | | | | PE7 | PE6 | PN13 | PN12 |
| T | PG10 | PG9 | VDDE | PG8 | | | | | | VDD12 | VSS | VDD12 | VSS | VSS | VSS | VDD12 | VSS | | | | | | PE5 | PE4 | PE3 | PE2 |
| U | PI9 | PI8 | PI2 | PI1 | | | | | | VSS | VDD12 | VSS | VDD12 | VSS | VDD12 | VSS | VDD12 | | | | | | PE1 | VSSM | VDDM | PE0 |
| V | PB1 | VSS | PI11 | PI10 | | | | | | | | | | | | | | | | | | | PD15 | PD14 | PD13 | PD12 |
| W | RESET | PB10 | VDDE | PB0 | | | | | | | | | | | | | | | | | | | PD11 | VDDM | VSSM | PD10 |
| Y | VSS | PM4 | PM3 | PB11 | | | | | | | | | | | | | | | | | | | PD9 | PD8 | PD7 | PD6 |
| AA | XTAL | VREG_BYPASS | VRC_CTRL | VDDREG | | | | | | | | | | | | | | | | | | | PD5 | VSSM | VDDM | PD4 |
| AB | EXTAL | PL4 | VSS | VDDPLL | | | | | | | | | | | | | | | | | | | PD3 | PD2 | PD1 | PD0 |
| AC | VSUP_TEST | PL5 | PN0 | PK4 | PK6 | PH0 | PF2 | PB13 | PK11 | PN2 | PN4 | PN8 | PB9 | PB7 | PJ7 | PB5 | MCKO | MDO6 | MDO10 | MVO0 | PC0 | VDDA | VSSEH_ADC | PC3 | PC1 | PC2 |
| AD | PL6 | VDDE | PN1 | VSS | PK7 | PH1 | VDDE | EVTI | MSEO | VSS | PN5 | PN9 | VDDE | PJ4 | PJ3 | VSS | MSEO2 | MDO7 | VDDE | MDO1 | PC6 | VSSA | VDDEH_ADC | PC4 | PC7 | PC5 |
| AE | PL7 | VSS | PK2 | VDDE | PK8 | PH2 | VSS | EVTO | PM0 | VDDE | PN6 | PN10 | VSS | PJ5 | PH4 | VDDE | MDO4 | MDO8 | VSS | MDO2 | PL1 | PL0 | PC10 | PC11 | PC9 | PC8 |
| AF | PL8 | PL9 | PK3 | PK5 | PK9 | PH3 | PB12 | PK10 | PM1 | PN3 | PN7 | PN11 | PB8 | PJ6 | PB4 | PB6 | MDO5 | MDO9 | MDO11 | MDO3 | PL3 | PL2 | PC15 | PC14 | PC13 | PC12 |

**Figure 4. 416 TEPBGA package pinout**

## 2.4    Signal description

The following sections provide signal descriptions and related information about the signals' functionality and configuration.

### 2.4.1    Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are floating with the following exceptions:

- PB[5] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash memory.
- RESET pad is driven low. This is released only after PHASE2 reset completion.
- Fast (4-16 MHz) external oscillator pads (EXTAL, XTAL) are tristate.
- The following pads are pull-up:
  — PB[6]
  — PH[0]
  — PH[1]
  — PH[3]

### NOTE

TCK pin must have an external pull-down resistor of 4.7 K.

### 2.4.2    Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

**Table 3. Voltage supply pin descriptions**

| Supply pin | Function | Pin number | | |
|---|---|---|---|---|
| | | **176 LQFP** | **208 LQFP** | **416 TEPBGA** |
| $V_{DD12}$[1] | 1.2 V core supply (1.08 V - 1.32 V) | 23, 50, 67, 110, 138, 175 | 23, 58, 79, 136, 162, 186, 207 | K10,K12,K14,K16,L11,L13,L15,L17,M10,M16,N11,N17,P10,P16,R11,R17,T10,T12,T14,T16,U11,U13,U15,U17 |
| $V_{SS}$ | 1.2 V ground | 7, 18, 36, 49, 66, 68, 111, 123, 133, 139, 154, 167, 176 | 7, 18, 38, 47, 57, 64, 78, 80, 137, 147, 157, 163, 185, 199, 208 | AB3,AD10,AD16,AD4,AE13,AE19,AE2,AE7,B11,B14,B19,B2,B25,B5,B8,C12,C15,C17,C21,C3,C6,C9,E2,E24,F3,H2,H25,J3,K11,K13,K15,K17,K24,L10,L12,L14,L16,L2,M11,M12,M13,M14,M15,M17,M3,N10,N12,N13,N14,N15,N16,P11,P12,P13,P14,P15,P17,P2,P25,R10,R12,R13,R14,R15,R16,R3,T11,T13,T15,T17,U10,U12,U14,U16,V2,Y1 |
| | VDD12 ground and VDDPLL ground (VSSPLL) | 24 | 24 | — |
| $V_{DDE\_B}$ | 3.3 V I/O supply. This supply is shared with internal flash, 16 MHz IRC oscillator and 4–16MHz crystal oscillator. | 6, 19, 37, 48, 65, 89, 112, 122, 132, 140, 166 | 6, 19, 37, 48, 56, 63, 77, 105, 138, 146, 156, 164, 184, 198 | AD13,AD19,AD2,AD7,AE10,AE16,AE4,B17,B21,B24,C19,E25,H24,L25,N24,W3 |
| $V_{DDA}$[2] | 3.3 V/5 V reference voltage and analog supply for A/D converter. This supply is shared with the SXOSC. | 79 | 95 | AC22 |
| $V_{SSA}$ | Reference ground and analog ground for A/D converter | 80 | 96 | AD22 |
| $V_{DDR}$ | Voltage regulator VREG supply | 20 | 20 | AA4 |
| $V_{SSR}$ | Voltage regulator ground | 21 | 21 | — |
| $V_{DDE\_A}$[2] | 3.3 V/5 V I/O supply. This supply is shared with the SXOSC. | 77 | 93 | AD23 |
| $V_{SSE\_A}$ | 3.3 V/5 V I/O supply ground | 78 | 94 | AC23 |
| $V_{DDM}$ | Stepper motor 3.3 V/5 V pad supply. SSD shares this supply. | 94, 104 | 110, 120, 130 | U25,W24,AA25 |
| $V_{SSM}$ | Stepper motor ground | 95, 105 | 111, 121, 131 | U24,W24,AA24 |

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Table 3. Voltage supply pin descriptions (continued)

| Supply pin | Function | Pin number | | |
|---|---|---|---|---|
| | | 176 LQFP | 208 LQFP | 416 TEPBGA |
| $V_{DDPLL}$ | 1.2 V PLL supply | 25 | 25 | AB4 |
| $V_{SUP\_TEST}$[3] | 9 V - 12 V flash test analog write signal | 22 | 22 | AC1 |
| $V_{DD\_DR}$ | 1.8V, 2.5V, and 3.3V DDR SDRAM supply | — | — | C2,C5,C8,C11,C14, E3,H3,L3,N3,T3 |
| $V_{DD33\_DR}$ | Functional supply for SDRAM pads (where available must be >= VDD_DR) | — | — | D6, D12, F4, R4 |

[1] Decoupling capacitors must be connected between these pins and the nearest $V_{SS}$ pin.

[2] VDDA must be at the same voltage as VDDE_A.

[3] This signal needs to be connected to ground during normal operation.

## 2.4.3 System pins

The system pins are listed in Table 4.

### Table 4. System pin descriptions

| System pin | Function | I/O direction | Pad type | RESET configuration[1] | Pin number | | |
|---|---|---|---|---|---|---|---|
| | | | | | 176 LQFP | 208 LQFP | 416 TEPBGA |
| $\overline{RESET}$ | Bidirectional reset with Schmitt-Trigger characteristics and noise filter. | I/O | M | Input, weak pull up | 30 | 30 | W1 |
| EXTAL | Analog input to the oscillator amplifier circuit. Input for the clock generator in bypass mode. | I | X | — | 27 | 27 | AB1 |
| XTAL | Analog output of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used. | O | X | — | 28 | 28 | AA1 |
| EXTAL32 | Analog input of the 32KHz oscillator amplifier circuit. | O | S | — | 70 | 86 | AF24 |
| XTAL32 | Analog output of the 32 KHz oscillator amplifier circuit. Input for the clock generator in bypass mode. | I | S | — | 69 | 85 | AF23 |

Table 4. System pin descriptions (continued)

| System pin | Function | I/O direction | Pad type | RESET configuration[1] | Pin number | | |
|---|---|---|---|---|---|---|---|
| | | | | | 176 LQFP | 208 LQFP | 416 TEPBGA |
| NMI | Non-Maskable Interrupt | I/O | S | Input, none | 45 | 53 | AC7 |
| VRC_CTRL | Voltage Regulator external NPN Ballast base control pin | | Analog | — | 29 | 29 | AA3 |
| VREF_RSDS[2] | RSDS interface reference voltage | | Analog | — | — | 145, 165 | J24,D24 |
| VREG_BYPASS[3] | Pin used for factory testing | I | — | — | 26 | 26 | AA2 |

[1] Reset configuration is given as I/O direction and pull direction (for example, "Input, pullup").

[2] Although this signal is not a supply for RSDS pads, it needs to be terminated in an external capacitor with a value of 47 pF.

[3] VREG_BYPASS should be connected to ground during normal operation.

## 2.4.4 Nexus pins

On the 176 LQFP and the 208 LQFP package options a reduced set of Nexus pins are optionally available, multiplexed with GPIO pins.

On the 416 TEPBGA package option all Nexus pins are dedicated to Nexus only.

Table 5. Nexus pins

| System pin | Function | Pad type | PCR | Pin number[1] | | |
|---|---|---|---|---|---|---|
| | | | | 176 LQFP | 208 LQFP | 416 TEPBGA |
| EVTI | Nexus Event In | M | PCR[80] | 169 | 201 | A17 |
| EVTO | Nexus Event Out | M | PCR[70] | 157 | 189 | C20 |
| MCKO | Nexus Msg Clock Out | F | PCR[85] | 174 | 206 | B18 |
| MSEO[0] | Nexus Msg Start/End Out | M | PCR[71] | 158 | 190 | B20 |
| MSEO[2] | Nexus Msg Start/End Out | M | PCR[73] | 159 | 191 | A20 |
| MDO[0] | Nexus Msg Data Out | M | PCR[81] | 170 | 202 | D16 |
| MDO[1] | Nexus Msg Data Out | M | PCR[82] | 171 | 203 | C16 |
| MDO[2] | Nexus Msg Data Out | M | PCR[83] | 172 | 204 | B16 |
| MDO[3] | Nexus Msg Data Out | M | PCR[84] | 173 | 205 | A16 |
| EVTI | Nexus Event In | M | PCR[197] | n/a | n/a | AD8 |
| EVTO | Nexus Event Out | M | PCR[198] | n/a | n/a | AE8 |
| MCKO | Nexus Msg Clock Out | F | PCR[200] | n/a | n/a | AC17 |
| MSEO[0] | Nexus Msg Start/End Out | M | PCR[199] | n/a | n/a | AD9 |
| MSEO[2] | Nexus Msg Start/End Out | M | PCR[201] | n/a | n/a | AD17 |
| MDO[0] | Nexus Msg Data Out | M | PCR[185] | n/a | n/a | AC20 |

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**Table 5. Nexus pins (continued)**

| System pin | Function | Pad type | PCR | Pin number[1] | | |
|---|---|---|---|---|---|---|
| | | | | **176 LQFP** | **208 LQFP** | **416 TEPBGA** |
| MDO[1] | Nexus Msg Data Out | M | PCR[186] | n/a | n/a | AD20 |
| MDO[2] | Nexus Msg Data Out | M | PCR[187] | n/a | n/a | AE20 |
| MDO[3] | Nexus Msg Data Out | M | PCR[188] | n/a | n/a | AF20 |
| MDO[4] | Nexus Msg Data Out | M | PCR[189] | n/a | n/a | AE17 |
| MDO[5] | Nexus Msg Data Out | M | PCR[190] | n/a | n/a | AF17 |
| MDO[6] | Nexus Msg Data Out | M | PCR[191] | n/a | n/a | AC18 |
| MDO[7] | Nexus Msg Data Out | M | PCR[192] | n/a | n/a | AD18 |
| MDO[8] | Nexus Msg Data Out | M | PCR[193] | n/a | n/a | AE18 |
| MDO[9] | Nexus Msg Data Out | M | PCR[194] | n/a | n/a | AF18 |
| MDO[10] | Nexus Msg Data Out | M | PCR[195] | n/a | n/a | AC19 |
| MDO[11] | Nexus Msg Data Out | M | PCR[196] | n/a | n/a | AF19 |

[1] On the 176 LQFP and 208 LQFP package options the Nexus pins are multiplexed with other GPIO. On the 416 TEPBGA package, there are additional dedicated Nexus pins.

## 2.4.5　DRAM interface

The DRAM interface pins are listed in Table 6.

**Table 6. DRAM interface pin summary**

| Port pin[1] | Function | I/O direction | Pad type | PCR | RESET config[2] | Pin number |
|---|---|---|---|---|---|---|
| | | | | | | **416 TEPBGA** |
| **DRAM Data Bus** | | | | | | |
| DDR_DQ[31] | DRAM Data Bus [31] | I/O | DDR | PCR[237] | None, None | A6 |
| DDR_DQ[30] | DRAM Data Bus [30] | I/O | DDR | PCR[238] | None, None | A5 |
| DDR_DQ[29] | DRAM Data Bus [29] | I/O | DDR | PCR[239] | None, None | A4 |
| DDR_DQ[28] | DRAM Data Bus [28] | I/O | DDR | PCR[240] | None, None | A3 |
| DDR_DQ[27] | DRAM Data Bus [27] | I/O | DDR | PCR[241] | None, None | A2 |
| DDR_DQ[26] | DRAM Data Bus [26] | I/O | DDR | PCR[242] | None, None | A1 |
| DDR_DQ[25] | DRAM Data Bus [25] | I/O | DDR | PCR[243] | None, None | B1 |
| DDR_DQ[24] | DRAM Data Bus [24] | I/O | DDR | PCR[244] | None, None | C4 |
| DDR_DQ[23] | DRAM Data Bus [23] | I/O | DDR | PCR[245] | None, None | C1 |
| DDR_DQ[22] | DRAM Data Bus [22] | I/O | DDR | PCR[246] | None, None | D4 |
| DDR_DQ[21] | DRAM Data Bus [21] | I/O | DDR | PCR[247] | None, None | D3 |
| DDR_DQ[20] | DRAM Data Bus [20] | I/O | DDR | PCR[248] | None, None | D2 |
| DDR_DQ[19] | DRAM Data Bus [19] | I/O | DDR | PCR[249] | None, None | D1 |

**Table 6. DRAM interface pin summary (continued)**

| Port pin[1] | Function | I/O direction | Pad type | PCR | RESET config[2] | Pin number 416 TEPBGA |
|---|---|---|---|---|---|---|
| DDR_DQ[18] | DRAM Data Bus [18] | I/O | DDR | PCR[250] | None, None | E4 |
| DDR_DQ[17] | DRAM Data Bus [17] | I/O | DDR | PCR[251] | None, None | E1 |
| DDR_DQ[16] | DRAM Data Bus [16] | I/O | DDR | PCR[252] | None, None | F1 |
| DDR_DQ[15] | DRAM Data Bus [15] | I/O | DDR | PCR[253] | None, None | G1 |
| DDR_DQ[14] | DRAM Data Bus [14] | I/O | DDR | PCR[254] | None, None | G4 |
| DDR_DQ[13] | DRAM Data Bus [13] | I/O | DDR | PCR[255] | None, None | H1 |
| DDR_DQ[12] | DRAM Data Bus [12] | I/O | DDR | PCR[256] | None, None | H4 |
| DDR_DQ[11] | DRAM Data Bus [11] | I/O | DDR | PCR[257] | None, None | J1 |
| DDR_DQ[10] | DRAM Data Bus [10] | I/O | DDR | PCR[258] | None, None | K4 |
| DDR_DQ[9] | DRAM Data Bus [9] | I/O | DDR | PCR[259] | None, None | K1 |
| DDR_DQ[8] | DRAM Data Bus [8] | I/O | DDR | PCR[260] | None, None | L1 |
| DDR_DQ[7] | DRAM Data Bus [7] | I/O | DDR | PCR[261] | None, None | L4 |
| DDR_DQ[6] | DRAM Data Bus [6] | I/O | DDR | PCR[262] | None, None | M4 |
| DDR_DQ[5] | DRAM Data Bus [5] | I/O | DDR | PCR[263] | None, None | M1 |
| DDR_DQ[4] | DRAM Data Bus [4] | I/O | DDR | PCR[264] | None, None | N4 |
| DDR_DQ[3] | DRAM Data Bus [3] | I/O | DDR | PCR[265] | None, None | N1 |
| DDR_DQ[2] | DRAM Data Bus [2] | I/O | DDR | PCR[266] | None, None | P4 |
| DDR_DQ[1] | DRAM Data Bus [1] | I/O | DDR | PCR[267] | None, None | P1 |
| DDR_DQ[0] | DRAM Data Bus [0] | I/O | DDR | PCR[268] | None, None | R1 |
| **DRAM Data Strobes** | | | | | | |
| DDR_DQS[3] | DRAM Data Strobe [3] | I/O | DDR | PCR[232] | None, None | B3 |
| DDR_DQS[2] | DRAM Data Strobe [2] | I/O | DDR | PCR[231] | None, None | G2 |
| DDR_DQS[1] | DRAM Data Strobe [1] | I/O | DDR | PCR[230] | None, None | K2 |
| DDR_DQS[0] | DRAM Data Strobe [0] | I/O | DDR | PCR[229] | None, None | N2 |
| **DRAM Data Enables** | | | | | | |
| DDR_DM[3] | DRAM Data Enable [3] | Output | DDR | PCR[236] | Output, None | B4 |
| DDR_DM[2] | DRAM Data Enable [2] | Output | DDR | PCR[235] | Output, None | G3 |
| DDR_DM[1] | DRAM Data Enable [1] | Output | DDR | PCR[234] | Output, None | K3 |
| DDR_DM[0] | DRAM Data Enable [0] | Output | DDR | PCR[233] | Output, None | P3 |
| **DRAM Address** | | | | | | |

**Table 6. DRAM interface pin summary (continued)**

| Port pin[1] | Function | I/O direction | Pad type | PCR | RESET config[2] | Pin number |
|---|---|---|---|---|---|---|
| | | | | | | 416 TEPBGA |
| DDR_A[15] | DRAM address [15] | Output | DDR | PCR[217] | Output, None | B15 |
| DDR_A[14] | DRAM address [14] | Output | DDR | PCR[216] | Output, None | D15 |
| DDR_A[13] | DRAM address [13] | Output | DDR | PCR[215] | Output, None | D14 |
| DDR_A[12] | DRAM address [12] | Output | DDR | PCR[214] | Output, None | A14 |
| DDR_A[11] | DRAM address [11] | Output | DDR | PCR[213] | Output, None | D13 |
| DDR_A[10] | DRAM address [10] | Output | DDR | PCR[212] | Output, None | C13 |
| DDR_A[9] | DRAM address [9] | Output | DDR | PCR[211] | Output, None | B13 |
| DDR_A[8] | DRAM address [8] | Output | DDR | PCR[210] | Output, None | A13 |
| DDR_A[7] | DRAM address [7] | Output | DDR | PCR[209] | Output, None | B12 |
| DDR_A[6] | DRAM address [6] | Output | DDR | PCR[208] | Output, None | A12 |
| DDR_A[5] | DRAM address [5] | Output | DDR | PCR[207] | Output, None | D11 |
| DDR_A[4] | DRAM address [4] | Output | DDR | PCR[206] | Output, None | A11 |
| DDR_A[3] | DRAM address [3] | Output | DDR | PCR[205] | Output, None | D10 |
| DDR_A[2] | DRAM address [2] | Output | DDR | PCR[204] | Output, None | C10 |
| DDR_A[1] | DRAM address [1] | Output | DDR | PCR[203] | Output, None | B10 |
| DDR_A[0] | DRAM address [0] | Output | DDR | PCR[202] | Output, None | A10 |
| **DRAM Bank Address** | | | | | | |
| DDR_BA[2] | DRAM Bank Address[2] | Output | DDR | PCR[220] | Output, None | A9 |
| DDR_BA[1] | DRAM Bank Address[1] | Output | DDR | PCR[219] | Output, None | A8 |
| DDR_BA[0] | DRAM Bank Address[0] | Output | DDR | PCR[218] | Output, None | A7 |
| **DRAM Control** | | | | | | |

**Table 6. DRAM interface pin summary (continued)**

| Port pin[1] | Function | I/O direction | Pad type | PCR | RESET config[2] | Pin number 416 TEPBGA |
|---|---|---|---|---|---|---|
| DDR_CAS | Column Address Strobe | Output | DDR | PCR[221] | Output, None | B6 |
| DDR_RAS | Row Address Strobe | Output | DDR | PCR[227] | Output, None | B7 |
| DDR_WEB | Write Enable | Output | DDR | PCR[228] | Output, None | B9 |
| DDR_ODT | DRAM On-die termination | Output | DDR | PCR[226] | Output, Pull Down | D5 |
| DDR_CLK | DRAM Clock | Output | DDR | PCR[225] | Output, None | C7 |
| DDR_CLKB | DRAM Clock bar | Output | DDR | NA | Output, None | D7 |
| DDR_CK | DRAM Clock Enable | Output | DDR | PCR[222] | Output, Pull Down | D8 |
| DDR_CS | DRAM Chip Select | Output | DDR | PCR[223] | Output, None | D9 |
| MVREF | DDR Reference Voltage | Input | — | NA | — | J4 |
| MVTT | DRAM Termination Voltage | Input | — | NA | — | F2,J2,M2,R2 |

1 These port pins are disabled and unpowered on packages where the DRAM interface is not bonded out.

2 Reset configuration is given as I/O direction and pull direction (for example, "Input, pullup").

## 2.4.6 VIU muxing

The DCU3, DCULite and VIU2 modules share the same pins for input video. It is, however, possible to feed independent video streams to VIU2 and DCU3 (operating in narrow mode). Figure 5 explains the pin sharing arrangement.
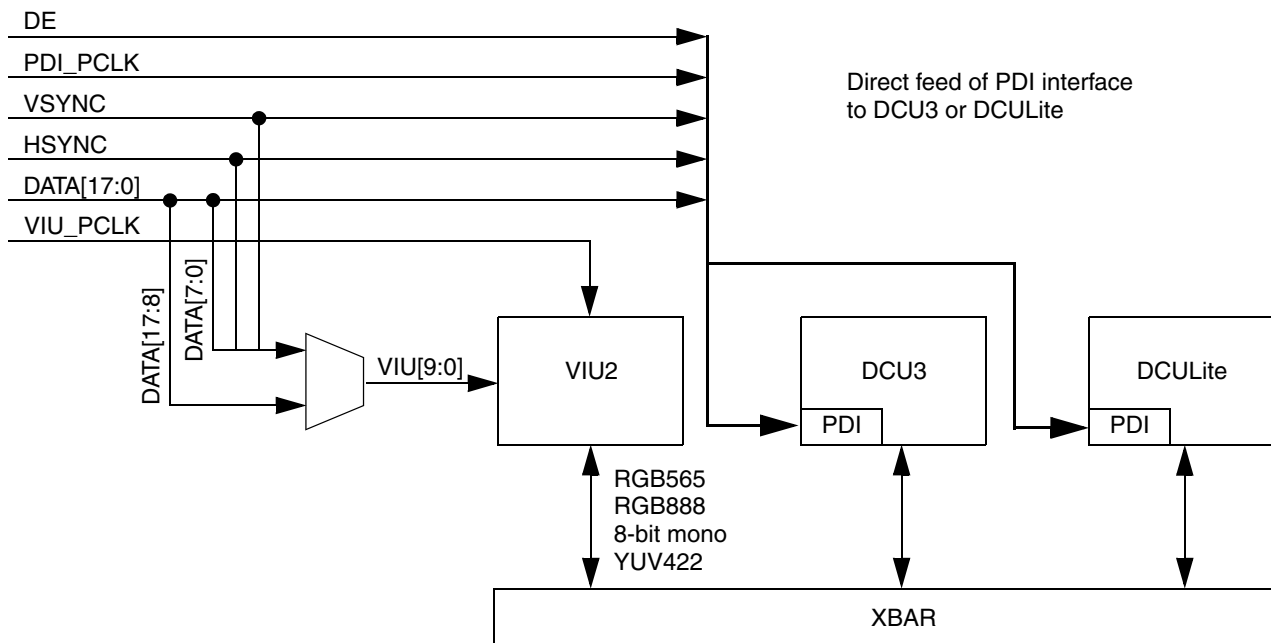
**Figure 5. VIU2, DCU3, and DCULite pin sharing**

VIU input data selection is done based on select bit (bit 0) of Miscellaneous control register (0xC3FE0340).

- VIU pix data: VIU[9:0]
- Select bit 1'b0: PDI[7:0],HSYNC,VSYNC
- Select bit 1'b1: PDI[17:8]

## 2.4.7 SGM muxing

The SGM shares pins between the PWM output signals and the I2S bus signals as shown in the "Port pin summary" table. When the PWM function is enabled in the SGM (SGMCTL[PWME]) the PWM (PWMO, PWMOA) signals are available. When the PWM function is disabled the I2S bus signals (I2S_DO, I2S_SCK) are available.

## 2.4.8 RSDS special function muxing

Ports PA[0:15], PG[0:7], PG[11] and PM[2] have the RSDS signalling option as a special function. The SIUL allocates pad control registers to these functions (PCR[270:282]), but because these pads share a common pin with the normal GPIO pins they do not operate in the same way as the normal GPIO ports. PG[11] in particular has a special configuration separate from the other pads.

The special-function pads are output-only, and the associated PCR[OBE] bit is controlled by the TCON_CTRL1 register (TCON_BYPASS and RSDS_MODE bits). However, the alternate function selection is taken from the associated normal GPIO pad. This allows selection of the DCU3 function as the alternate function of the pad and then the TCON module to select if the output style is TCON/RSDS or digital RGB format.

Therefore, when the TCON bypass is active (bypass disabled with or without RSDS active), it is important not to configure the normal GPIO ports for output operation with a non-DCU3 alternate function on ports PA[0:15] and PG[0:7].

For PG[11], the PCR[282] OBE bit is fully controlled by the TCON module and will become an output whenever the DCU3 alternate option is selected. Therefore, only select the DCU3 function on this pin when ready to configure it as a clock for a TFT panel.

## 2.4.9 Functional ports

The functional port pins are listed in Table 7.

**Table 7. Port pin summary**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PORT A** | | | | | | | | | | | |
| PA[0] | PCR[0] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[0]<br>DCU_R0<br>SDA_1<br>eMIOS0[18] | RSDS0P | SIUL<br>DCU3<br>I²C_1<br>PWM/Timer | I/O | M /<br>RSDS | None,<br>none | 116 | 139 | K26 |
| PA[1] | PCR[1] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[1]<br>DCU_R1<br>SCL_1<br>eMIOS0[17] | RSDS0M | SIUL<br>DCU3<br>I²C_1<br>PWM/Timer | I/O | M /<br>RSDS | None,<br>none | 117 | 140 | K25 |
| PA[2] | PCR[2] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[2]<br>DCU_R2<br>—<br>— | RSDS1P | SIUL<br>DCU3<br>—<br>— | I/O | M /<br>RSDS | None,<br>none | 118 | 141 | K23 |
| PA[3] | PCR[3] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[3]<br>DCU_R3<br>—<br>— | RSDS1M | SIUL<br>DCU3<br>—<br>— | I/O | M /<br>RSDS | None,<br>none | 119 | 142 | J23 |
| PA[4] | PCR[4] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[4]<br>DCU_R4<br>—<br>— | RSDS2P | SIUL<br>DCU3<br>—<br>— | I/O | M /<br>RSDS | None,<br>none | 120 | 143 | J26 |
| PA[5] | PCR[5] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[5]<br>DCU_R5<br>—<br>— | RSDS2M | SIUL<br>DCU3<br>—<br>— | I/O | M /<br>RSDS | None,<br>none | 121 | 144 | J25 |
| PA[6] | PCR[6] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[6]<br>DCU_R6<br>—<br>— | RSDS3P | SIUL<br>DCU3<br>—<br>— | I/O | M /<br>RSDS | None,<br>none | 124 | 148 | H26 |
| PA[7] | PCR[7] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[7]<br>DCU_R7<br>—<br>— | RSDS3M | SIUL<br>DCU3<br>—<br>— | I/O | M /<br>RSDS | None,<br>none | 125 | 149 | G26 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number 176 LQFP | Pin number 208 LQFP | Pin number 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PA[8] | PCR[8] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[8]<br>DCU_G0<br>SCL_2<br>eMIOS0[20] | RSDS4P | SIUL<br>DCU3<br>I2C_2<br>PWM/Timer | I/O | M / RSDS | None, none | 126 | 150 | G25 |
| PA[9] | PCR[9] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[9]<br>DCU_G1<br>SDA_2<br>eMIOS0[19] | RSDS4M | SIUL<br>DCU3<br>I2C_2<br>PWM/Timer | I/O | M / RSDS | None, none | 127 | 151 | G24 |
| PA[10] | PCR[10] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[10]<br>DCU_G2<br>—<br>— | RSDS5P | SIUL<br>DCU3<br>—<br>— | I/O | M / RSDS | None, none | 128 | 152 | H23 |
| PA[11] | PCR[11] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[11]<br>DCU_G3<br>—<br>— | RSDS5M | SIUL<br>DCU3<br>—<br>— | I/O | M / RSDS | None, none | 129 | 153 | G23 |
| PA[12] | PCR[12] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[12]<br>DCU_G4<br>—<br>— | RSDS6P | SIUL<br>DCU3<br>—<br>— | I/O | M / RSDS | None, none | 130 | 154 | F26 |
| PA[13] | PCR[13] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[13]<br>DCU_G5<br>—<br>— | RSDS6M | SIUL<br>DCU3<br>—<br>— | I/O | M / RSDS | None, none | 131 | 155 | F25 |
| PA[14] | PCR[14] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[14]<br>DCU_G6<br>—<br>— | RSDS7P | SIUL<br>DCU3<br>—<br>— | I/O | M / RSDS | None, none | 134 | 158 | F24 |
| PA[15] | PCR[15] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[15]<br>DCU_G7<br>—<br>— | RSDS7M | SIUL<br>DCU3<br>—<br>— | I/O | M / RSDS | None, none | 135 | 159 | F23 |
| **PORT B** | | | | | | | | | | | |
| PB[0] | PCR[16] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[16]<br>CANTX_0<br>TXD_0<br>— | — | SIUL<br>FlexCAN_0<br>LINFlex_0<br>— | I/O | S | None, none | 13 | 13 | W4 |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PB[1] | PCR[17] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[17]<br>CANRX_0<br>RXD_0<br>— | — | SIUL<br>FlexCAN_0<br>LINFlex_0<br>— | I/O | S | None, none | 12 | 12 | V1 |
| PB[2] | PCR[18] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[18]<br>TXD_0<br>—<br>— | — | SIUL<br>LINFlex_0<br>—<br>— | I/O | S | None, none | 153 | 183 | D21 |
| PB[3] | PCR[19] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[19]<br>RXD_0<br>—<br>— | — | SIUL<br>LINFlex_0<br>—<br>— | I/O | S | None, none | 152 | 182 | A22 |
| PB[4] | PCR[20] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[20]<br>SCK_1<br>MA0<br>— | — | SIUL<br>DSPI_1<br>ADC<br>— | I/O | S | None, none | 62 | 74 | AF15 |
| PB[5] | PCR[21] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[21]<br>SOUT_1<br>MA1<br>FABM | — | SIUL<br>DSPI_1<br>ADC<br>Control | I/O | S | Input, pull-down | 63 | 75 | AC16 |
| PB[6] | PCR[22] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[22]<br>SIN_1<br>MA2<br>ABS[0] | — | SIUL<br>DSPI_1<br>ADC<br>Control | I/O | S | Input, pull-up | 64 | 76 | AF16 |
| PB[7] | PCR[23] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[23]<br>SIN_0<br>eMIOS1[20]<br>I2S_SCK/PWMO | — | SIUL<br>DSPI_0<br>PWM/Timer<br>SGM | I/O | S | None, none | 55 | 67 | AC14 |
| PB[8] | PCR[24] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[24]<br>SOUT_0<br>eMIOS1[19]<br>I2S_DO/PWMOA | — | SIUL<br>DSPI_0<br>PWM/Timer<br>SGM | I/O | S | None, none | 54 | 66 | AF13 |
| PB[9] | PCR[25] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[25]<br>SCK_0<br>eMIOS1[18]<br>I2S_FS | — | SIUL<br>DSPI_0<br>PWM/Timer<br>SGM | I/O | M | None, none | 53 | 65 | AC13 |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PB[10] | PCR[26] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[26]<br>CANRX_1<br>I2S_DO/PWMOA<br>— | — | SIUL<br>FlexCAN_1<br>SGM<br>— | I/O | S | None, none | 14 | 14 | W2 |
| PB[11] | PCR[27] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[27]<br>CANTX_1<br>SGM_MCLK<br>— | — | SIUL<br>FlexCAN_1<br>SGM<br>— | I/O | S | None, none | 15 | 15 | Y4 |
| PB[12] | PCR[28] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[28]<br>RXD_1<br>eMIOS1[10]<br>CS2_0 | — | SIUL<br>LINFlex_1<br>PWM/Timer<br>DSPI_0 | I/O | S | None, none | 46 | 54 | AF7 |
| PB[13] | PCR[29] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[29]<br>TXD_1<br>eMIOS1[11]<br>CS1_0 | — | SIUL<br>LINFlex_1<br>PWM/Timer<br>DSPI_0 | I/O | S | None, none | 47 | 55 | AC8 |
| PB[14] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PB[15] | — | — | Reserved | — | — | — | — | — | — | — | — |
| **PORT C** | | | | | | | | | | | |
| PC[0] | PCR[30] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[30]<br>—<br>—<br>— | ANS[0] | SIUL<br>—<br>—<br>— | I/O | J | None, none | 88 | 104 | AC21 |
| PC[1] | PCR[31] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[31]<br>—<br>—<br>— | ANS[1] | SIUL<br>—<br>—<br>— | I/O | J | None, none | 87 | 103 | AC25 |
| PC[2] | PCR[32] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[32]<br>—<br>—<br>— | ANS[2] | SIUL<br>—<br>—<br>— | I/O | J | None, none | 86 | 102 | AC26 |
| PC[3] | PCR[33] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[33]<br>—<br>—<br>— | ANS[3] | SIUL<br>—<br>—<br>— | I/O | J | None, none | 85 | 101 | AC24 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PC[4] | PCR[34] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[34]<br>—<br>—<br>— | ANS[4] | SIUL<br>—<br>—<br>— | I/O | J | None,<br>none | 84 | 100 | AD24 |
| PC[5] | PCR[35] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[35]<br>—<br>—<br>— | ANS[5] | SIUL<br>—<br>—<br>— | I/O | J | None,<br>none | 83 | 99 | AD26 |
| PC[6] | PCR[36] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[36]<br>—<br>—<br>— | ANS[6] | SIUL<br>—<br>—<br>— | I/O | J | None,<br>none | 82 | 98 | AD21 |
| PC[7] | PCR[37] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[37]<br>—<br>—<br>— | ANS[7] | SIUL<br>—<br>—<br>— | I/O | J | None,<br>none | 81 | 97 | AD25 |
| PC[8] | PCR[38] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[38]<br>—<br>—<br>— | ANS[8] | SIUL<br>—<br>—<br>— | I/O | J | None,<br>none | 76 | 92 | AE26 |
| PC[9] | PCR[39] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[39]<br>—<br>—<br>— | ANS[9] | SIUL<br>—<br>—<br>— | I/O | J | None,<br>none | 75 | 91 | AE25 |
| PC[10] | PCR[40] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[40]<br>—<br>I2S_DO/PWMO<br>— | ANS[10] | SIUL<br>—<br>SGM<br>— | I/O | J | None,<br>none | 74 | 90 | AE23 |
| PC[11] | PCR[41] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[41]<br>—<br>MA0<br>CS2_1 | ANS[11] | SIUL<br>—<br>ADC<br>DSPI_1 | I/O | J | None,<br>None | 73 | 89 | AE24 |
| PC[12] | PCR[42] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[42]<br>—<br>MA1<br>CS1_1 | ANS[12] | SIUL<br>—<br>ADC<br>DSPI_1 | I/O | J | None,<br>None | 72 | 88 | AF26 |

*Pin number* (spanning 176 LQFP / 208 LQFP / 416 TEPBGA columns)

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number 176 LQFP | Pin number 208 LQFP | Pin number 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PC[13] | PCR[43] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[43]<br>—<br>MA2<br>CS0_1 | ANS[13] | SIUL<br>—<br>ADC<br>DSPI_1 | I/O | J | None,<br>None | 71 | 87 | AF25 |
| PC[14] | PCR[44] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[44]<br>—<br>—<br>— | ANS[14]<br>EXTAL32 | SIUL<br>—<br>—<br>— | I/O | J | None,<br>None | 70 | 86 | AF24 |
| PC[15] | PCR[45] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[45]<br>—<br>—<br>— | ANS[15]<br>XTAL32 | SIUL<br>—<br>—<br>— | I/O | J | None,<br>None | 69 | 85 | AF23 |
| **PORT D** | | | | | | | | | | | |
| PD[0] | PCR[46] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[46]<br>M0C0M<br>SSD0_0<br>eMIOS1[8] | — | SIUL<br>SMD<br>SSD<br>PWM/Timer | I/O | SMD | None,<br>None | 90 | 106 | AB26 |
| PD[1] | PCR[47] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[47]<br>M0C0P<br>SSD0_1<br>eMIOS1[16] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None,<br>None | 91 | 107 | AB25 |
| PD[2] | PCR[48] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[48]<br>M0C1M<br>SSD0_2<br>eMIOS1[23] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None,<br>None | 92 | 108 | AB24 |
| PD[3] | PCR[49] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[49]<br>M0C1P<br>SSD0_3<br>eMIOS0[9] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None,<br>None | 93 | 109 | AB23 |
| PD[4] | PCR[50] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[50]<br>M1C0M<br>SSD1_0<br>eMIOS0[8] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None,<br>None | 96 | 112 | AA26 |
| PD[5] | PCR[51] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[51]<br>M1C0P<br>SSD1_1<br>eMIOS0[16] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None,<br>None | 97 | 113 | AA23 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number 176 LQFP | Pin number 208 LQFP | Pin number 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PD[6] | PCR[52] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[52]<br>M1C1M<br>SSD1_2<br>eMIOS0[23] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 98 | 114 | Y26 |
| PD[7] | PCR[53] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[53]<br>M1C1P<br>SSD1_3<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | 99 | 115 | Y25 |
| PD[8] | PCR[54] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[54]<br>M2C0M<br>SSD2_0<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | 100 | 116 | Y24 |
| PD[9] | PCR[55] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[55]<br>M2C0P<br>SSD2_1<br>eMIOS0[9] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 101 | 117 | Y23 |
| PD[10] | PCR[56] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[56]<br>M2C1M<br>SSD2_2<br>eMIOS0[10] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 102 | 118 | W26 |
| PD[11] | PCR[57] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[57]<br>M2C1P<br>SSD2_3<br>eMIOS0[11] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 103 | 119 | W23 |
| PD[12] | PCR[58] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[58]<br>M3C0M<br>SSD3_0<br>eMIOS0[12] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 106 | 122 | V26 |
| PD[13] | PCR[59] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[59]<br>M3C0P<br>SSD3_1<br>eMIOS0[13] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 107 | 123 | V25 |
| PD[14] | PCR[60] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[60]<br>M3C1M<br>SSD3_2<br>eMIOS0[14] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 108 | 124 | V24 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PD[15] | PCR[61] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[61]<br>M3C1P<br>SSD3_3<br>eMIOS0[15] | — | SIUL<br>SMC<br>SSD<br>PWM/Timer | I/O | SMD | None, None | 109 | 125 | V23 |
| **PORT E** | | | | | | | | | | | |
| PE[0] | PCR[62] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[62]<br>M4C0M<br>SSD4_0<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 126 | U26 |
| PE[1] | PCR[63] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[63]<br>M4C0P<br>SSD4_1<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 127 | U23 |
| PE[2] | PCR[64] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[64]<br>M4C1M<br>SSD4_2<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 128 | T26 |
| PE[3] | PCR[65] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[65]<br>M4C1P<br>SSD4_3<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 129 | T25 |
| PE[4] | PCR[66] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[66]<br>M5C0M<br>SSD5_0<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 132 | T24 |
| PE[5] | PCR[67] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[67]<br>M5C0P<br>SSD5_1<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 133 | T23 |
| PE[6] | PCR[68] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[68]<br>M5C1M<br>SSD5_2<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 134 | R24 |
| PE[7] | PCR[69] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[69]<br>M5C1P<br>SSD5_3<br>— | — | SIUL<br>SMC<br>SSD<br>— | I/O | SMD | None, None | — | 135 | R23 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 176 LQFP | 208 LQFP | 416 TEPBGA |
| **PORT F** | | | | | | | | | | | | |
| PF[0] | PCR[70] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[70]<br>eMIOS1[19]<br>EVTO<br>DCULITE_B2 | — | SIUL<br>PWM/Timer<br>NEXUS<br>DCULite | I/O | M | None,<br>None | 157 | 189 | C20 |
| PF[1] | PCR[71] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[71]<br>eMIOS1[20]<br>MSEO<br>DCULITE_B3 | — | SIUL<br>PWM/Timer<br>NEXUS<br>DCULite | I/O | M | None,<br>None | 158 | 190 | B20 |
| PF[2] | PCR[72] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[72]<br>NMI<br>—<br>— | — | SIUL<br>NMI<br>—<br>— | I/O | S | None,<br>None | 45 | 53 | AC7 |
| PF[3] | PCR[73] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[73]<br>eMIOS1[21]<br>MSEO<br>DCULITE_B4 | — | SIUL<br>PWM/Timer<br>NEXUS<br>DCULite | I/O | M | None,<br>None | 159 | 191 | A20 |
| PF[4] | PCR[74] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[74]<br>eMIOS1[14]<br>SDA_1<br>DCULITE_B5 | — | SIUL<br>PWM/Timer<br>$I^2C$_1<br>DCULite | I/O | M | None,<br>None | 160 | 192 | D19 |
| PF[5] | PCR[75] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[75]<br>QUADSPI_IO1_B<br>eMIOS1[15]<br>VIU8_PDI16 | — | SIUL<br>QuadSPI<br>PWM/Timer<br>VIU2/PDI | I/O | M | None,<br>None | 161 | 193 | A19 |
| PF[6] | PCR[76] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[76]<br>QUADSPI_IO0_B<br>eMIOS1[16]<br>VIU9_PDI17 | — | SIUL<br>QuadSPI<br>PWM/Timer<br>VIU2/PDI | I/O | M | None,<br>None | 162 | 194 | D18 |
| PF[7] | PCR[77] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[77]<br>eMIOS1[15]<br>SCL_1<br>DCULITE_B6 | — | SIUL<br>PWM/Timer<br>$I^2C$_1<br>DCULite | I/O | M | None,<br>None | 163 | 195 | C18 |
| PF[8] | PCR[78] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[78]<br>SDA_0<br>CS2_1<br>RXD_1 | — | SIUL<br>$I^2C$_0<br>DSPI_1<br>LINFlex_1 | I/O | S | None,<br>None | 164 | 196 | A18 |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PF[9] | PCR[79] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[79]<br>SCL_0<br>CS1_1<br>TXD_1 | — | SIUL<br>$I^2C$_0<br>DSPI_1<br>LINFlex_1 | I/O | S | None,<br>None | 165 | 197 | D17 |
| PF[10] | PCR[80] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[80]<br>QUADSPI_PCS_A<br>—<br>EVTI | — | SIUL<br>QuadSPI<br>—<br>NEXUS | I/O | M | None,<br>None | 169 | 201 | A17 |
| PF[11] | PCR[81] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[81]<br>QUADSPI_IO2_A<br>—<br>MDO0 | — | SIUL<br>QuadSPI<br>—<br>NEXUS | I/O | M | None,<br>None | 170 | 202 | D16 |
| PF[12] | PCR[82] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[82]<br>QUADSPI_IO3_A<br>—<br>MDO1 | — | SIUL<br>QuadSPI<br>—<br>NEXUS | I/O | M | None,<br>None | 171 | 203 | C16 |
| PF[13] | PCR[83] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[83]<br>QUADSPI_IO0_A<br>—<br>MDO2 | — | SIUL<br>QuadSPI<br>—<br>NEXUS | I/O | M | None,<br>None | 172 | 204 | B16 |
| PF[14] | PCR[84] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[84]<br>QUADSPI_IO1_A<br>—<br>MDO3 | — | SIUL<br>QuadSPI<br>—<br>NEXUS | I/O | M | None,<br>None | 173 | 205 | A16 |
| PF[15] | PCR[85] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[85]<br>QUADSPI_CLK_A<br>CLKOUT<br>MCKO | — | SIUL<br>QuadSPI<br>Control<br>NEXUS | I/O | F | None,<br>None | 174 | 206 | B18 |
| **PORT G** | | | | | | | | | | | |
| PG[0] | PCR[86] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[86]<br>DCU_B0<br>SCL_3<br>eMIOS0[21] | RSDS8P | SIUL<br>DCU3<br>$I^2C$_3<br>PWM/Timer | I/O | M | None,<br>None | 136 | 160 | E26 |
| PG[1] | PCR[87] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[87]<br>DCU_B1<br>SDA_3<br>eMIOS0[22] | RSDS8M | SIUL<br>DCU3<br>$I^2C$_3<br>PWM/Timer | I/O | M | None,<br>None | 137 | 161 | D26 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PG[2] | PCR[88] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[88]<br>DCU_B2<br>—<br>— | RSDS9P | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 141 | 166 | D25 |
| PG[3] | PCR[89] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[89]<br>DCU_B3<br>—<br>— | RSDS9M | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 142 | 167 | C25 |
| PG[4] | PCR[90] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[90]<br>DCU_B4<br>—<br>— | RSDS10P | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 143 | 168 | C26 |
| PG[5] | PCR[91] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[91]<br>DCU_B5<br>—<br>— | RSDS10M | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 144 | 169 | B26 |
| PG[6] | PCR[92] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[92]<br>DCU_B6<br>—<br>— | RSDS11P | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 145 | 170 | A26 |
| PG[7] | PCR[93] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[93]<br>DCU_B7<br>—<br>— | RSDS11M | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 146 | 171 | A25 |
| PG[8] | PCR[94] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[94]<br>DCU_VSYNC<br>—<br>— | — | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 1 | 1 | T4 |
| PG[9] | PCR[95] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[95]<br>DCU_HSYNC<br>—<br>— | — | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 2 | 2 | T2 |
| PG[10] | PCR[96] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[96]<br>DCU_DE<br>—<br>— | — | SIUL<br>DCU3<br>—<br>— | I/O | M | None,<br>None | 3 | 3 | T1 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PG[11] | PCR[97] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[97]<br>DCU_PCLK<br>—<br>— | RSDSCLKP | SIUL<br>DCU3<br>—<br>— | I/O | F | None,<br>None | 147 | 172 | E23 |
| PG[12] | PCR[98] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[98]<br>CS0_1<br>PDI_DE<br>DCULITE_B7 | — | SIUL<br>DSPI_1<br>PDI<br>DCULite | I/O | M | None,<br>None | 168 | 200 | A15 |
| PG[13] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PG[14] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PG[15] | — | — | Reserved | — | — | — | — | — | — | — | — |
| **PORT H** | | | | | | | | | | | |
| PH[0][6] | PCR[99] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[99]<br>TCK<br>—<br>— | — | SIUL<br>JTAG<br>—<br>— | I/O | S | Input,<br>Pull Up | 41 | 49 | AC6 |
| PH[1][6] | PCR[100] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[100]<br>TDI<br>—<br>— | — | SIUL<br>JTAG<br>—<br>— | I/O | S | Input,<br>Pull Up | 42 | 50 | AD6 |
| PH[2][6] | PCR[101] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[101]<br>TDO<br>—<br>— | — | SIUL<br>JTAG<br>—<br>— | I/O | M | Output,<br>None | 43 | 51 | AE6 |
| PH[3][6] | PCR[102] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[102]<br>TMS<br>—<br>— | — | SIUL<br>JTAG<br>—<br>— | I/O | S | Input,<br>Pull Up | 44 | 52 | AF6 |
| PH[4] | PCR[103] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[103]<br>CS0_0<br>eMIOS1[21]<br>DCULITE_G6 | — | SIUL<br>DSPI_0<br>PWM/Timer<br>DCULite | I/O | M | None,<br>None | 61 | 73 | AE15 |
| PH[5] | PCR[104] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[104]<br>VIU7_PDI15<br>I2S_FS<br>eMIOS1[8] | — | SIUL<br>VIU2/PDI<br>SGM<br>PWM/Timer | I/O | S | None,<br>None | 38 | — | — |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PH[6] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[7] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[8] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[9] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[10] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[11] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[12] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[13] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[14] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PH[15] | — | — | Reserved | — | — | — | — | — | — | — | — |
| **PORT J** | | | | | | | | | | | |
| PJ[0] | PCR[105] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[105]<br>DCULITE_B6<br>—<br>I2S_DO / PWMO | — | SIUL<br>DCULite<br>—<br>SGM | I/O | M | None,<br>None | — | — | L26 |
| PJ[1] | PCR[106] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[106]<br>VIU1_PDI_HSYNC<br>eMIOS1[9]<br>eMIOS0[8] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 4 | 4 | U4 |
| PJ[2] | PCR[107] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[107]<br>VIU0_PDI_VSYNC<br>eMIOS1[14]<br>eMIOS0[9] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 5 | 5 | U3 |
| PJ[3] | PCR[108] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[108]<br>VIU_PCLK<br>eMIOS0[22]<br>PDI_DE | — | SIUL<br>VIU2<br>PWM/Timer<br>PDI | I/O | S | None,<br>None | 60 | 72 | AD15 |
| PJ[4] | PCR[109] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[109]<br>VIU2_PDI0<br>eMIOS0[21]<br>eMIOS0[23] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 56 | 68 | AD14 |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number 176 LQFP | Pin number 208 LQFP | Pin number 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PJ[5] | PCR[110] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[110]<br>VIU3_PDI1<br>eMIOS0[20]<br>eMIOS0[16] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | M | None,<br>None | 57 | 69 | AE14 |
| PJ[6] | PCR[111] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[111]<br>VIU4_PDI2<br>eMIOS0[19]<br>eMIOS0[15] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 58 | 70 | AF14 |
| PJ[7] | PCR[112] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[112]<br>VIU5_PDI3<br>eMIOS0[18]<br>eMIOS0[14] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 59 | 71 | AC15 |
| PJ[8] | PCR[113] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[113]<br>VIU6_PDI4<br>eMIOS0[17]<br>eMIOS0[13] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 8 | 8 | U2 |
| PJ[9] | PCR[114] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[114]<br>VIU7_PDI5<br>eMIOS1[22]<br>eMIOS0[12] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 9 | 9 | U1 |
| PJ[10] | PCR[115] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[115]<br>VIU8_PDI6<br>eMIOS1[17]<br>eMIOS0[11] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 10 | 10 | V4 |
| PJ[11] | PCR[116] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[116]<br>VIU9_PDI7<br>eMIOS1[15]<br>eMIOS0[10] | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>PWM/Timer | I/O | S | None,<br>None | 11 | 11 | V3 |
| PJ[12] | PCR[117] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[117]<br>DCU_TAG<br>—<br>DCULITE_G6 | — | SIUL<br>DCU3<br>—<br>DCULite | I/O | M | None,<br>None | 148 | 178 | A23 |
| PJ[13] | PCR[118] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[118]<br>QUADSPI_PCS_B<br>eMIOS1[8]<br>VIU5_PDI13 | — | SIUL<br>QuadSPI<br>PWM/Timer<br>VIU2/PDI | I/O | M | None,<br>None | 149 | 179 | D22 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 176 LQFP | 208 LQFP | 416 TEPBGA |
| PJ[14] | PCR[119] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[119]<br>QUADSPI_CLK_B<br>eMIOS1[17]<br>PDI_PCLK | — | SIUL<br>QuadSPI<br>PWM/Timer<br>PDI | I/O | F | None,<br>None | 150 | 180 | C22 |
| PJ[15] | PCR[120] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[120]<br>QUADSPI_IO3_B<br>eMIOS1[9]<br>VIU6_PDI14 | — | SIUL<br>QuadSPI<br>PWM/Timer<br>VIU2/PDI | I/O | M | None,<br>None | 151 | 181 | B22 |
| **PORT K** | | | | | | | | | | | | |
| PK[0] | PCR[121] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[121]<br>eMIOS1[18]]<br>—<br>DCULITE_G7 | — | SIUL<br>PWM/Timer<br>—<br>DCULite | I/O | M | None,<br>None | 155 | 187 | A21 |
| PK[1] | PCR[122] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[122]<br>QUADSPI_IO2_B<br>eMIOS1[14]<br>VIU7_PDI15 | — | SIUL<br>QuadSPI<br>PWM/Timer<br>VIU2/PDI | I/O | M | None,<br>None | 156 | 188 | D20 |
| PK[2] | PCR[123] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[123]<br>VIU0_PDI8<br>eMIOS1[10]<br>DCULITE_TAG | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>DCULite | I/O | M | None,<br>None | 31 | 39 | AE3 |
| PK[3] | PCR[124] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[124]<br>VIU1_PDI9<br>eMIOS1[11]<br>DCULITE_DE | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>DCULite | I/O | M | None,<br>None | 32 | 40 | AF3 |
| PK[4] | PCR[125] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[125]<br>VIU2_PDI10<br>eMIOS1[12]<br>DCULITE_HSYNC | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>DCULite | I/O | M | None,<br>None | 33 | 41 | AC4 |
| PK[5] | PCR[126] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[126]<br>VIU3_PDI11<br>eMIOS1[13]<br>DCULITE_VSYNC | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>DCULite | I/O | M | None,<br>None | 34 | 42 | AF4 |
| PK[6] | PCR[127] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[127]<br>VIU4_PDI12<br>eMIOS1[9]<br>DCULITE_PCLK | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>DCULite | I/O | F | None,<br>None | 35 | 43 | AC5 |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PK[7] | PCR[128] | Option 0 / Option 1 / Option 2 / Option 3 | GPIO[128] / RXD_2 / DCULITE_R2 / TCON[8] | — | SIUL / LINFlex_2 / DCULite / TCON | I/O | M | None, None | — | 44 | AD5 |
| PK[8] | PCR[129] | Option 0 / Option 1 / Option 2 / Option 3 | GPIO[129] / TXD_2 / DCULITE_R3 / TCON[9] | — | SIUL / LINFlex_2 / DCULite / TCON | I/O | M | None, None | — | 45 | AE5 |
| PK[9] | PCR[130] | Option 0 / Option 1 / Option 2 / Option 3 | GPIO[130] / I2S_DO / PWMO / DCULITE_R4 / TCON[10] | — | SIUL / SGM / DCULite / TCON | I/O | M | None, None | — | 46 | AF5 |
| PK[10] | PCR[131] | Option 0 / Option 1 / Option 2 / Option 3 | GPIO[131] / SDA_1 / eMIOS1[12] / DCULITE_TAG | — | SIUL / I2C_1 / PWM/Timer / DCULite | I/O | S | None, None | 51 | 59 | AF8 |
| PK[11] | PCR[132] | Option 0 / Option 1 / Option 2 / Option 3 | GPIO[132] / SCL_1 / eMIOS1[13] / DCU_TAG | — | SIUL / I2C_1 / PWM/Timer / DCU3 | I/O | S | None, None | 52 | 60 | AC9 |
| PK[12] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PK[13] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PK[14] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PK[15] | — | — | Reserved | — | — | — | — | — | — | — | — |
| **PORT L** | | | | | | | | | | | |
| PL[0] | PCR[133] | Option 0 / Option 1 / Option 2 / Option 3 | GPIO[133] / — / CANRX_1 / SDA_1 | ANS[19] | SIUL / — / FlexCAN_1 / I2C1 | I/O | M / ANALOG | None, None | — | 81 | AE22 |
| PL[1] | PCR[134] | Option 0 / Option 1 / Option 2 / Option 3 | GPIO[134] / — / CANTX_1 / SCL_1 | ANS[18] | SIUL / — / FlexCAN_1 / I2C1 | I/O | M / ANALOG | None, None | — | 82 | AE21 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PL[2] | PCR[135] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[135]<br>—<br>CANRX_0<br>eMIOS1[22] | ANS[17] | SIUL<br>—<br>FlexCAN_0<br>PWM/Timer | I/O | S / ANALOG | None, None | — | 83 | AF22 |
| PL[3] | PCR[136] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[136]<br>—<br>CANTX_0<br>eMIOS1[23] | ANS[16] | SIUL<br>—<br>FlexCAN_0<br>PWM/Timer | I/O | S / ANALOG | None, None | — | 84 | AF21 |
| PL[4] | PCR[137] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[137]<br>CS2_2<br>VIU5_PDI13<br>TCON[6] | — | SIUL<br>DSPI_2<br>VIU2/PDI<br>TCON | I/O | M | None, None | — | 31 | AB2 |
| PL[5] | PCR[138] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[138]<br>CS1_2<br>VIU6_PDI14<br>TCON[7] | — | SIUL<br>DSPI_2<br>VIU2/PDI<br>TCON | I/O | M | None, None | — | 32 | AC2 |
| PL[6] | PCR[139] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[139]<br>CS0_2<br>VIU7_PDI15<br>eMIOS1[18] | — | SIUL<br>DSPI_2<br>VIU2/PDI<br>PWM/Timer | I/O | S | None, None | — | 33 | AD1 |
| PL[7] | PCR[140] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[140]<br>SIN_2<br>VIU8_PDI16<br>eMIOS1[19] | — | SIUL<br>DSPI_2<br>VIU2/PDI<br>PWM/Timer | I/O | S | None, None | — | 34 | AE1 |
| PL[8] | PCR[141] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[141]<br>SOUT_2<br>VIU9_PDI17<br>eMIOS1[20] | — | SIUL<br>DSPI_2<br>VIU2/PDI<br>PWM/Timer | I/O | S | None, None | — | 35 | AF1 |
| PL[9] | PCR[142] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[142]<br>SCK_2<br>PDI_PCLK<br>eMIOS1[21] | — | SIUL<br>DSPI_2<br>PDI<br>PWM/Timer | I/O | S | None, None | — | 36 | AF2 |
| PL[10] | PCR[143] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[143]<br>eMIOS1[10]<br>DCULITE_G2<br>— | — | SIUL<br>PWM/Timer<br>DCULite<br>— | I/O | M | None, None | — | 174 | C24 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PL[11] | PCR[144] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[144]<br>eMIOS1[11]<br>DCULITE_G3<br>— | — | SIUL<br>PWM/Timer<br>DCULite<br>— | I/O | M | None,<br>None | — | 175 | A24 |
| PL[12] | PCR[145] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[145]<br>eMIOS1[12]<br>DCULITE_G4<br>— | — | SIUL<br>PWM/Timer<br>DCULite<br>— | I/O | M | None,<br>None | — | 176 | C23 |
| PL[13] | PCR[146] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[146]<br>eMIOS1[13]<br>DCULITE_G5<br>— | — | SIUL<br>PWM/Timer<br>DCULite<br>— | I/O | M | None,<br>None | — | 177 | B23 |
| PL[14] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PL[15] | — | — | Reserved | — | — | — | — | — | — | — | — |
| **PORT M** | | | | | | | | | | | |
| PM[0] | PCR[147] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[147]<br>I2S_SCK / PWMO<br>DCULITE_R5<br>TCON[11] | — | SIUL<br>SGM<br>DCULite<br>TCON | I/O | M | None,<br>None | — | 61 | AE9 |
| PM[1] | PCR[148] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[148]<br>I2S_FS<br>DCULITE_R6<br>— | — | SIUL<br>SGM<br>DCULite<br>— | I/O | M | None,<br>None | — | 62 | AF9 |
| PM[2] | PCR[149] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[149]<br>eMIOS1[17]<br>DCULITE_R7<br>DCULITE_DE | RSDSCLKM | SIUL<br>PWM/Timer<br>DCULite<br>DCULite | I/O | M | None,<br>None | — | 173 | D23 |
| PM[3] | PCR[150] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[150]<br>CANRX_2<br>RXD_3<br>TCON[4] | — | SIUL<br>FlexCAN_2<br>LINFlex_3<br>TCON | I/O | M | None,<br>None | — | 16 | Y3 |
| PM[4] | PCR[151] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[151]<br>CANTX_2<br>TXD_3<br>TCON[5] | — | SIUL<br>FlexCAN_2<br>LINFlex_3<br>TCON | I/O | M | None,<br>None | — | 17 | Y2 |

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**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PM[5] | PCR[152] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[152]<br>VIU5_PDI13<br>eMIOS1[22]<br>DCU_TAG | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>DCU3 | I/O | M | None, None | 16 | — | — |
| PM[6] | PCR[153] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[153]<br>VIU6_PDI14<br>eMIOS1[23]<br>DCULITE_TAG | — | SIUL<br>VIU2/PDI<br>PWM/Timer<br>DCULite | I/O | M | None, None | 17 | — | — |
| PM[7] | PCR[154] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[154]<br>VIU8_PDI16<br>I2S_DO / PWMOA<br>eMIOS1[16] | — | SIUL<br>VIU2/PDI<br>SGM<br>PWM/Timer | I/O | S | None, None | 39 | — | — |
| PM[8] | PCR[155] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[155]<br>VIU9_PDI17<br>I2S_SCK / PWMO<br>eMIOS1[23] | — | SIUL<br>VIU2/PDI<br>SGM<br>PWM/Timer | I/O | S | None, None | 40 | — | — |
| PM[9] | PCR[156] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[156]<br>PDI_PCLK<br>SGM_MCLK<br>eMIOS0[8] | — | SIUL<br>PDI<br>SGM<br>PWM/Timer | I/O | M | None, None | 113 | — | — |
| PM[10] | PCR[157] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[157]<br>RXD_2<br>CANRX_2<br>eMIOS0[16] | — | SIUL<br>LINFlex_2<br>FlexCAN_2<br>PWM/Timer | I/O | S | None, None | 114 | — | — |
| PM[11] | PCR[158] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[158]<br>TXD_2<br>CANTX_2<br>eMIOS0[23] | — | SIUL<br>LINFlex_2<br>FlexCAN_2<br>PWM/Timer | I/O | S | None, None | 115 | — | — |
| PM[12] | PCR[159] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[159]<br>DCULITE_B7<br>—<br>I2S_SCK / PWMO | — | SIUL<br>DCULite<br>—<br>SGM | I/O | M | None, None | — | — | L24 |
| PM[13] | PCR[160] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[160]<br>DCULITE_PCLK<br>—<br>SGM_MCLK | — | SIUL<br>DCULite<br>—<br>SGM | I/O | F | None, None | — | — | L23 |
| PM[14] | — | — | Reserved | — | — | — | — | — | — | — | — |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | Pin number | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 176 LQFP | 208 LQFP | 416 TEPBGA | |
| PM[15] | — | — | | Reserved | — | — | — | — | — | — | — | — | |
| **PORT N** | | | | | | | | | | | | | |
| PN[0] | PCR[161] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[161]<br>DCULITE_HSYNC<br>—<br>TCON[4] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None,<br>None | — | — | AC3 | |
| PN[1] | PCR[162] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[162]<br>DCULITE_VSYNC<br>—<br>TCON[5] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None,<br>None | — | — | AD3 | |
| PN[2] | PCR[163] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[163]<br>DCULITE_R0<br>RXD_2<br>VIU0_PDI8 | — | SIUL<br>DCULite<br>LINFlex_2<br>VIU2/PDI | I/O | M | None,<br>None | — | — | AC10 | |
| PN[3] | PCR[164] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[164]<br>DCULITE_R1<br>TXD_2<br>VIU1_PDI9 | — | SIUL<br>DCULite<br>LINFlex_2<br>VIU2/PDI | I/O | M | None,<br>None | — | — | AF10 | |
| PN[4] | PCR[165] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[165]<br>DCULITE_R2<br>—<br>TCON[6] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None,<br>None | — | — | AC11 | |
| PN[5] | PCR[166] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[166]<br>DCULITE_R3<br>—<br>TCON[7] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None,<br>None | — | — | AD11 | |
| PN[6] | PCR[167] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[167]<br>DCULITE_R4<br>—<br>TCON[8] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None,<br>None | — | — | AE11 | |
| PN[7] | PCR[168] | Option 0<br>Option 1<br>Option 2<br>Option 3 | | GPIO[168]<br>DCULITE_R5<br>—<br>TCON[9] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None,<br>None | — | — | AF11 | |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PN[8] | PCR[169] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[169]<br>DCULITE_R6<br>—<br>TCON[10] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None, None | — | — | AC12 |
| PN[9] | PCR[170] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[170]<br>DCULITE_R7<br>—<br>TCON[11] | — | SIUL<br>DCULite<br>—<br>TCON | I/O | M | None, None | — | — | AD12 |
| PN[10] | PCR[171] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[171]<br>DCULITE_G0<br>RXD_3<br>VIU2_PDI10 | — | SIUL<br>DCULite<br>LINFlex_3<br>VIU2/PDI | I/O | M | None, None | — | — | AE12 |
| PN[11] | PCR[172] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[172]<br>DCULITE_G1<br>TXD_3<br>VIU3_PDI11 | — | SIUL<br>DCULite<br>LINFlex_3<br>VIU2/PDI | I/O | M | None, None | — | — | AF12 |
| PN[12] | PCR[173] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[173]<br>DCULITE_G2<br>—<br>eMIOS0[17] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None, None | — | — | R26 |
| PN[13] | PCR[174] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[174]<br>DCULITE_G3<br>—<br>eMIOS0[18] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None, None | — | — | R25 |
| PN[14] | PCR[175] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[175]<br>DCULITE_G4<br>—<br>eMIOS0[19] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None, None | — | — | P26 |
| PN[15] | PCR[176] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[176]<br>DCULITE_G5<br>—<br>eMIOS0[20] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None, None | — | — | P24 |
| **PORT P** | | | | | | | | | | | |
| PP[0] | PCR[177] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[177]<br>DCULITE_G6<br>—<br>eMIOS0[21] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None, None | — | — | P23 |

**Table 7. Port pin summary (continued)**

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PP[1] | PCR[178] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[178]<br>DCULITE_G7<br>—<br>eMIOS0[22] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None,<br>None | — | — | N26 |
| PP[2] | PCR[179] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[179]<br>DCULITE_B0<br>CANRX_2<br>VIU4_PDI12 | — | SIUL<br>DCULite<br>FlexCAN_2<br>VIU2/PDI | I/O | M | None,<br>None | — | — | N25 |
| PP[3] | PCR[180] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[180]<br>DCULITE_B1<br>CANTX_2<br>PDI_DE | — | SIUL<br>DCULite<br>FlexCAN_2<br>PDI | I/O | M | None,<br>None | — | — | N23 |
| PP[4] | PCR[181] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[181]<br>DCULITE_B2<br>—<br>eMIOS0[11] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None,<br>None | — | — | M26 |
| PP[5] | PCR[182] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[182]<br>DCULITE_B3<br>—<br>eMIOS0[13] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None,<br>None | — | — | M25 |
| PP[6] | PCR[183] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[183]<br>DCULITE_B4<br>—<br>eMIOS0[15] | — | SIUL<br>DCULite<br>—<br>PWM/Timer | I/O | M | None,<br>None | — | — | M24 |
| PP[7] | PCR[184] | Option 0<br>Option 1<br>Option 2<br>Option 3 | GPIO[184]<br>DCULITE_B5<br>—<br>I2S_FS | — | SIUL<br>DCULite<br>—<br>SGM | I/O | M | None,<br>None | — | — | M23 |
| PP[8] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PP[9] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PP[10] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PP[11] | — | — | Reserved | — | — | — | — | — | — | — | — |

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## Table 7. Port pin summary (continued)

| Port pin | PCR | Alternate function[1] | Function | Special function[2] | Peripheral[3] | I/O direction | Pad Type[4] | RESET config[5] | 176 LQFP | 208 LQFP | 416 TEPBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PP[12] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PP[13] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PP[14] | — | — | Reserved | — | — | — | — | — | — | — | — |
| PP[15] | — | — | Reserved | — | — | — | — | — | — | — | — |

(Pin number columns: 176 LQFP, 208 LQFP, 416 TEPBGA)

1  Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIUL module.
PCR[PA] = 00 selects Option 0
PCR[PA] = 01 selects Option 1
PCR[PA] = 10 selects Option 2
PCR[PA] = 11 selects Option 3
This is intended to select the output functions. To use one of the input functions, the PCR[IBE] bit must be written to '1', regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2  Special functions are enabled independently from the standard digital pin functions. Enabling standard I/O functions in the PCR registers may interfere with their functionality. ADC functions are enabled using the PCR[APC] bit; other functions are enabled by enabling the respective module.

3  Using the PSMI registers in the System Integration Unit Lite (SIUL), different pads can be multiplexed to the same peripheral input. Please see the SIUL chapter of the *MPC5645S Microcontroller Reference Manual* for details.

4  See the "Pad types" table for an explanation of the letters in this column.

5  Reset configuration is given as I/O direction and pull, e.g., "Input, pullup".

6  Out of reset pins PH[0:3] are available as JTAG pins (TCK, TDI, TDO and TMS respectively). It is up to the user to configure pins PH[0:3] when needed.

The location of TCON[0:3] pins is mentioned in the following table.

## Table 8. Location of TCON[0:3] Pins

| Function | Port Name | PCR | Ball Number |
|---|---|---|---|
| DCU_TAG / TCON0 | PK11 | PCR[132] | Ball No: AC09 |
| DCU_TAG / TCON0 | PJ12 | PCR[117] | Ball No: A23 |
| DCU_HSYNC/TCON1 | PG9 | PCR[95] | Ball No: T02 |
| DCU_VSYNC / TCON2 | PG8 | PCR[94] | Ball No: T04 |
| DCU_DE / TCON3 | PG10 | PCR[96] | Ball No: T01 |
| DCU_TAG/TCON3 | PM5 | PCR[152] | NC (only on 176) |

The following pad types are available for system pins and functional port pins:

**Table 9. Pad Types**

| Pad | Function |
|---|---|
| S | Slow (pad_ssr, pad_ssr_hv) |
| M | Medium (pad_msr, pad_msr_hv) |
| F | Fast (pad_fc) |
| J | Input/output with analog features (pad_tgate, pad_tgate_hv) |
| Analog | Input only with analog features (pad_ae, pad_ae_hv) |
| SMD | Stepper Motor Detector |
| DDR | DDR pads |
| RSDS | RSDS pads |

# 3 System design information

## 3.1 Power-up sequencing

The preferred power-up sequence for MPC5645S is as follows:

1. Generic IO supplies or noise-free supplies, consisting of:
   — VDDA
   — VDDE_A
   — VDDE_B
   — VDDM
   — VDD_DR
   — VDD33_DR
   — VDDPLL

2. All 3.3V supplies (VDDE_B & VDD33_DR) should be ramped up first, and then the rest of the I/O supplies should be ramped up (VDDA, VDDE_A, VDDM, VDD_DR).

3. VDDR, the regulator input supply, should be the last supply to ramp up; all supplies can be ramped up together as long as VDDR is included. So all 5V supplies should be ramped up after the 3.3V supplies, and if all the supplies are of the same level, they can be ramped up together as well.

4. LV supply (VDD12). If Vreg is in bypass mode and the core supply (1.2V) is supplied externally, then this should be the last supply given.

### NOTE

For DDR, the 3.3 V supply (VDD33_DR) should come before VDD_DR.

### NOTE

Vreg bypass mode is for factory testing only.

This sequence ensures that when VREG releases its LVDs, the IO and other HV segments are powered properly. This is important because MPC5645S doesn't monitor LVDs on IO HV supplies.

# 4 Electrical characteristics

## 4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level ($V_{DD}$ or $V_{SS}$). This could be done by internal pull up and pull down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

## 4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 10 are used and the parameters are tagged accordingly in the tables where appropriate.

**Table 10. Parameter Classifications**

| Classification tag | Tag description |
|---|---|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

### NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

## 4.3 Absolute maximum ratings

**Table 11. Absolute maximum ratings**

| Symbol | C | | Parameter | Conditions | Value | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | | |
| $V_{DDA}$ | SR | D | Voltage on VDDA pin (ADC reference) with respect to ground ($V_{SSA}$) | — | −0.3 | +5.5 | V | D1.1 |
| | | | | Relative to $V_{DD}$ | $V_{DD}$−0.3 | $V_{DD}$+0.3 | | |
| $V_{SSA}$ | SR | D | Voltage on VSSA (ADC reference) pin with respect $V_{SS}$ | — | $V_{SS}$−0.1 | $V_{SS}$+0.1 | V | D1.2 |
| $V_{DDPLL}$ | CC | D | Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground ($V_{SSPLL}$) | — | 1.08 | 1.4 | V | D1.3 |
| | | | | Relative to $V_{DD}$ | $V_{DD}$−0.3 | $V_{DD}$+0.3 | | |
| $V_{DDR}$ | SR | D | Voltage on VDDR pin (regulator supply) with respect to ground ($V_{SSR}$) | — | −0.3 | +5.5 | V | D1.4 |
| | | | | Relative to $V_{DD}$ | $V_{DD}$−0.3 | $V_{DD}$+0.3 | | |
| $V_{SSR}$ | SR | D | Voltage on VSSR (regulator ground) pin with respect to $V_{SS}$ | — | $V_{SS}$−0.1 | $V_{SS}$+0.1 | V | D1.5 |
| $V_{DD12}$ | CC | D | Voltage on VDD12 pin with respect to ground ($V_{SS12}$) | — | 1.08 | 1.4 | V | D1.6 |
| $V_{SS12}$ | CC | D | Voltage on VSS12 pin with respect to $V_{SS}$ | — | $V_{SS}$−0.1 | $V_{SS}$+0.1 | V | D1.7 |
| $V_{DDE\_A}$[1] | SR | D | Voltage on VDDE_A (I/O supply) pin with respect to ground ($V_{SSE\_A}$) | — | −0.3 | +5.5 | V | D1.8 |
| $V_{DDE\_B}$[1] | SR | D | Voltage on VDDE_B (I/O supply) pin with respect to ground ($V_{SS}$) | — | −0.3 | +3.6 | V | D1.9 |

Table 11. Absolute maximum ratings (continued)

| Symbol | C | | Parameter | Conditions | Value | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | | |
| $V_{DDM}$[1] | SR | D | Voltage on VDDM (stepper motor supply) pin with respect to ground ($V_{SSM}$) | — | −0.3 | +5.5 | V | D1.10 |
| $V_{SS}$[2] | SR | D | I/O supply ground | — | 0 | 0 | V | D1.11 |
| $V_{DD\_DR}$ | | D | Voltage on $V_{DDDDR}$ with respect to $V_{SS}$ | — | −0.3 | 3.6 | V | D1.12 |
| $V_{RSDS}$ | | D | Voltage on $V_{DDRSDS}$ with respect to $V_{SS}$ | — | −0.3 | 3.6 | V | D1.13 |
| $V_{IN}$ | SR | D | Voltage on any GPIO pin with respect to ground ($V_{SS}$) | — | −0.3 | $V_{DDmax}$ ($V_{DDE}$ max of that segment) | V | — |
| $I_{INJPAD}$ | SR | D | Injected input current on any pin during overload condition | — | −10 | 10 | mA | D1.15 |
| $I_{INJSUM}$ | SR | D | Absolute sum of all injected input currents during overload condition | — | −50 | 50 | | D1.16 |
| $T_{STORAGE}$ | SR | T | Storage temperature | — | −55 | 150 | °C | D1.17 |
| $ESD_{HBM}$ | SR | T | ESD Susceptibility (Human Body Model) | — | — | 2000 | V | D1.18 |

[1] Throughout the remainder of this document $V_{DD}$ refers collectively to I/O voltage supplies, i.e., $V_{DDE\_A}$, $V_{DDE\_B}$, and $V_{DDM}$, unless otherwise noted.

[2] Throughout the remainder of this document $V_{SS}$ refers collectively to I/O voltage supply grounds, i.e., $V_{SSE\_A}$, $V_{SSPLL}$, and $V_{SSM}$, unless otherwise noted.

## NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground ($V_{SS}$) must not exceed the recommended values.

# 4.4    Recommended operating conditions

Table 12. Recommended operating conditions (3.3 V)

| Symbol | C | | Parameter | Conditions | Value | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | | |
| $V_{DDA}$[1] | SR | P | Voltage on VDDA pin (ADC reference) with respect to ground ($V_{SS}$) | — | +3.0 | +3.6 | V | D2.1 |
| | | D | | Relative to $V_{DD}$ | $V_{DD}$−0.1 | $V_{DD}$+0.1 | | |
| $V_{SSA}$ | SR | P | Voltage on VSSA (ADC reference) pin with respect $V_{SS}$ | — | $V_{SS}$−0.1 | $V_{SS}$+0.1 | V | D2.2 |
| $V_{DDPLL}$ | CC | P | Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground ($V_{SSPLL}$) | — | 1.08 | 1.32 | V | D2.3 |

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**Table 12. Recommended operating conditions (3.3 V) (continued)**

| Symbol | C | | Parameter | Conditions | Value Min | Value Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| $V_{DDR}{}^2$ | SR | P | Voltage on VDDR pin (regulator supply) with respect to ground ($V_{SSR}$) | — | +3.0 | +3.6 | V | D2.4 |
| | | D | | Relative to $V_{DD}$ | $V_{DD}$–0.1 | $V_{DD}$+0.1 | | |
| $V_{SSR}$ | SR | D | Voltage on VSSR (regulator ground) pin with respect to $V_{SS}$ | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V | D2.5 |
| $V_{DD12}{}^{3,4}$ | CC | P | Voltage on VDD12 pin with respect to ground ($V_{SS12}$) | — | 1.08 | 1.4 | V | D2.6 |
| $V_{SS12}$ | CC | D | Voltage on VSS12 pin with respect to $V_{SS}$ | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V | D2.7 |
| $V_{DD}{}^{5,6,7}$ | SR | P | Voltage on $V_{DD}$ pins ($V_{DDE\_A}$, $V_{DDE\_B}$, $V_{DD\_DR}$, $V_{DDM}$) with respect to ground ($V_{SS}$) | — | $V_{DDmin}{}^5$ | $V_{DDmax}{}^5$ | V | D2.8 |
| $V_{SS}{}^8$ | SR | D | I/O supply ground | — | 0 | 0 | V | D2.9 |
| $V_{DDE\_A}{}^9$ | SR | P | Voltage on VDDE_A (I/O supply) pin with respect to ground ($V_{SSE\_A}$) | — | +3.0 | +3.6 | V | D2.10 |
| $V_{DDE\_B}$ | SR | P | Voltage on VDDE_B (I/O supply) pin with respect to ground ($V_{SSE\_B}$) | — | +3.0 | +3.6 | V | D2.11 |
| $V_{DDM}$ | SR | P | Voltage on VDDM (stepper motor supply) pin with respect to ground ($V_{SSM}$) | — | +3.0 | +3.6 | V | D2.12 |
| $V_{DD\_DR}$ | | P | Voltage on $V_{DDDDR}$ with respect to $V_{SS}$ | — | +1.62 | +3.6 | V | D2.13 |
| $V_{SS\_DR}$ | | D | Voltage on $V_{SSRSDS}$ with respect to $V_{SS}$ | — | +1.62 | +3.6 | V | D2.14 |
| $V_{RSDS}$ | | P | Voltage on $V_{DDDDR}$ with respect to $V_{SS}$ | — | +3.0 | +3.6 | V | D2.15 |
| $TV_{DD}$ | SR | D | $V_{DD}$ slope to ensure correct power up[10] | — | — | 12 | V/ms | D2.16 |
| $T_A$ | SR | P | Ambient temperature under bias | — | -40 | +105 | °C | D2.17 |
| $T_J$ | SR | D | Junction temperature under bias | | -40 | +140 | | D2.18 |

[1] 100 nF capacitance needs to be provided between $V_{DDA}$/$V_{SSA}$ pair.

[2] 10 µF capacitance must be connected between $V_{DDR}$ and $V_{SS12}$ because of a sharp surge due to external ballast.

[3] $V_{DD12}$ cannot be used to drive any external component.

[4] Each $V_{DD12}$/$V_{SS12}$ supply pair should have a 10 µF capacitor. Absolute combined maximum capacitance is 40 µF. Preferably, all the VDD12 supply pads should be shorted and then connected to a 4×10 µF capacitance. This is to ensure the ESR of external capacitance does not exceed 0.2 Ω. A 100 nF capacitor must be placed close to the pin.

[5] $V_{DD}$ refers collectively to I/O voltage supplies, i.e., $V_{DDE\_A}$, $V_{DDE\_B}$, $V_{DD\_DR}$, and $V_{DDM}$.

[6] 100 nF capacitance needs to be provided between each $V_{DD}$/$V_{SS}$ pair. VDDmin value for is 3 V for VDDE_A & VDDM as well as for VDDE_B, while it is 1.62 V for VDD_DR. VDD max value is 3.6 V for VDDE_A & VDDM as well as for VDDE_B & VDD_DR.

[7] Full electrical specification cannot be guaranteed when voltage drops below 3.0V. In particular, ADC electrical characteristics and I/O's DC electrical specification may not be guaranteed.
When voltage drops below $V_{LVDHVL}$ device is reset.

[8] $V_{SS}$ refers collectively to I/O voltage supply grounds, i.e., $V_{SSE\_A}$, $V_{SS}$, and $V_{SSM}$ unless otherwise noted.

[9] $V_{DDE\_A}$ should not be less than $V_{DDA}$.

[10] Guaranteed by device validation.

## 4.5 Thermal characteristics

**Table 13. Recommended operating conditions (5.0 V)**

| Symbol | C | | Parameter | Conditions | Value | | Unit | Spe-cID |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | | |
| $V_{DDA}$[1] | SR | P | Voltage on VDDA pin (ADC reference) with respect to ground ($V_{SS}$) | — | +4.5 | +5.5 | V | D2.19 |
| | | D | | Voltage drop[2] | +3.0 | +5.5 | | |
| | | D | | Relative to $V_{DD}$ | $V_{DD}$–0.1 | $V_{DD}$+0.1 | | |
| $V_{SSA}$ | SR | D | Voltage on VSSA (ADC reference) pin with respect $V_{SS}$ | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V | D2.20 |
| $V_{DDPLL}$ | CC | P | Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground ($V_{SSPLL}$) | — | 1.08 | 1.32 | V | D2.21 |
| $V_{DDR}$[3] | SR | P | Voltage on VDDR pin (regulator supply) with respect to ground ($V_{SSR}$) | — | +4.5 | +5.5 | V | D2.22 |
| | | D | | Voltage drop[2] | +4.5 | +5.5 | | |
| | | D | | Relative to $V_{DD}$ | $V_{DD}$–0.1 | $V_{DD}$+0.1 | | |
| $V_{SSR}$ | SR | D | Voltage on VSSR (regulator ground) pin with respect to $V_{SS}$ | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V | D2.23 |
| $V_{DD12}$[4,5] | CC | P | Voltage on VDD12 pin with respect to ground ($V_{SS12}$) | — | 1.08 | 1.4 | V | D2.24 |
| $V_{SS12}$ | CC | D | Voltage on VSS12 pin with respect to $V_{SS}$ | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V | D2.25 |
| $V_{DD}$[6,7] | SR | P | Voltage on VDD pins (VDDE_A, VDDE_B, VDD_DR, VDDMA, VDDMB, VDDMC) with respect to ground ($V_{SS}$) | Voltage drop[2] | $V_{DDmin}$[6] | $V_{DDmax}$[6] | V | D2.26 |
| $V_{SS}$[8] | SR | D | I/O supply ground | — | 0 | 0 | V | D2.27 |
| $V_{DDE\_A}$[9] | SR | P | Voltage on VDDE_A (I/O supply) pin with respect to ground ($V_{SSE\_A}$) | — | +4.5 | +5.5 | V | D2.28 |
| $V_{DDE\_B}$[10] | SR | P | Voltage on VDDE_B (I/O supply) pin with respect to ground ($V_{SSE\_B}$) | — | +3.0 | +3.6 | V | D2.29 |
| $V_{DDM}$ | SR | P | Voltage on VDDMA (stepper motor supply) pin with respect to ground ($V_{SSMA}$) | — | +4.5 | +5.5 | V | D2.30 |
| $V_{DD\_DR}$[11] | | P | Voltage on $V_{DD\_DR}$ with respect to $V_{SS}$ | — | +1.62 | +3.6 | V | D2.31 |
| $V_{SS\_DR}$ | | D | Voltage on $V_{SSRSDS}$ with respect to $V_{SS}$ | — | +1.62 | +3.6 | V | D2.32 |
| $V_{RSDS}$ | | P | Voltage on $V_{DD\_DR}$ with respect to $V_{SS}$ | — | +3.0 | +3.6 | V | D2.33 |
| $TV_{DD}$ | SR | D | $V_{DD}$ slope to ensure correct power up[12] | — | — | 12 | V/ms | D2.34 |
| $T_A$ | SR | P | Ambient temperature under bias | — | –40 | +105 | °C | D2.35 |
| | | | | | –40 | +105 | | |
| $T_J$ | SR | D | Junction temperature under bias | — | –40 | +140 | — | D2.36 |

[1] 100 nF capacitance needs to be provided between $V_{DDA}$/$V_{SSA}$ pair.

[2] Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, I/O DC and ADC electrical characteristics may not be guaranteed below 4.5 V during the voltage drop sequence.

[3] 10 µF capacitance must be connected between $V_{DDR}$ and $V_{SS12}$. It is recommended that this cap should be placed, as close as possible to the DUT pin on board.

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4 $V_{DD12}$ cannot be used to drive any external component.

5 Each $V_{DD12}$/$V_{SS12}$ supply pair should have a 10 µF capacitor. Absolute combined maximum capacitance is 40 µF. Preferably, all the VDD12 supply pads should be shorted and then connected to a 4×10 µF capacitance. This is to ensure the ESR of external capacitance does not exceed 0.2 Ω. A 100 nF capacitor must be placed close to the pin.

6 $V_{DD}$ refers collectively to I/O voltage supplies, i.e., $V_{DDE\_A}$, $V_{DDE\_B}$, $V_{DD\_DR}$, $V_{DDMA}$, $V_{DDMB}$ and $V_{DDMC}$. VDDmin value for is 4.5 V for VDDE_A & VDDM, 3 V VDDE_B, while it is 1.62 V for VDD_DR. VDD max value is 5.5 V for VDDE_A & VDDM and 3.6 V for VDDE_B & VDD_DR.

7 100 nF capacitance needs to be provided between each $V_{DD}$/$V_{SS}$ pair.

8 $V_{SS}$ refers collectively to I/O voltage supply grounds, i.e., $V_{SSE\_A}$, $V_{SSE\_B}$, $V_{SSE\_A}$, $V_{SSE\_E}$, $V_{SSMA}$, $V_{SSMB}$ and $V_{SSMC}$) unless otherwise noted.

9 $V_{DDE\_A}$ should not be less than $V_{DDA}$.

10 VDDE_B cannot go beyond 3.6V under any operating condition.

11 VDD_DR can be 1.8, 2.5 and 3.3V (typical) based on type of SDR memory.

12 Guaranteed by device validation.

### Table 14. Thermal characteristics for 176-pin LQFP[1]

| Symbol | C | | Parameter | Conditions | Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | CC | D | Junction to Ambient Natural Convection[2] | Single layer board - 1s | 36 | °C/W | D3.1 |
| $R_{\theta JA}$ | CC | D | Junction to Ambient Natural Convection[2] | Four layer board - 2s2p | 29 | °C/W | D3.2 |
| $R_{\theta JMA}$ | CC | D | Junction to Ambient[2] | @200 ft./min., single layer board - 1s | 28 | °C/W | D3.3 |
| $R_{\theta JMA}$ | CC | D | Junction to Ambient[2] | @200 ft./min., Four layer board - 2s2p | 23 | °C/W | D3.4 |
| $R_{\theta JB}$ | CC | D | Junction to Board[3] | — | 18 | °C/W | D3.5 |
| $R_{\theta JCtop}$ | CC | D | Junction to Case (Top)[4] | — | 5 | °C/W | D3.6 |
| $\Psi_{JT}$ | CC | D | Junction to Package Top Natural Convection[5] | — | 2 | °C/W | D3.7 |

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### Table 15. Thermal characteristics for 208-pin LQFP[1]

| Symbol | C | | Parameter | Conditions | Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | CC | D | Junction to Ambient Natural Convection[2] | Single layer board - 1s | 34 | °C/W | D3.8 |
| $R_{\theta JA}$ | CC | D | Junction to Ambient Natural Convection[2] | Four layer board - 2s2p | 27 | °C/W | D3.9 |
| $R_{\theta JMA}$ | CC | D | Junction to Ambient[2] | @200 ft./min., single layer board - 1s | 27 | °C/W | D3.10 |
| $R_{\theta JMA}$ | CC | D | Junction to Ambient[2] | @200 ft./min., Four layer board - 2s2p | 22 | °C/W | D3.11 |
| $R_{\theta JB}$ | CC | D | Junction to Board[3] | — | 18 | °C/W | D3.12 |
| $R_{\theta JCtop}$ | CC | D | Junction to Case (Top)[4] | — | 5 | °C/W | D3.13 |

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Table 15. Thermal characteristics for 208-pin LQFP[1] (continued)

| Symbol | C | | Parameter | Conditions | Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| $\Psi_{JT}$ | CC | D | Junction to Package Top Natural Convection[5] | — | 2 | °C/W | D3.14 |

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization.

[2] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[4] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### Table 16. Thermal characteristics for 416-pin TEPBGA[1]

| Symbol | C | | Parameter | Conditions | Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | CC | D | Junction to Ambient Natural Convection[2] | Single layer board - 1s | 26 | °C/W | D3.15 |
| $R_{\theta JA}$ | CC | D | Junction to Ambient Natural Convection[2] | Four layer board - 2s2p | 18 | °C/W | D3.16 |
| $R_{\theta JMA}$ | CC | D | Junction to Ambient[2] | @200 ft./min., single layer board - 1s | 20 | °C/W | D3.17 |
| $R_{\theta JMA}$ | CC | D | Junction to Ambient[2] | @200 ft./min., Four layer board - 2s2p | 15 | °C/W | D3.18 |
| $R_{\theta JB}$ | CC | D | Junction to Board[3] | — | 10 | °C/W | D3.19 |
| $R_{\theta JCtop}$ | CC | D | Junction to Case (Top)[4] | — | 6 | °C/W | D3.20 |
| $\Psi_{JT}$ | CC | D | Junction to Package Top Natural Convection[5] | — | 2 | °C/W | D3.21 |

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization.

[2] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[4] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 4.5.1    General notes for specifications at maximum junction temperature

An estimate of the chip junction temperature, $T_J$, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D)$$

*Eqn. 1*

where:

$T_A$ = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$P_D$ = power dissipation in the package (W)

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The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D)$$ *Eqn. 2*

where:

$T_B$= board temperature for the package perimeter ($^o$C)

$R_{\theta JB}$= junction-to-board thermal resistance ($^o$C/W) per JESD51-8S

$P_D$= power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$ *Eqn. 3*

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^o$C/W)

$R_{\theta JC}$= junction to case thermal resistance ($^o$C/W)

$R_{\theta CA}$= case to ambient thermal resistance ($^o$C/W)

$R_{\theta JC}$ s device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

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A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter ($\Psi_{JT}$) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \qquad \textbf{\textit{Eqn. 4}}$$

where:

$T_T$= thermocouple temperature on top of the package ($^o$C)

$\Psi_{JT}$= thermal characterization parameter ($^o$C/W)

$P_D$= power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

## 4.6 EMI (electromagnetic interference) characteristics

Table 17. EMI testing specifications[1] [2]

| Symbol | Parameter | Conditions | Clocks | Frequency Range | Level (Typ) | Unit |
|---|---|---|---|---|---|---|
| Radiated Emissions | $V_{EME}$ | Device Configuration, test conditions and EM testing per standard IEC61967-2 | FOSC – 8MHz, External Crystal FCPU – 124MHz FBUS – 124MHz No PLL Frequency Modulation | 150 kHz – 50 MHz | 19 | dBμV |
| | | | | 50 MHz – 150 MHz | 30 | |
| | | | | 150 MHz – 500 MHz | 25 | |
| | | | | 500 MHz – 1000 MHz | 19 | |
| | | | | IEC Level | K | — |
| | | | FOSC - 8MHz, External Crystal FCPU -124MHz FBUS -124MHz 2% PLL Frequency Modulation | 150 kHz – 50 MHz | 15 | dBμV |
| | | | | 50 MHz – 150 MHz | 24 | |
| | | | | 150 MHz – 500 MHz | 17 | |
| | | | | 500 MHz – 1000 MHz | 14 | |
| | | | | IEC Level | L | — |

[1] The reported emission level is the value of the maximum emission, rounded up to the next whole number.

[2] IEC Level Maximum:, L is less than or equal to 24 dBμV, K is less than or equal to 30 dBμV.

## 4.7 Power management

### 4.7.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN (BCP68 or NJD2873) ballast to be connected as shown in Figure 6 as well as an external capacitance ($C_{REG}$) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 15 nH.

For the MPC5645S microcontroller, 100 nF should be placed between each $V_{DD12}/V_{SS12}$ supply pair and also between the $V_{DDPLL}/V_{SSPLL}$ pair. Additionally, 10 μF should be placed between the $V_{DDR}$ pin and the adjacent $V_{SS}$ pin.

$V_{DDR}$ = 3.0 V to 3.6 V / 4.5 V to 5.5 V, $T_A$ = -40 to 105 °C, unless otherwise specified.

$V_{DDR}$

VRC_CTRL

$V_{DD12}$
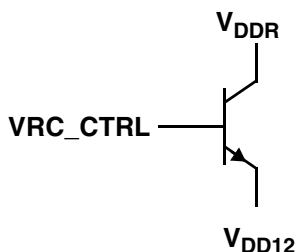
**Figure 6. External NPN ballast connections**

**Table 18. Voltage regulator electrical characteristics**

| Symbol | C | | Parameter | Conditions | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| $V_{DDR}$ | SR | P | Power supply | — | 3.0 | 5.5 | V | D5.1 |
| $T_J$ | SR | D | Junction temperature | — | -40 | 140 | °C | D5.2 |
| $I_{REG}$ | CC | T | Current consumption | Reference included, @ 55 °C No load @ Full load | — | 2 11 | mA | D5.3 |
| $I_L$ | CC | T | Output current capacity | DC load current | — | 450 | mA | D5.4 |
| $V_{DD12}$ | CC | D | Output voltage (value @ $I_L$ = 0 @ 27°C) | Pre-trimming sigma < 7 mV | — | 1.330 | V | D5.5 |
| | | P | | Post-trimming | 1.145 | 1.32 | | |
| | | T | Output voltage (value @ $I_L$ = Imax) | Post-trimming | 1.145 | — | | |
| | SR | D | External decoupling/stability capacitor | 4 capacitances of 10 µF each | 10 * 4 | | µF | D5.6 |
| | | D | | ESR of external cap | 0.05 | 0.2 | Ω | |
| | | D | | 1 bond wire R + 1 pad R | 0.2 | 1 | Ω | |
| $L_{BOND}$ | CC | D | Bonding Inductance for Bipolar Base Control pad | — | 0 | 15 | nH | D5.7 |
| | CC | D | Power supply rejection | @ DC @ no load | Cload = 10 µF * 4 | — | −30 | dB | D5.8 |
| | | D | | @ 200 kHz @ no load | | | −100 | | |
| | | D | | @ DC @ 400 mA | | | −30 | | |
| | | D | | @ 200 kHz @ 400 mA | | | −30 | | |
| | CC | D | Load current transient | Cload = 10 µF * 4 | — | 10% to 90% of $I_L$ (max) in 100 ns | | D5.9 |
| $t_{SU}$ | CC | T | Start-up time after input supply stabilizes[1] | Cload = 10 µF * 4 | — | 500 | µs | D5.10 |

[1] Time after the input supply to the voltage regulator has ramped up (VDDR) and the voltage regulator has asserted the Power OK signal.

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**Table 19. Low-power voltage regulator electrical characteristics**

| Symbol | | C | Parameter | Conditions | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| $T_J$ | SR | D | Junction temperature | — | −40 | 140 | °C | D5.2 |
| $I_{REG}$ | CC | T | Current consumption | Reference included, @ 55 °C No load @ Full load | — | 5 600 | µA | D5.3 |
| $I_L$ | CC | T | Output current capacity | DC load current | — | 15 | mA | D5.4 |
| $V_{DD12}$ | CC | D | Output voltage | Pre-trimming sigma < 7 mV | — | 1.33 | V | D5.5 |
| | | P | | Post-trimming | 1.14 | 1.32 | | |

**Table 20. Ultra low-power voltage regulator electrical characteristics**

| Symbol | | C | Parameter | Conditions | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| $T_J$ | SR | D | Junction temperature | — | −40 | 140 | °C | D5.2 |
| $I_{REG}$ | CC | T | Current consumption | Reference included, @ 55 °C No load @ Full load | — | 2 100 | µA | D5.3 |
| $I_L$ | CC | T | Output current capacity | DC load current | — | 5 | mA | D5.4 |
| $V_{DD12}$ | CC | D | Output voltage (value @ $I_L$ = 0 @ 27°C) | Pre-trimming sigma < 7 mV | — | 1.33 | V | D5.5 |
| | | P | | Post-trimming | 1.14 | 1.32 | | |

## 4.7.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD}$ and the $V_{DD12}$ voltage while device is supplied:

- POR monitors $V_{DD}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD}$ to ensure device reset below minimum functional supply
- LVDHV5 monitors $V_{DD}$ when application uses device in the 5.0V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

**Table 21. Low voltage monitor electrical characteristics**

| Symbol | C | | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| $V_{PORH}$ | CC | C | Power-on reset threshold | — | 1.5 | — | 2.7 | V | D5.11 |
| $V_{LVDHV3H}$ | CC | C | LVDHV3 low voltage detector high threshold | — | — | — | 2.9 | | D5.12 |
| $V_{LVDHV3L}$ | CC | C | LVDHV3 low voltage detector low threshold | — | 2.5 | — | — | | D5.13 |
| $V_{LVDHV5H}$ | CC | C | LVDHV5 low voltage detector high threshold | — | — | — | 4.4 | | D5.14 |
| $V_{LVDHV5L}$ | CC | C | LVDHV5 low voltage detector low threshold | — | 3.9 | — | — | | D5.15 |
| $V_{LVDLVCORH}$ | CC | C | LVDLVCOR low voltage detector high threshold | $T_A$ = 25°C, after trimming | — | — | 1.185 | | D5.16 |
| $V_{LVDLVCORL}$ | CC | C | LVDLVCOR low voltage detector low threshold | | 1.095 | — | — | | D5.17 |

[1] $V_{DD}$ = 3.3V ± 10% / 5.0V ± 10%, $T_A$ = -40 / +105°C, unless otherwise specified

[2] All values need to be confirmed during device validation.

## 4.7.3 Low voltage domain power consumption

Table 22 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

**Table 22. DC electrical characteristics**

| Symbol | C | | Parameter | Conditions[1] | | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{DDMAX}$[2] | CC | D | RUN mode maximum average current | — | — | — | 295 | 375[3] | mA |
| $I_{DDRUN}$[4] | CC | P | RUN mode typical average current[5] | $f_{CPU}$ = 125MHz, Dual Display Drive with external DRAM, 416 TEPBGA package option only | — | — | 275 | — | mA |
| | | | | $f_{CPU}$ = 125MHz, Single Display Drive, no external DRAM, 176 LQFP / 208 LQFP package options | — | — | 240 | — | |
| $I_{DDHALT}$ | CC | C | HALT mode current[6] | Slow internal RC oscillator (128KHz) running | $T_A$ = 25 °C | — | 17.5 | 23.5 | mA |
| | | P | | | $T_A$ = 105 °C | — | 35 | 45.5 | |
| $I_{DDSTOP}$ | CC | D | STOP mode current[7] [8] | Slow internal RC oscillator (128KHz) running | $T_A$ = −40°C | — | 645 | — | µA |
| | | D | | | $T_A$ = 0°C | — | 1100 | — | |
| | | P | | | $T_A$ = 25°C | — | 1531 | 5500 | |
| | | D | | | $T_A$ = 55°C | — | 3.8 | — | mA |
| | | D | | | $T_A$ = 85°C | — | 9.7 | — | |
| | | C | | | $T_A$ = 105°C | — | 17.67 | 36.5 | |

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**Table 22. DC electrical characteristics (continued)**

| Symbol | C | | Parameter | Conditions[1] | | Value[2] | | | Unit |
|--------|---|---|-----------|---------------|---|-----|-----|-----|------|
| | | | | | | Min | Typ | Max | |
| $I_{DDSTDBY2}$ | CC | D | STANDBY2 mode current[9] (64K SRAM on) | SXOSC (32KHz) ON and RTC running | $T_A = -40^oC$ | — | 470 | — | µA |
| | | D | | | $T_A = 0^oC$ | — | 480 | — | |
| | | P | | | $T_A = 25^oC$ | — | 481 | 490 | |
| | | D | | | $T_A = 55^oC$ | — | 525 | — | |
| | | D | | | $T_A = 85^oC$ | — | 650 | — | |
| | | P | | | $T_A = 105^oC$ | — | 870 | 910 | |
| | CC | D | | SXOSC (32KHz) and RTC OFF | $T_A = -40^oC$ | — | 63 | — | µA |
| | | D | | | $T_A = 0^oC$ | — | 85 | — | |
| | | P | | | $T_A = 25^oC$ | — | 93 | 100 | |
| | | D | | | $T_A = 55^oC$ | — | 95 | — | |
| | | D | | | $T_A = 85^oC$ | — | 190 | — | |
| | | P | | | $T_A = 105^oC$ | — | 390 | 430 | |
| $I_{DDSTDBY1}$ | CC | D | STANDBY1 mode current (8K SRAM on)[10] | SXOSC (32KHz) ON and RTC running | $T_A = -40^oC$ | — | 415 | — | µA |
| | | D | | | $T_A = 0^oC$ | — | 422 | — | |
| | | P | | | $T_A = 25^oC$ | — | 426 | 430 | |
| | | D | | | $T_A = 55^oC$ | — | 575 | — | |
| | | D | | | $T_A = 85^oC$ | — | 680 | — | |
| | | P | | | $T_A = 105^oC$ | — | 810 | 915 | |
| | CC | D | | SXOSC (32 KHz) and RTC OFF | $T_A = -40^oC$ | — | 20 | — | µA |
| | | D | | | $T_A = 0^oC$ | — | 22 | — | |
| | | P | | | $T_A = 25^oC$ | — | 29 | 75 | |
| | | D | | | $T_A = 55^oC$ | — | 47 | — | |
| | | D | | | $T_A = 85^oC$ | — | 118 | — | |
| | | P | | | $T_A = 105^oC$ | — | 236 | 410 | |

[1] $V_{DD}$ = 3.0V to 5.5V, $T_A$ = -40 to 105 °C, unless otherwise specified.

[2] $I_{DDMAX}$ is composed of the current consumption on all supplies ($V_{DD12}$, $V_{DDE\_A}$, $V_{DDE\_B}$, $V_{DDA}$, $V_{DDR}$, $V_{DDM}$, $V_{DDPLL}$, $V_{DD\_DR}$). It does not include current consumption linked to I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application; switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

[3] Higher current may be sinked by device during power-up and standby exit. Please refer to inrush current in Table 23.

[4] RUN current measured with typical application and accesses on both flash and RAM.

[5] Data and Code Flash in Normal Power. Code fetched from RAM: DCUs running with 20MHz pixel clock, QuadSPI fetching data at 80MHz, GPU accessing internal SRAM and external DRAM, DMA, RLE, and VIU active, Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/ADC/SMD/SSD/SGM) and running at max frequency, periodic SW/WDG timer reset enabled.

# 4.8  DC electrical specifications

## 4.8.1  DC specification for CMOS090LP2 library @ VDDE = 3.3 V

### NOTE

These pad specifications are applicable for pads in the Digital segment Only. See the "GPIO power bank supplies and functionality" table in the "Voltage Regulators and Power Supplies" chapter of the reference manual for details.

**Table 23. DC electrical specifications**

| Symbol | C | | Parameter | Condition | Value | | Unit | SpecID |
|--------|---|---|-----------|-----------|-------|-----|------|--------|
| | | | | | Min | Max | | |
| Vdd | SR | P | Core supply voltage | — | 1.08 | 1.32 | V | D9.1 |
| Vdde | SR | P | I/O supply voltage | — | 3.0 | 3.6 | V | D9.2 |
| Vdd33 | SR | P | I/O pre-driver supply voltage | — | 3.0 | 3.6 | V | D9.3 |
| Vih_c | SR | P | CMOS input buffer high voltage | With hysteresis enabled | 0.65×Vdde | Vdde+0.3 | V | D9.4 |
| | | | | With hysteresis disabled | 0.55×Vdde | Vdde+0.3 | | |
| Vil_c | SR | P | CMOS input buffer low voltage | With hysteresis enabled | Vss–0.3 | 0.35×Vdde | V | D9.5 |
| | | | | With hysteresis disabled | Vss–0.3 | 0.40×Vdde | | |
| Vhys_c | SR | T | CMOS input buffer hysteresis | — | 0.1×Vdde | — | V | D9.6 |
| Vih_fod_h | SR | P | 5 V tolerant CMOS input buffer high voltage | With hysteresis enabled | 0.65×Vdd33 | Vdd33+0.3 | V | D9.7 |
| Vil_fod_h | SR | P | 5 V tolerant CMOS input buffer low voltage | With hysteresis enabled | Vss–0.3 | 0.35×Vdd33 | V | D9.8 |
| Iact_s | SR | T | Selectable weak pullup/pulldown current | — | 25 | 150 | µA | D9.9 |
| Iinact_d | SR | P | Digital pad input leakage current | Weak pull inactive | –2.5 | 2.5 | µA | D9.10 |

**Table 23. DC electrical specifications (continued)**

| Symbol | | C | Parameter | Condition | Value | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | | |
| Iinact_a | SR | P | Analog pad input leakage current | Weak pull inactive | −150 | 150 | nA | D9.11 |
| Voh | SR | P | Output high voltage | Refer to Table 24 | 0.8 ×Vdde | — | V | D9.12 |
| Vol | SR | P | Output low voltage | Refer to Table 24 | — | 0.2×Vdde | V | D9.13 |
| Vol_fod_h | SR | C | Fast open-drain output low voltage | Iol_fod_h = 10 mA | — | 0.2×Vdd33 | — | D9.16 |

**Table 24. Drive current, VDDE=3.3 V (+/- 10%)**

| Pad | C | Drive mode | Minimum Ioh (mA)[1] | Minimum Iol (mA)[2] |
|---|---|---|---|---|
| pad_fc | C | 00 | 16.1 | 24 |
| | | 01 | 31.8 | 47.9 |
| | | 10 | 47.2 | 70.6 |
| | | 11 | 77 | 114.5 |
| pad_msr | C | All | 61.9 | 83.6 |
| pad_ssr | C | All | 61.9 | 83.6 |

[1]  Ioh is defined as the current sourced by the pad to drive the output to Voh.

[2]  Iol is defined as the current sunk by the pad to drive the output to Vol.

**Table 25. Supply leakage**

| Pad | C | VDD | VDDE (Typ/Max) | VDD33 (Typ/Max) |
|---|---|---|---|---|
| pad_fc | D | 90 µA | 3 nA / 4 µA | 1 nA / 30 µA |
| pad_msr | | — | — | — |
| pad_ssr | | — | — | — |

## 4.8.2 DC specification for CMOS090LP2fg library @ VDDE = 5.0 V

### NOTE

These pad specifications are applicable for pads in the Analog segment Only. See the "GPIO power bank supplies and functionality" table in the "Voltage Regulators and Power Supplies" chapter of the reference manual for details.

**Table 26. DC electrical specifications**

| Symbol | | C | Parameter | Condition | Value | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | | |
| Vdd | SR | P | Core supply voltage | — | 1.08 | 1.32 | V | D9.17 |
| Vdde | SR | P | I/O supply voltage | — | 4.5 | 5.5 | V | D9.18 |
| Vdd33 | SR | P | I/O pre-driver supply voltage | — | 3.0 | 3.6 | V | D9.19 |
| Vih_hys | SR | P | CMOS input buffer high voltage | With hysteresis enabled | 0.65×Vdde | Vdde+0.3 | V | D9.20 |
| Vil_hys | SR | P | CMOS input buffer low voltage | With hysteresis enabled | Vss–0.3 | 0.35×Vdde | V | D9.21 |
| Vih | SR | P | CMOS input buffer high voltage | With hysteresis disabled | 0.55×Vdde | Vdde+0.3 | V | D9.22 |
| Vil | SR | P | CMOS input buffer low voltage | With hysteresis disabled | Vss–0.3 | 0.40×Vdde | V | D9.23 |
| Vhys | SR | T | CMOS input buffer hysteresis | — | 0.1×Vdde | — | V | D9.24 |
| Pull_Ioh | SR | P | Weak pullup current | — | 35 | 135 | µA | D9.25 |
| Pull_Iol | SR | P | Weak pulldown current | — | 35 | 200 | µA | D9.26 |
| Iinact_d | SR | P | Digital pad input leakage current | Weak pull inactive | –2.5 | 2.5 | µA | D9.27 |
| Iinact_a | SR | P | Analog pad input leakage current | Weak pull inactive | –150 | 150 | nA | D9.28 |
| Voh | SR | P | Slew rate controlled output high voltage | — | 0.8×Vdde | — | V | D9.29 |
| Vol | SR | P | Slew rate controlled output low voltage | — | — | 0.2×Vdde | V | D9.30 |
| Voh_ls | SR | C | Low swing output pad output high voltage | — | 2.64 | — | V | D9.31 |
| Ioh_msr | SR | C | pad_msr_hv Ioh | — | 11.6 | 40.7 | mA | D9.32 |
| Iol_msr | SR | C | pad_msr_hv Iol | — | 17.7 | 68.2 | mA | D9.33 |
| Ioh_ssr | SR | C | pad_ssr_hv Ioh | — | 6.0 | 21.3 | mA | D9.34 |
| Iol_ssr | SR | C | pad_ssr_hv Iol | — | 9.2 | 36.3 | mA | D9.35 |
| Rtgate | SR | D | Pad_tgate_hv input resistance | — | 250 | 800 | Ω | D9.39 |

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### Table 27. DC electrical specifications

| Symbol | | Parameter | Condition | Value | | Unit | SpecID |
|--------|---|-----------|-----------|-------|-----|------|--------|
| | | | | Min | Max | | |
| Vdd | SR | Core supply voltage | — | 1.08 | 1.32 | V | D9.45 |
| Vdde | SR | I/O supply voltage | — | 3.0 | 3.6 | V | D9.46 |
| Vdd33 | SR | I/O pre-driver supply voltage | — | 3.0 | 3.6 | V | D9.47 |
| Vih_hys | SR | CMOS input buffer high voltage | With hysteresis enabled | $0.65\times$Vdde | Vdde+0.3 | V | D9.48 |
| Vil_hys | SR | CMOS input buffer low voltage | With hysteresis enabled | Vss$-$0.3 | $0.35\times$Vdde | V | D9.49 |
| Vih | SR | CMOS input buffer high voltage | With hysteresis disabled | $0.55\times$Vdde | Vdde+0.3 | V | D9.50 |
| Vil | SR | CMOS input buffer low voltage | With hysteresis disabled | Vss$-$0.3 | $0.40\times$Vdde | V | D9.51 |
| Vhys | SR | CMOS input buffer hysteresis | — | $0.1\times$Vdde | — | V | D9.52 |
| Pull_Ioh | SR | Weak pullup current | — | 15 | 70 | µA | D9.53 |
| Pull_Iol | SR | Weak pulldown current | — | 15 | 95 | µA | D9.54 |
| Iinact_d | SR | Digital pad input leakage current | Weak pull inactive | −2.5 | 2.5 | µA | D9.55 |
| Iinact_a | SR | Analog pad input leakage current | Weak pull inactive | −150 | 150 | nA | D9.56 |
| Voh | SR | Slew rate controlled output high voltage | — | $0.8\times$Vdde | — | V | D9.57 |
| Vol | SR | Slew rate controlled output low voltage | — | — | $0.2\times$Vdde | V | D9.58 |
| Ioh_msr | SR | pad_msr_hv Ioh | — | 5.4 | 21 | mA | D9.59 |
| Iol_msr | SR | pad_msr_hv Iol | — | 8.1 | 38.6 | mA | D9.60 |
| Ioh_ssr | SR | pad_ssr_hv Ioh | — | 2.8 | 11.2 | mA | D9.61 |
| Iol_ssr | SR | pad_ssr_hv Iol | — | 4.2 | 20.6 | mA | D9.62 |
| Rtgate | SR | Pad_tgate_hv input resistance | — | 325 | 1250 | Ω | D9.65 |

### Table 28. Supply leakage

| Pad | VDD | | VDDE | | VDD33 | |
|-----|-----|-----|------|-----|-------|-----|
| | Typ | Max | Typ | Max | Typ | Max |
| pad_msr_hv | 0.818 nA | 83.7 nA | 0.81 nA | 118 nA | — | — |
| pad ssr_hv | 0.818 nA | 83.7 nA | 0.858 nA | 88.7 nA | — | — |
| pad_i_hv | 0.307 nA | 48.4 nA | 88.2 pA | 30 nA | — | — |
| biasref_hv | — | — | — | — | — | — |

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**Table 28. Supply leakage (continued)**

| Pad | VDD | | VDDE | | VDD33 | |
|---|---|---|---|---|---|---|
| | **Typ** | **Max** | **Typ** | **Max** | **Typ** | **Max** |
| core_v_det_hv | 0 | 0 | — | — | 0 | 0 |
| core_v_det_lp_hv | 0 | 0 | — | — | — | — |
| corner_esdpadcell_hv | — | — | — | — | — | — |
| corner_esdpadcell_id00_hv | — | — | — | — | — | — |
| corner_esdpadcell_id11_hv | — | — | — | — | — | — |
| corner_esdpadcell_lp_hv | — | — | — | — | — | — |
| esd_term_35_84_hv | — | — | — | — | — | — |
| pad_9v_hv | 0 | 0 | — | — | — | — |
| pad_ae_hv | — | — | — | — | — | — |
| pad_esdspacer_hv | — | — | — | — | — | — |
| pad_tgate_hv | — | — | — | — | — | — |
| pad_vdd33_hv | — | — | — | — | — | — |
| pad_vdde_hv | 0 | 0 | — | — | 0 | 0 |
| pad_vddint3v_hv | 0 | 0 | — | — | 0 | 0 |
| pad_vddint_hv | 0 | 0 | — | — | — | — |
| pad_vss_hv | 0 | 0 | — | — | — | — |
| pad_vsse_hv | 0 | 0 | — | — | — | — |
| pad_vssint3v_hv | 0 | 0 | — | — | — | — |
| pad_vssint_hv | 0 | 0 | — | — | — | — |
| spcr_17_82_hv | — | — | — | — | — | — |
| spcr_35_84_hv | — | — | — | — | — | — |
| spcr_71_88_hv | — | — | — | — | — | — |
| spcr_143_38_hv | — | — | — | — | — | — |
| spcr_vdde_lvl_hv | — | — | — | — | — | — |

**Table 29. AVG IDDE specifications**

| Cell | Period (ns) | Load (pF)[1] | VDDE (V) | Drive/slew select | IDDE (mA) |
|---|---|---|---|---|---|
| pad_msr_hv[2] | 24 | 50 | 5.5 | 11 | 14 |
| | 62 | 50 | 5.5 | 01 | 5.3 |
| | 317 | 50 | 5.5 | 00 | 1.1 |
| | 425 | 200 | 5.5 | 00 | 3 |

**Table 29. AVG IDDE specifications (continued)**

| Cell | Period (ns) | Load (pF)[1] | VDDE (V) | Drive/slew select | IDDE (mA) |
|---|---|---|---|---|---|
| pad_ssr_hv[2] | 37 | 50 | 5.5 | 11 | 9 |
| | 130 | 50 | 5.5 | 01 | 2.5 |
| | 650 | 50 | 5.5 | 00 | 0.5 |
| | 840 | 200 | 5.5 | 00 | 1.5 |

[1] All loads are lumped loads.

[2] Average current is for pad configured as output only. Use pad_i current for input.

## 4.8.3 DC specification for CMOS090_ddr library @ VDDE = 3.3 V

**Table 30. DC electrical specifications at 3.3 V VDDE**

| Symbol | | Parameter | Value | | Unit | SpecID |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Vdd | SR | Core supply voltage | 1.08 | 1.32 | V | D9.71 |
| Vdde | SR | I/O supply voltage | 3.0 | 3.6 | V | D9.72 |
| Vdd33 | SR | I/O pre-driver supply voltage | 3.0 | 3.6 | V | D9.73 |
| Vref | SR | Input reference voltage | 1.3 | 1.7 | V | D9.74 |
| Vtt | SR | Termination voltage | Vref−0.05 | Vref+0.05 | V | D9.75 |
| Vih | SR | Input high voltage | Vref+0.20 | — | V | D9.76 |
| Vil | SR | Input low voltage | — | Vref−0.2 | V | D9.77 |
| Voh | SR | Output high voltage | Vtt+0.8 | — | V | D9.78 |
| Vol | SR | Output low voltage | — | Vtt−0.8 | V | D9.79 |

**Table 31. Output drive current @ VDDE = 3.3 V (+/-10%)**

| Pad | C | Drive mode | Minimum Ioh (mA) | Minimum Iol (mA) |
|---|---|---|---|---|
| pad_st_acc | D | 111 | −16 | 16 |
| pad_st_dq | D | 111 | −16 | 16 |
| pad_st_clk | D | 111 | −16 | 16 |
| pad_st | D | 111 | −16 | 16 |
| pad_st_odt | D | 111 | −16 | 16 |
| pad_st_ck | D | 111 | −16 | 16 |

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## 4.8.4    DC specification for CMOS090_ddr library @ VDDE = 2.5 V

**Table 32. DC electrical specifications at 2.5 V VDDE**

| Symbol | | C | Parameter | Value | | Unit | SpecID |
|--------|----|---|-----------|-------|-----|------|--------|
| | | | | Min | Max | | |
| Vdd | SR | P | Core supply voltage | 1.08 | 1.32 | V | D9.80 |
| Vdde | SR | P | I/O supply voltage | 2.3 | 2.7 | V | D9.81 |
| Vdd33 | SR | P | I/O pre-driver supply voltage | 3.0 | 3.6 | V | D9.82 |
| Vref | SR | P | Input reference voltage | 0.49×Vdde | 0.51×Vdde | V | D9.83 |
| Vtt | SR | P | Termination voltage | Vref–0.04 | Vref+0.04 | V | D9.84 |
| Vih | SR | P | Input high voltage | Vref+0.15 | — | V | D9.85 |
| Vil | SR | P | Input low voltage | — | Vref–0.15 | V | D9.86 |
| Voh | SR | P | Output high voltage | Vtt+0.81 | — | V | D9.87 |
| Vol | SR | P | Output low voltage | — | Vtt–0.81 | V | D9.88 |

**Table 33. Output drive current @ VDDE = 2.5 V (+/-200mV)**

| Pad | C | Drive mode | Minimum Ioh (mA) | Minimum Iol (mA) | Libraries |
|-----|---|-----------|------------------|------------------|-----------|
| pad_st_acc | D | 011 | −16.2 | 16.2 | 6MDDR |
| pad_st_dq | D | 011 | −16.2 | 16.2 | 6MDDR |
| pad_st_ck | D | 011 | −16.2 | 16.2 | 6MDDR |

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## 4.8.5 DC specification for CMOS090_ddr library @ VDDE = 1.8 V

**Table 34. DC electrical specifications for 1.8 V VDDE**

| Symbol | C | | Parameter | Value | | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Vdd | SR | P | Core supply voltage | 1.08 | 1.32 | V | D9.89 |
| Vdde | SR | P | I/O supply voltage | 1.7 | 1.9 | V | D9.90 |
| Vdd33 | SR | P | I/O pre-driver supply voltage | 3.0 | 3.6 | V | D9.91 |
| Vref | SR | P | Input reference voltage | 0.49×Vdde | 0.51×Vdde | V | D9.92 |
| Vtt | SR | P | Termination voltage | Vref–0.04 | Vref+0.04 | V | D9.93 |
| Vih | SR | P | Input high voltage | Vref+0.125 | — | V | D9.94 |
| Vil | SR | P | Input low voltage | — | Vref–0.125 | V | D9.95 |
| Voh | SR | P | Output high voltage | Vtt+0.81 | — | V | D9.96 |
| Vol | SR | P | Output low voltage | — | Vtt–0.81 | V | D9.97 |

**Table 35. Output drive current @ VDDE = 1.8 V (+/-100mV)**

| Pad | | Drive mode | Minimum Ioh (mA) | Minimum Iol (mA) | Libraries |
|---|---|---|---|---|---|
| pad_st_acc | D | 000 | –3.57 | 3.57 | 6MDDR |
| | | 001 | –7.84 | 7.84 | |
| | | 010 | –5.36 | 5.36 | |
| | | 110 | –13.4 | 13.4 | |
| pad_st_dq | D | 000 | –3.57 | 3.57 | 6MDDR |
| | | 001 | –7.84 | 7.84 | |
| | | 010 | –5.36 | 5.36 | |
| | | 110 | –13.4 | 13.4 | |
| pad_st_clk | D | 000 | –3.57 | 3.57 | 6MDDR |
| | | 001 | –7.84 | 7.84 | |
| | | 010 | –5.36 | 5.36 | |
| | | 110 | –13.4 | 13.4 | |

### Table 36. ODT DC electrical characteristics

| Symbol | | C | Parameter | Condition | Value | | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| Rtt | SR | C | Effective impedance value | Rainbow supports only 150 ohm termination and that can be enabled by enabling any bit of the termination control register (all of them are OR'ed). | 120 | 150 | 180 | Ω | D9.98 |

### Table 37. core_v_det_odt and core_v_det33_odt specifications

| VDDE | C | VDD | Vtrip max (V) | Vtrip min | Hysteresis min (V) |
|---|---|---|---|---|---|
| 3.5 | C | Rising | 0.79 | 0.44 | 0.07 |
| | C | Falling | 0.56 | 0 | |
| 1.62 | C | Rising | 0.65 | 0.3 | 0.16 |
| | C | Falling | 0.33 | 0 | |
| Rising | C | 0.0 | 1.40 | 0.3 | — |

## 4.8.6    SMD Characteristics

### Table 38. SMD pad electrical characteristics

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IL}$ | CC | P | Low level input voltage | — | −0.4 | — | $0.35 \times V_{DDM}$ | V |
| $V_{IH}$ | CC | P | High level input voltage | — | $0.65 \times V_{DDM}$ | — | $V_{DDM}+0.4$ | |
| $V_{HYST}$ | CC | C | Schmitt trigger hysteresis | — | $0.1 \times V_{DDM}$ | — | — | |
| $V_{OL}$ | CC | P | Low level output voltage | $I_{OL}$ = 20 mA[1] | — | — | 0.32 | |
| | | | | $I_{OL}$ = 30 mA[2] | — | — | 0.48 | |
| $V_{OH}$ | CC | P | High level output voltage | $I_{OH}$ = −20 mA[1] | $V_{DDM}$−0.32 | — | — | |
| | | | | $I_{OH}$ = −30 mA[2] | $V_{DDM}$−0.48 | — | — | |

**Table 38. SMD pad electrical characteristics (continued)**

| Symbol | C | | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{PU}$ | CC | P | Internal pull-up device current | $V_{in}=V_{IL}$ | −130 | — | — | µA |
| | | | | $V_{in}=V_{IH}$ | — | — | 0 | |
| $I_{PD}$ | CC | P | Internal pull-down device current | $V_{in}=V_{IL}$ | 0 | — | — | |
| | | | | $V_{in}=V_{IH}$ | — | — | 130 | |
| $I_{IN}$ | CC | P | Input leakage current | — | −1 | — | 1 | |
| $R_{DSONH}$ | CC | C | SMD pad driver active high impedance | $I_{OH} \leq -30$ mA[2] | — | — | 16 | Ω |
| $R_{DSONL}$ | CC | C | SMD pad driver active low impedance | $I_{OL} \leq 30$ mA[2] | — | — | 16 | Ω |
| $V_{OMATCH}$ | CC | C | Output driver matching $V_{OH} / V_{OL}$ | $I_{OH} / I_{OL} \leq 30$ mA[2] | — | — | 90 | mV |

[1]  VDD = 5.0 V ±10%, Tj = −40 to +140 °C.

[2]  VDD = 5.0 V ±10%, Tj = −40 to +120 °C.



**Figure 7. Pad output delay**

**MPC5645S Microcontroller Data Sheet, Rev. 14**
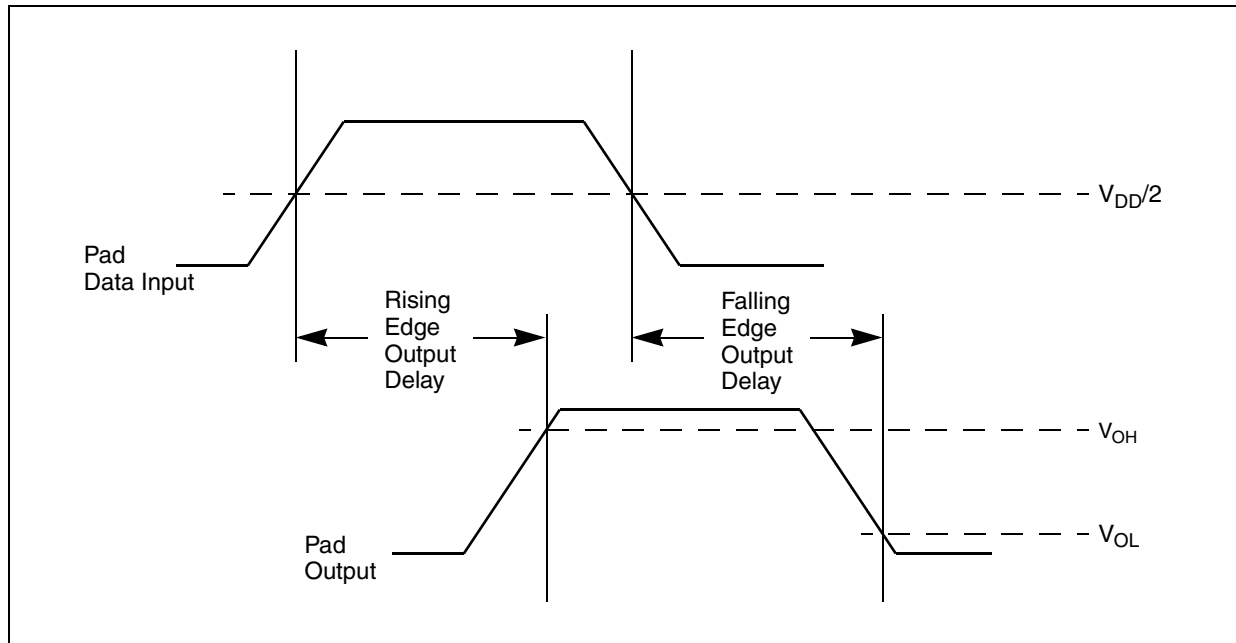
**Table 39. SMD pad delays**

| Symbol | C | | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| — | CC | D | SMD pad delay | CL=50pf $V_{DD}$=5V±10% SRE=1 | — | — | 165 | ns |
| | | | | CL=50pf $V_{DD}$=5V±10% SRE=0 | — | — | 35 | ns |
| — | CC | D | SMD pad delay | CL=50pf $V_{DD}$=3.3V±10% SRE=1 | — | — | 350 | ns |
| | | | | CL=50pf $V_{DD}$=3.3V±10% SRE=0 | — | — | 50 | ns |

# 4.9    SSD Characteristics

**Table 40. SSD electrical characteristics**

| Symbol | C | | Parameter | Value[1] | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{VREF}$ | CC | P | Reference voltage ($I_{VREF}$ = 0) | $V_{DDM}$/2 – 0.03 | $V_{DDM}$/2 | $V_{DDM}$/2 + 0.03 | V |
| $I_{VREF}$ | CC | P | Reference voltage output current | 1.85 | — | — | mA |
| $R_{IN}$ | CC | D | Input resistance (against $V_{DDM}$/2) | 0.8 | 1.0 | 1.2 | MΩ |
| $V_{IN}$ | CC | C | Input common mode range | $V_{SSM}$ | — | $V_{DDM}$ | V |
| $SSD_{CONST}$ | CC | C | SSD constant | 0.549 | 0.572 | 0.597 | — |
| $SSD_{OFFSET}$ | CC | C | SSD offset (unipolar, $N_{sample}$ = 256) | –9 | — | 9 | counts |
| | | | SSD offset (bipolar, $N_{sample}$ = 256) | –8 | — | 8 | |
| | | | SSD offset (bipolar with offset cancellation, $N_{sample}$ = 256) | –5 | — | 5 | |
| $f_{SSDSMP}$ | CC | D | SSD cmpout sample rate | 0.5 | — | 2.0 | MHz |

[1]  Vdd = 5.0V ±10%, Tj = –40 to +140 °C.

# 4.10    $\overline{RESET}$ electrical characteristics

The device implements a dedicated bidirectional RESET pin.
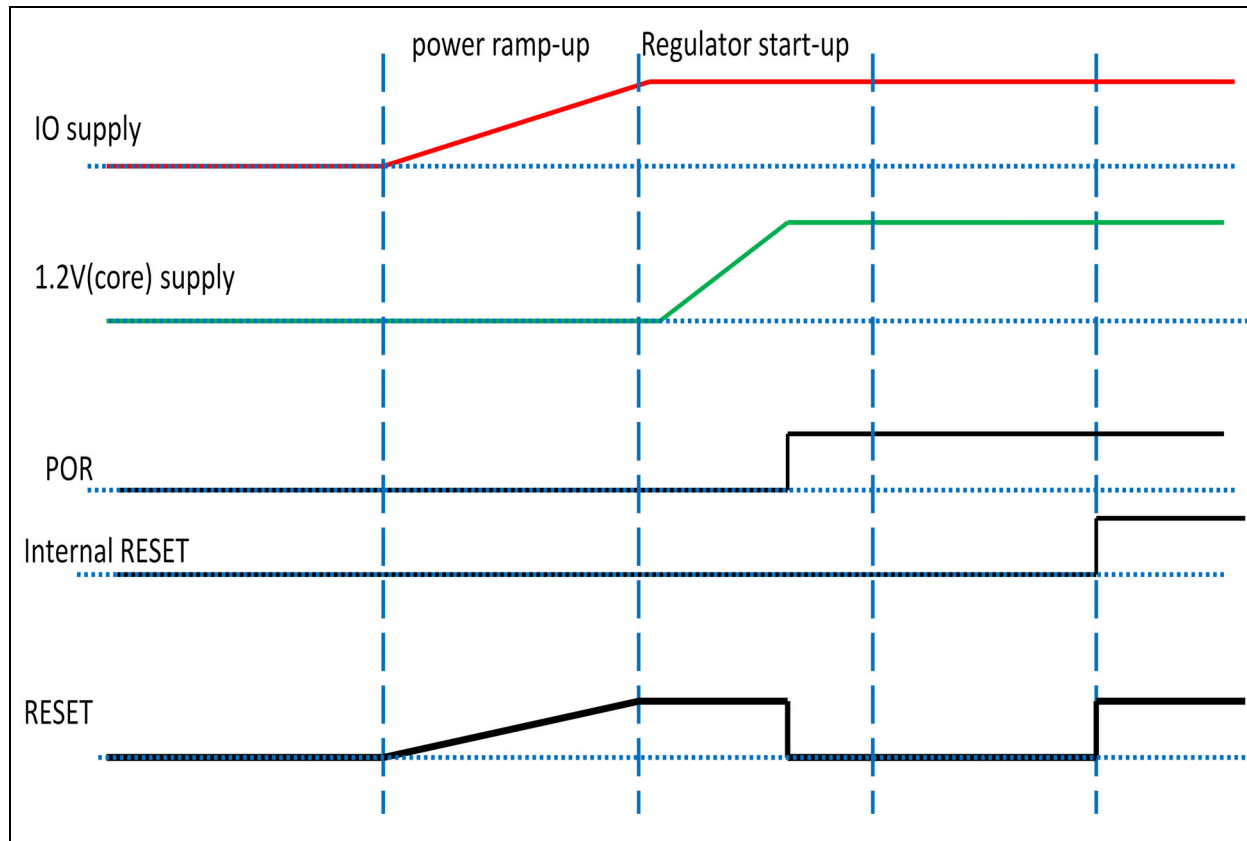
**Figure 8. Startup reset requirements**
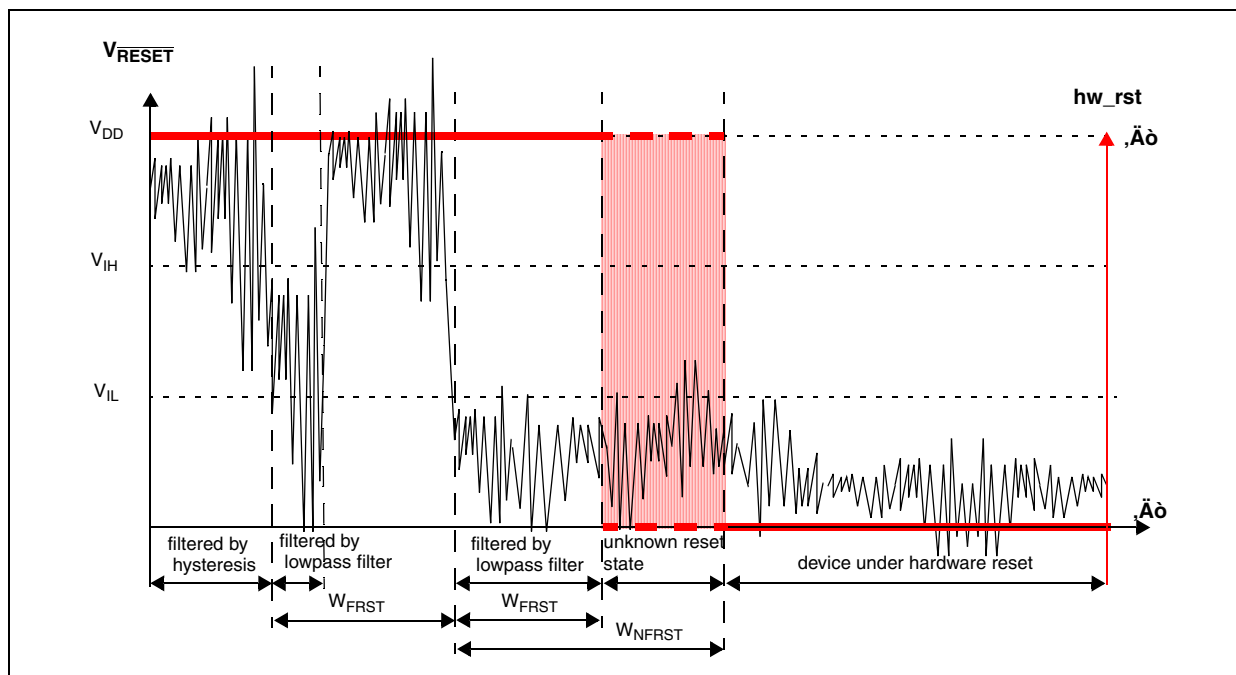


**Figure 9. Noise filtering on reset signal**

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**Table 41. Reset electrical characteristics**

| Symbol | C | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|--------|---|-----------|---------------|-----|-----|-----|------|--------|
| | | | | Min | Typ | Max | | |
| $V_{IH}$ | SR | P | Input High Level CMOS Schmitt Trigger | — | $0.65V_{DD}$ | — | $V_{DD}$+0.4 | V | D8.1 |
| $V_{IL}$ | SR | P | Input low Level CMOS Schmitt Trigger | — | -0.4 | — | $0.35V_{DD}$ | V | D8.2 |
| $V_{HYS}$ | CC[3] | D | Input hysteresis CMOS Schmitt Trigger | — | $0.1V_{DD}$ | — | — | V | D8.3 |
| $V_{OL}$ | CC[4] | P | Output low level | Push Pull, $I_{OL}$ = 2mA, $V_{DD}$ = 5.0V ± 10%, ipp_hve = 0 (recommended) | — | — | $0.1V_{DD}$ | V | D8.4 |
| | | D | | Push Pull, $I_{OL}$ = 1mA, $V_{DD}$ = 5.0V ± 10%, ipp_hve = 1[5] | — | — | $0.1V_{DD}$ | | |
| | | C | | Push Pull, $I_{OL}$ = 1mA, $V_{DD}$ = 3.3V ± 10%, ipp_hve = 1 (recommended) | — | — | 0.5 | | |
| $T_{tr}$ | CC[4] | T | Output transition time output pin[6] MEDIUM configuration | $C_L$ = 25pF, $V_{DD}$ = 5.0V ± 10%, ipp_hve = 0 | — | — | 10 | ns | D8.5 |
| | | | | $C_L$ = 50pF, $V_{DD}$ = 5.0V ± 10%, ipp_hve = 0 | — | — | 20 | | |
| | | | | $C_L$ = 100pF, $V_{DD}$ = 5.0V ± 10%, ipp_hve = 0 | — | — | 40 | | |
| | | | | $C_L$ = 25pF, $V_{DD}$ = 3.3V ± 10%, ipp_hve = 1 | — | — | 12 | | |
| | | | | $C_L$ = 50pF, $V_{DD}$ = 3.3V ± 10%, ipp_hve = 1 | — | — | 25 | | |
| | | | | $C_L$ = 100pF, $V_{DD}$ = 3.3V ± 10%, ipp_hve = 1 | — | — | 40 | | |
| $W_{FRST}$ | SR | T | $\overline{RESET}$ Input Filtered Pulse | — | — | — | 70 | ns | D8.6 |
| $W_{NFRST}$ | SR | T | $\overline{RESET}$ Input Not Filtered Pulse | — | 400 | — | — | ns | D8.7 |
| $|I_{WPU}|$ | CC[4] | T | Weak pull-up current absolute value | — | 10 | — | — | µA | D8.8 |

[1] $V_{DD}$ = 3.3V ± 10% / 5.0V ± 10%, $T_A$ = -40 / +105°C, unless otherwise specified.

[2] All values need to be confirmed during device validation.

[3] Data based on characterization results, not tested in production.

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Guaranteed by design simulation.

<sup>5</sup> This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the reference manual).

<sup>6</sup> $C_L$ calculation should include device and package capacitance ($C_{PKG} < 5pF$).

# 4.11 Fast external crystal oscillator (4–16 MHz) electrical characteristics

This device implements the fast external oscillator (FXOSC) using a low power Loop Controlled Pierce Oscillator (LCP) configuration.

**Table 42. Fast external crystal oscillator electrical characteristics**

| Symbol | | Parameter | Conditions | Value | | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| $f_{OSC}$ | C | Crystal oscillator range | Loop controlled Pierce | 4.0 | — | 16 | MHz | O9.1 |
| $i_{OSC}$ | D | Startup current | — | 100 | — | — | µA | O9.2 |
| $t_{UPOSC}$ | C | Oscillator start-up time | Loop controlled Pierce | — | 4[1] | 50[2] | ms | O9.3 |
| $t_{CQOUT}$ | D | Clock quality check time-out | — | 0.45 | | 2.5 | s | O9.4 |
| $f_{CMFA}$ | D | Clock monitor failure assert frequency | — | 200 | 400 | 800 | kHz | O9.5 |
| $f_{EXT}$ | D | External square wave input frequency[2] | — | 2.0 | — | 50 | MHz | O9.6 |
| $t_{EXTL}$ | D | External square wave pulse width low | — | 9.5 | — | — | ns | O9.7 |
| $t_{EXTH}$ | D | External square wave pulse width high | — | 9.5 | — | — | ns | O9.8 |
| $t_{EXTR}$ | D | External square wave rise time | — | — | — | 1 | ns | O9.9 |
| $t_{EXTF}$ | D | External square wave fall time | — | — | — | 1 | ns | O9.10 |
| $C_{IN}$ | D | Input capacitance | EXTAL and XTAL pins | — | 7 | — | pF | O9.11 |
| $V_{IH,EXTAL}$ | P | EXTAL pin input high voltage[2] | — | $0.75\times V_{DDPLL}$ | — | — | V | O9.12 |
| | T | | | — | — | $V_{DDPLL}+0.3$ | | |
| $V_{IL,EXTAL}$ | P | EXTAL pin input low voltage[2] | — | — | — | $0.25\times V_{DDPLL}$ | V | O9.13 |
| | T | | | $V_{SSPLL}-0.3$ | — | — | | |
| $V_{HYS,EXTAL}$ | C | EXTAL pin input hysteresis[2] | — | — | 180 | — | mV | O9.14 |
| $V_{PP,EXTAL}$ | C | EXTAL pin oscillation amplitude | Loop controlled Pierce | — | 1.0 | — | V | O9.15 |

<sup>1</sup> $f_{OSC}$ = 4 MHz, C = 22 pF.

<sup>2</sup> Maximum value is for extreme cases using high Q, low frequency crystals.

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## 4.12 Slow external crystal oscillator (32 KHz) electrical characteristics

The device provides a slow external oscillator/resonator driver (SXOSC).
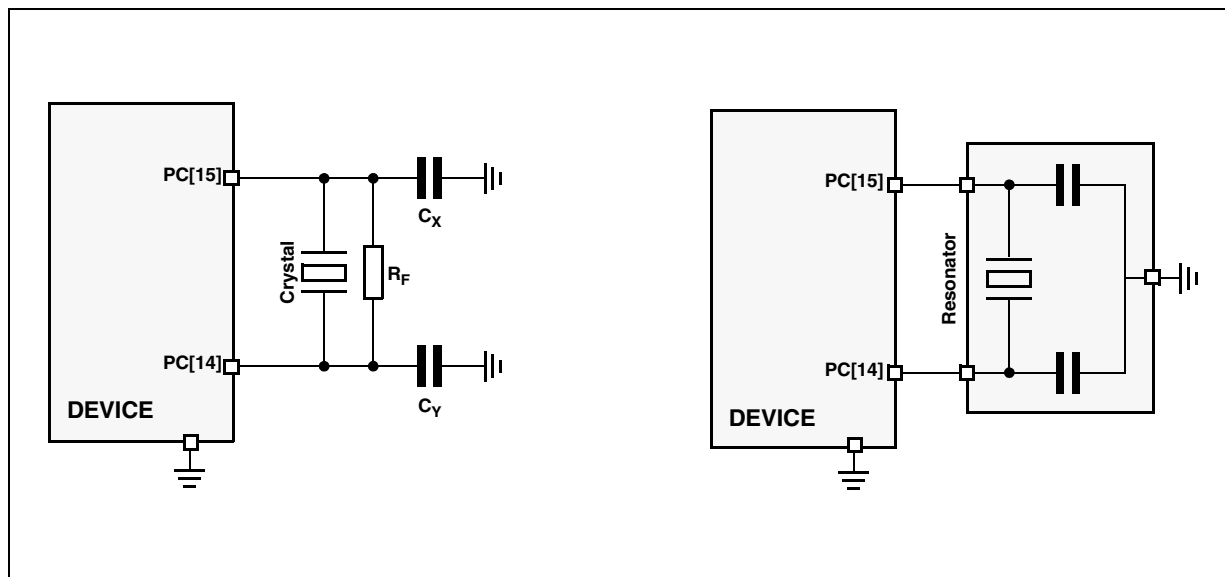


**Figure 10. Crystal oscillator and resonator connection scheme**

### NOTE
PC[14]/PC[15] must not be directly used to drive external circuits.
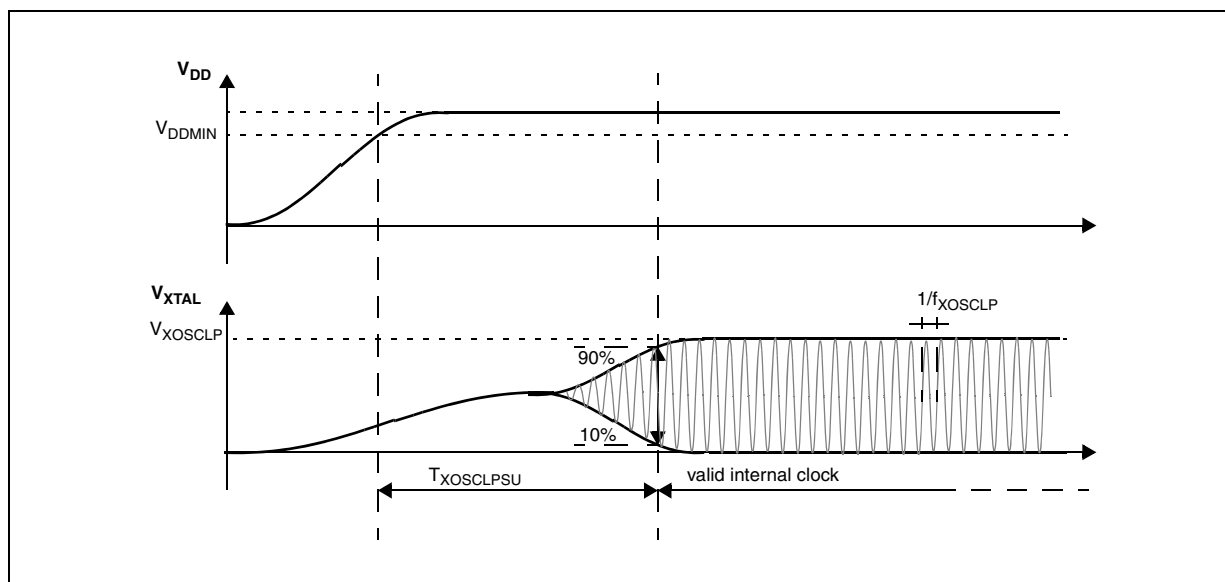


**Figure 11. Slow external crystal oscillator electrical characteristics**

**Table 43. Slow external crystal oscillator electrical characteristics**

| Symbol | C | | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| $f_{XOSCLP}$ | SR | C | Oscillator frequency | — | 32 | — | 40 | kHz | O10.1 |
| $V_{XOSCLP}$ | CC[3] | C | Oscillation amplitude | $V_{DDA}$=3.3V±10%, $V_{DDE\_A}$=3.3V±10% | 1.12 | 1.33 | 1.74 | V | O10.2 |
| | | | | $V_{DDA}$=5.0V±10%, $V_{DDE\_A}$=5.0V±10% | 1.12 | 1.37 | 1.74 | | |
| $I_{XOSCLP}$ | CC[3] | D | Oscillator consumption | — | — | — | 5 | µA | O10.3 |
| $T_{XOSCLPSU}$ | CC[3] | D | Oscillator start-up time | — | — | — | 2 | s | O10.4 |
| $V_{IH}$ | SR | C | Input high level CMOS Schmitt Trigger | Oscillator bypass mode | 0.65$V_{DDA}$ 0.65$V_{DDE\_A}$ | — | $V_{DDA}$+0.4 $V_{DDE\_A}$+0.4 | V | O10.5 |
| $V_{IL}$ | SR | C | Input low level CMOS Schmitt Trigger | Oscillator bypass mode | $V_{SS}$–0.4 | — | 0.35$V_{DDA}$ 0.35$V_{DDE\_A}$ | V | O10.6 |

[1]  $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = -40 to +105 °C, unless otherwise specified.
[2]  All values need to be confirmed during device validation.
[3]  Granted by device validation.

# 4.13  FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the fast external oscillator driver.

**Table 44. FMPLL electrical characteristics**

| Symbol | C | | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| $f_{PLLIN}$ | SR | T | PLL reference clock[3] | — | 4 | — | 120 | MHz | O11.1 |
| $\Delta_{PLLIN}$ | SR | T | PLL reference clock duty cycle[3] | — | 47.5 | — | 52.5 | % | O11.2 |
| $f_{PLLOUT}$ | CC[4] | T | PLL output clock frequency | — | 15 | — | 250[5] | MHz | O11.3 |
| $f_{CPU}$ | CC[4] | T | System clock frequency | — | — | — | 125[6] | MHz | O11.4 |
| $T_{LOCK}$ | CC[4] | T | PLL lock time | Stable oscillator ($f_{PLLIN}$ = 10 MHz) | — | — | 100 | µs | O11.5 |
| $\Delta T_{PKJIT}$ | CC[4] | T | PLL jitter | $f_{PLLOUT}$ (PHI i.e. FMPLL O/P) = 15.625 MHz @ 10 MHz resonator | –509 | — | 509 | ps | O11.6 |
| $\Delta T_{LTJIT}$ | CC[4] | T | PLL long term jitter | $f_{PLLIN}$ = 10 MHz (resonator) | –2.4 | — | 2.4 | ns | O11.7 |
| $I_{PLL}$ | CC[7] | D | Current Consumption (Normal Mode for Analog Supply) | $T_A$ = 25°C | — | — | 500 | µA | O11.8 |

[1]  $V_{DDPLL}$ = 1.2 V ± 10%, $T_A$ = -40 to +105 °C, unless otherwise specified.
[2]  All values need to be confirmed during device validation.
[3]  PLLIN clock retrieved directly from XOSCHS clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify $f_{PLLIN}$ and $\Delta_{PLLIN}$.

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[4] Data based on device simulation.

[5] 2x sys clock required for generation of DDR timing.

[6] $f_{CPU}$ of 125 MHz can be achieved only at temperatures up to 105 °C with a maximum FM depth of 2%.

[7] Data based on characterization results, not tested in production

## 4.14 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

**Table 45. Fast internal oscillator electrical characteristics**

| Symbol | C | | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| $f_{RCM}$ | CC[3] | P | RC oscillator high frequency | $T_A$ = 25 °C, trimmed | — | 16 | — | MHz | O12.1 |
| $I_{RCMRUN}$ | CC[3] | D | RC oscillator high frequency current in running mode | $T_A$ = 25 °C, trimmed | — | — | 200 | µA | O12.2 |
| $I_{RCMPWD}$ | CC[3] | D | RC oscillator high frequency current in power down mode | $T_A$ = 25 °C | — | — | 10 | µA | O12.3 |
| $\Delta RCMVAR$ | CC[4] | C | RC oscillator variation in temperature and supply with respect to $f_{RC}$ at $T_A$ = 55 °C in high-frequency configuration | — | –5 | — | +5 | % | O12.5 |

[1] $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = -40 to +105 °C, unless otherwise specified.

[2] All values need to be confirmed during device validation.

[3] Guaranteed by device simulation, not tested in production.

[4] Guaranteed by device characterization, not tested in production.

## 4.15 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

**Table 46. Slow internal RC oscillator electrical characteristics**

| Symbol | C | | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| $f_{RCL}$ | CC[3] | P | RC oscillator low frequency | $T_A$ = 25 °C, trimmed | — | 128 | — | kHz | O13.1 |
| $I_{RCL}$ | CC[3] | D | RC oscillator low frequency current | $T_A$ = 25 °C, trimmed | — | — | 5 | µA | O13.2 |
| $\Delta RCLVAR$ [3] | CC[3] | C | RC oscillator variation in temperature and supply with respect to $f_{RC}$ at $T_A$ = 55 °C in high frequency configuration | High frequency configuration | –10 | — | +10 | % | O13.4 |

[1] $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = -40 to +105 °C, unless otherwise specified.

[2] All values need to be confirmed during device validation.

[3] Guaranteed by device simulation, not tested in production

## 4.16 Flash memory electrical characteristics

**Table 47. Program and erase specifications**

| Symbol | C | Parameter | Min Value | Typical Value[1] | Initial Max[2] | Max[3] | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| $T_{dwprogram}$ | C | Double Word (64 bits) Program Time[4] | — | — | 22 | 500 | µs | D14.1 |
| $T_{16kpperase}$ | C | 16 KB Block Pre-program and Erase Time | — | — | 1000 | 5000 | ms | D14.2 |
| $T_{64kpperase}$ | C | 64 KB Block Pre-program and Erase Time | — | — | 1800 | 5000 | ms | D14.3 |
| $T_{128kpperase}$ | C | 128 KB Block Pre-program and Erase Time | — | — | 2600 | 7500 | ms | D14.4 |
| $T_{256kpperase}$ | C | 256 KB Block Pre-program and Erase Time | — | — | 5200 | 15000 | ms | D14.5 |

[1] Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

[2] Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

[3] The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

[4] Actual hardware programming times. This does not include software overhead.

**Table 48. Flash module life**

| Symbol | C | Parameter | Conditions | Value Min | Value Typ | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| P/E | C | Number of program/erase cycles per block for 16 KB, 48KB and 64KB blocks, across full operating temperature range (Tj) | — | 100,000 | — | P/E cycles | D14.6 |
| P/E | C | Number of program/erase cycles per block for 128KB and 256KB blocks, across full operating temperature range (Tj) | — | 1, 000 | 100,000 | P/E cycles | D14.7 |
| Data retention | C | Minimum data retention at 85 °C average ambient temperature[1] | Blocks with 0 - 1,000 P/E cycles | 20 | — | Years | D14.8 |
| | | | Blocks with 1,001 - 10,000 P/E cycles | 10 | — | Years | |
| | | | Blocks with 10,001 - 100,000 P/E cycles | 5 | — | Years | |

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

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## 4.17 ADC parameters

The device provides a 10-bit Successive Approximation Register (SAR) Analog to Digital Converter.
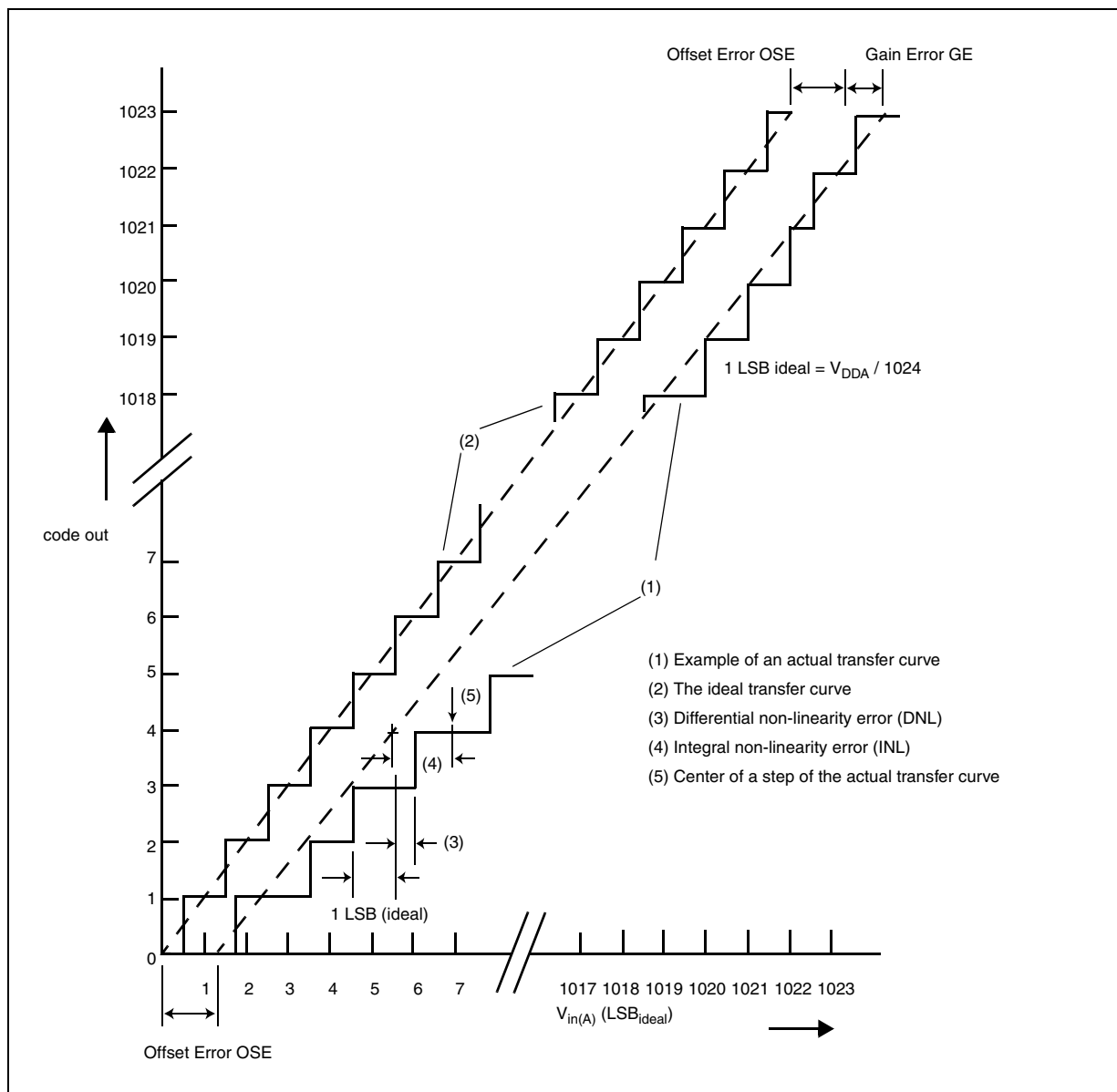


**Figure 12. ADC Characteristics and Error Definitions**

## 4.17.1    Input Impedance and ADC Accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: $C_S$ being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S$ equal to 3 pF, a resistance of 330k$\Omega$ is obtained ($R_{EQ}$ = 1 / (fc*$C_S$)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S$) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 5:

*Eqn. 5*

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 5 generates a constraint for external network design, in particular on resistive path. Internal switch resistances ($R_{SW}$ and $R_{AD}$) can be neglected with respect to external resistances.



$R_S$      Source Impedance
$R_F$      Filter Resistance
$C_F$      Filter Capacitance
$R_L$      Current Limiter Resistance
$R_{SW1}$  Channel Selection Switch Impedance
$R_{AD}$   Sampling Switch Impedance
$C_P$      Pin Capacitance (two contributions, $C_{P1}$ and $C_{P2}$)
$C_S$      Sampling Capacitance
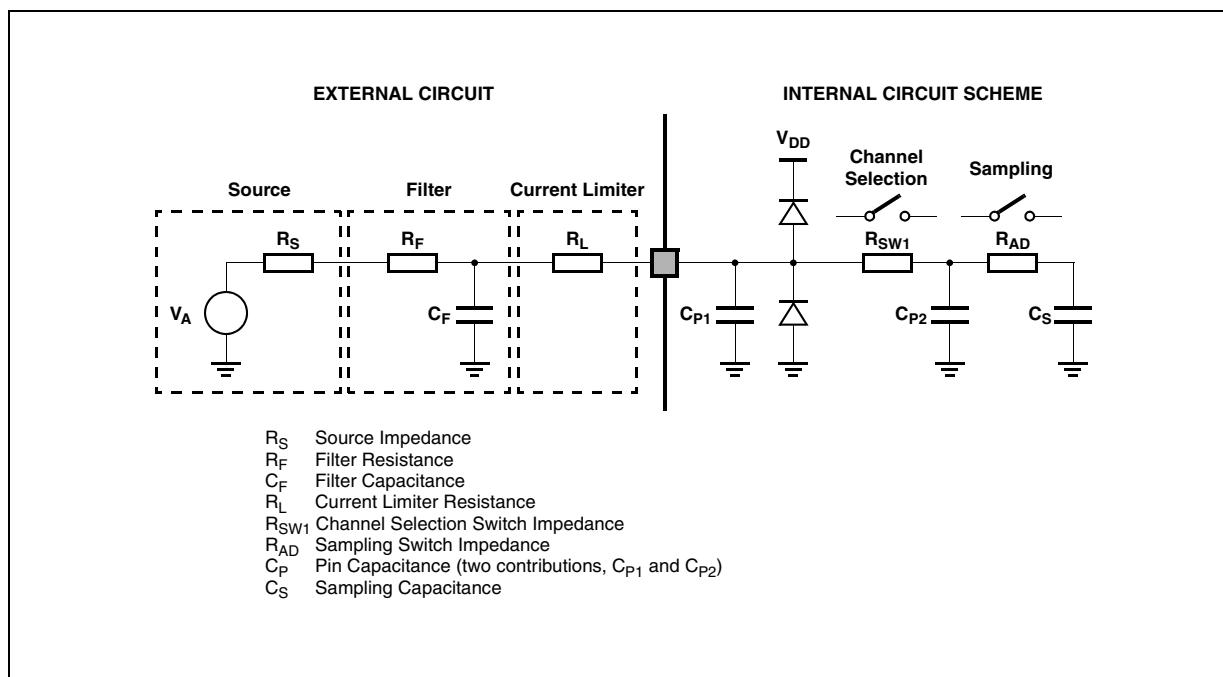
**Figure 13. Input Equivalent Circuit (Precise Channels)**
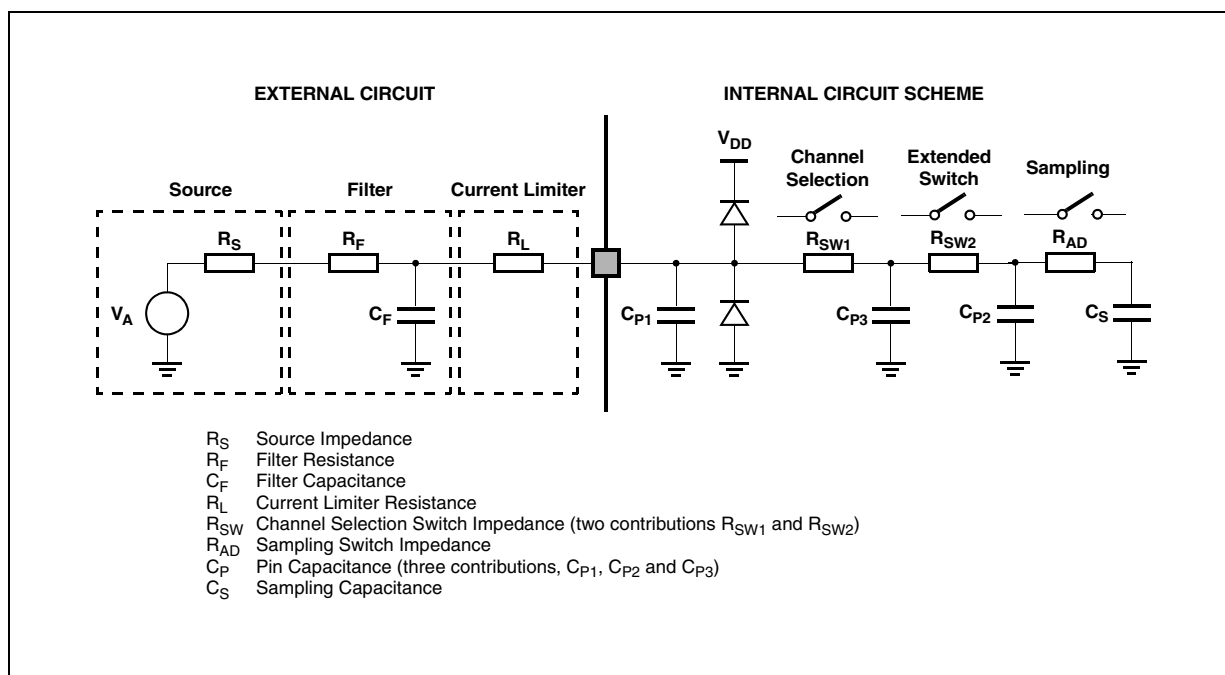
**Figure 14. Input Equivalent Circuit (Extended Channels)**

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances $C_F$, $C_{P1}$ and $C_{P2}$ are initially charged at the source voltage $V_A$ (refer to the equivalent circuit reported in Figure 13): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).
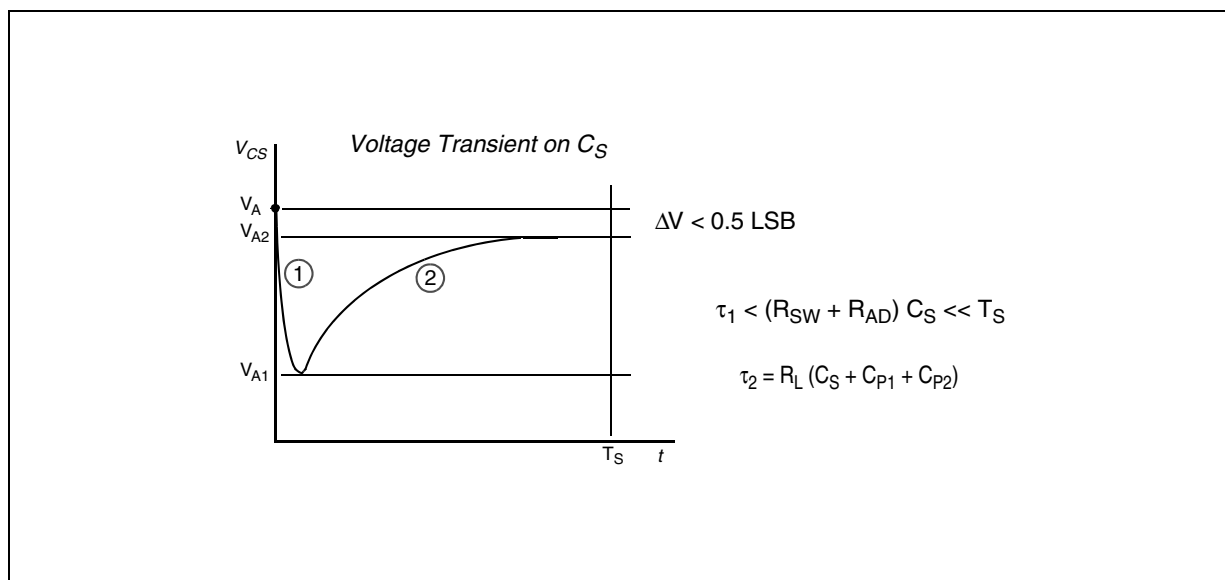


**Figure 15. Transient Behavior during Sampling Phase**

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance $C_{P1}$ and $C_{P2}$ to the sampling capacitance $C_S$ occurs ($C_S$ is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which $C_{P2}$ is reported in parallel to $C_{P1}$ (call $C_P = C_{P1} + C_{P2}$), the two capacitances $C_P$ and $C_S$ are in series, and the time constant is

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$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

Equation 6 can again be simplified considering only $C_S$ as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time $T_S$ is always much longer than the internal time constant:

*Eqn. 7*

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

The charge of $C_{P1}$ and $C_{P2}$ is redistributed also on $C_S$, determining a new value of the voltage $V_{A1}$ on the capacitance according to Equation 8:

*Eqn. 8*

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

- A second charge transfer involves also $C_F$ (that is typically bigger than the on-chip capacitance) through the resistance $R_L$: again considering the worst case in which $C_{P2}$ and $C_S$ were in parallel to $C_{P1}$ (since the time constant in reality would be faster), the time constant is:

*Eqn. 9*

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time $T_S$, a constraints on $R_L$ sizing is obtained:

*Eqn. 10*

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, $R_L$ shall be sized also according to the current limitation constraints, in combination with $R_S$ (source impedance) and $R_F$ (filter resistance). Being $C_F$ definitively bigger than $C_{P1}$, $C_{P2}$ and $C_S$, then the final voltage $V_{A2}$ (at the end of the charge transfer transient) will be much higher than $V_{A1}$. Equation 11 must be respected (charge balance assuming now $C_S$ already charged at $V_{A1}$):

*Eqn. 11*

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on $C_S$ with respect to the ideal source $V_A$; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time ($T_S$). The filter is typically designed to act as anti-aliasing.
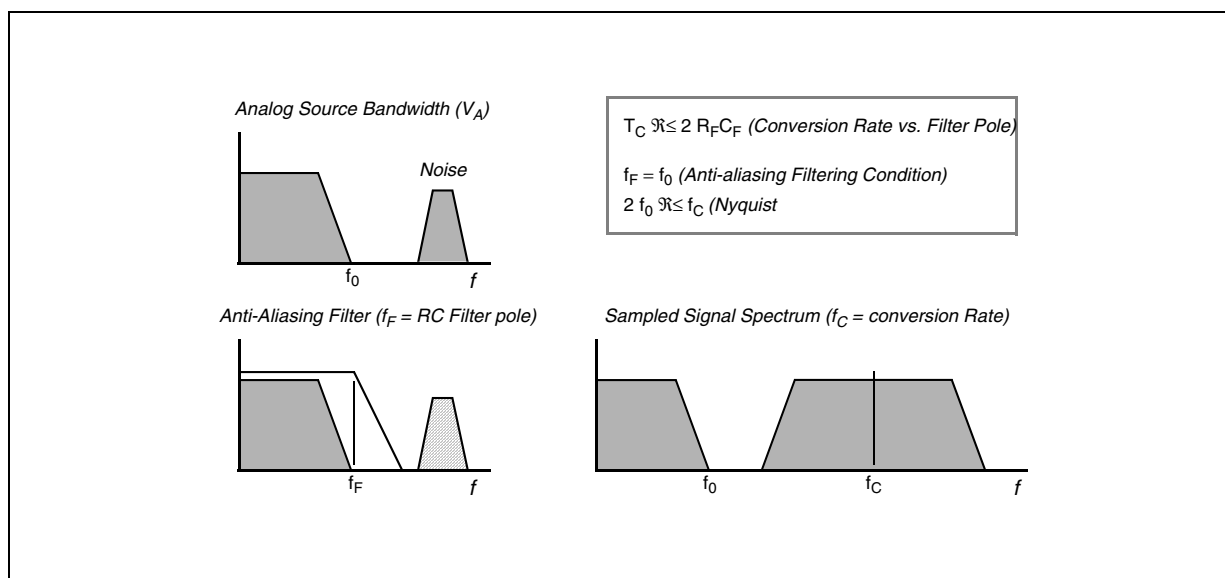
**Figure 16. Spectral Representation of Input Signal**

Calling $f_0$ the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, $f_F$), according to the Nyquist theorem the conversion rate $f_C$ must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period ($T_C$). Again the conversion period $T_C$ is longer than the sampling time $T_S$, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time $T_S$, so the charge level on $C_S$ cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on $C_S$; from the two charge balance equations above, it is simple to derive Equation 12 between the ideal and real sampled voltage on $C_S$:

*Eqn. 12*

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when $V_A$ is maximum, that is for instance 5V), assuming to accept a maximum error of half a count, a constraint is evident on $C_F$ value:

*Eqn. 13*

$$C_F > 2048 \bullet C_S$$

## 4.17.2   ADC electrical characteristics

**Table 49. ADC electrical characteristics**

| Symbol | C | Parameter | Conditions[1] | Value[2] Min | Value[2] Typ | Value[2] Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| $V_{SSA}$ | SR D | Voltage on VSSA (ADC reference) pin with respect to ground ($V_{SS}$)[3] | — | -0.1 | — | 0.1 | V | D15.1 |
| $V_{DDA}$ | SR D | Voltage on VDDA pin (ADC reference) with respect to ground ($V_{SS}$) | — | $V_{DDE\_A}$–0.1 | — | $V_{DDE\_A}$+0.1 | V | D15.2 |
| $V_{AINx}$ | SR D | Analog input voltage[4] | — | $V_{SSA}$-0.1 | — | $V_{DDA}$+0.1 | V | D15.3 |
| $f_{ADC}$ | SR D | ADC analog frequency | — | 6 | — | 32 | MHz | D15.4 |
| $t_{ADC\_PU}$ | SR D | ADC power up delay | — | — | — | 1.5 | µs | D15.5 |
| $t_{ADC\_S}$ | CC[5] T | Sample time[6] | $f_{ADC}$ = 32 MHz, ADC_conf_sample_input = 17 | 0.5 | — | — | µs | D15.6 |
| | | | $f_{ADC}$ = 6 MHz, ADC_conf_sample_input = 127 | — | — | 21 | | |
| $t_{ADC\_C}$ | CC[5] T | Conversion time[7] | $f_{ADC}$ = 32 MHz, ADC_conf_comp = 2 | 0.625 | — | — | µs | D15.7 |
| $C_S$ | CC[5] D | ADC input sampling capacitance | — | — | — | 3 | pF | D15.8 |
| $C_{P1}$ | CC[5] D | ADC input pin capacitance 1 | — | — | — | 3 | pF | D15.9 |
| $C_{P2}$ | CC[5] D | ADC input pin capacitance 2 | — | — | — | 1 | pF | D15.10 |
| $C_{P3}$ | CC[5] D | ADC input pin capacitance 3 | — | — | — | 1 | pF | D15.11 |
| $R_{SW1}$ | CC[5] D | Internal resistance of analog source | — | — | — | 3 | kΩ | D15.12 |
| $R_{SW2}$ | CC[5] D | Internal resistance of analog source | — | — | — | 2 | kΩ | D15.13 |
| $R_{AD}$ | CC[5] D | Internal resistance of analog source | — | — | — | 0.1 | kΩ | D15.14 |
| $I_{INJ}$ | SR T | Input current Injection | Current injection on one ADC input, different from the converted one | -10 | — | 10 | mA | D15.15 |
| INL | CC[5] P | Integral Non Linearity | No overload | -1.5 | — | 1.5 | LSB | D15.16 |
| DNL | CC[5] P | Differential Non Linearity | No overload | -1.0 | — | 1.0 | LSB | D15.17 |
| OFS | CC[5] T | Offset error | After offset cancellation | — | 0.5 | — | LSB | D15.18 |
| GNE | CC[5] T | Gain error | — | — | 0.6 | — | LSB | D15.19 |

Table 49. ADC electrical characteristics (continued)

| Symbol | C | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|--------|---|-----------|---------------|-----|-----|-----|------|--------|
| | | | | Min | Typ | Max | | |
| TUEP | CC[5] | T | Total Unadjusted Error for precise channels, input only pins | No overload | -2 | — | 2 | LSB | D15.22 |
| | | | | overload conditions on adjacent channel | — | — | — | LSB | |
| TUEX | CC[5] | T | Total Unadjusted Error for extended channel, | No overload | -3 | — | 3 | LSB | D15.23 |
| | | | | overload conditions on adjacent channel | — | — | — | LSB | |

[1]  $V_{DDA}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = -40 to +105 °C, unless otherwise specified.

[2]  All values need to be confirmed during device validation.

[3]  Analog and digital $V_{SS}$ **must** be common (to be tied together externally).

[4]  $V_{AINx}$ may exceed $V_{SSA}$ and $V_{DDA}$ limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

[5]  Guaranteed by design.

[6]  During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{ADC\_S}$. After the end of the sample time $t_{ADC\_S}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{ADC\_S}$ depend on programming.

[7]  This parameter does not include the sample time $t_{ADC\_S}$, but only the time for determining the digital result and the time to load the result's register with the conversion result.

# 4.18   AC specifications

## 4.18.1   AC specification for CMOS090LP2 library @ VDDE = 3.3 V

Table 50. Functional pad type AC specifications

| Name | C | Prop. delay (ns) L>H / H>L[1] | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select |
|------|---|-----|-----|-----|-----|-----|-----|
| | | Min | Max | Min | Max | | MSB, LSB |
| pad_ssr | C | — | 4.5 / 4.5 | — | 2.2 / 2.2 | 50 | 11[2] |
| | | — | 8 / 8 | — | 6 / 6 | 200 | |
| | | — | 45 / 45 | — | 22 / 22 | 50 | 10 |
| | | — | 60 / 60 | — | 28 / 28 | 200 | |
| | | — | 90 / 90 | — | 42 / 42 | 50 | 01 |
| | | — | 110 / 110 | — | 50 / 50 | 200 | |
| | | — | 430 / 430 | — | 210 / 210 | 50 | 00 |
| | | — | 480 / 480 | — | 220 / 220 | 200 | |

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**Table 50. Functional pad type AC specifications (continued)**

| Name | C | Prop. delay (ns) L>H / H>L[1] | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | MSB, LSB |
| pad_fc | C | — | 2.5 / 2.5 | — | 1.2 / 1.2 | 10 | 00 |
| | | — | 2.5 / 2.5 | — | 1.2 / 1.2 | 20 | 01 |
| | | — | 2.5 / 2.5 | — | 1.2 / 1.2 | 30 | 10 |
| | | — | 2.5 / 2.5 | — | 1.2 / 1.2 | 50 | 11[2] |
| pad_msr | C | — | 4.0 / 4.5 | — | 1.02 / 1.4 | 50 | 11[2] |
| | | — | 7.3 / 8.3 | — | 3.5 / 4.2 | 200 | |
| | | — | 24 / 22 | — | 9.1 / 10.3 | 50 | 10 |
| | | — | 33 / 31 | — | 14 / 15 | 200 | |
| | | — | 49 / 44 | — | 18 / 21 | 50 | 01 |
| | | — | 60 / 53 | — | 24 / 25 | 200 | |
| | | — | 332 / 302 | — | 126 / 151 | 50 | 00 |
| | | — | 362 / 325 | — | 136 / 158 | 200 | |

[1] L>H signifies low-to-high propagation delay and H>L signifies high-to-low propagation delay.

[2] Can be used on the tester.

## 4.18.2 AC specification for CMOS090LP2fg library @ VDDE = 5.0 V

**Table 51. Functional pad type AC specifications**

| Name | C | Prop. delay (ns) L>H / H>L[1] | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | MSB, LSB |
| pad_msr_hv[2] | C | 4.6 / 3.7 | 12 / 12 | 2.2 / 2.2 | 5.3 / 5.9 | 50 | 11[3] |
| | | 13 / 10 | 32 / 32 | 9 / 9 | 22 / 22 | 200 | |
| | | N/A | | | | | 10[4] |
| | | 12 / 13 | 28 / 34 | 5.6 / 6 | 12 / 15 | 50 | 01 |
| | | 23 / 23 | 52 / 59 | 11 / 14 | 28 / 31 | 200 | |
| | | 69 / 71 | 152 / 165 | 34 / 35 | 70 / 74 | 50 | 00 |
| | | 95 / 90 | 205 / 220 | 44 / 51 | 96 / 96 | 200 | |

**Table 51. Functional pad type AC specifications (continued)**

| Name | C | Prop. delay (ns) L>H / H>L[1] | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | MSB, LSB |
| pad_ssr_hv[2] | C | 7.3 / 5.7 | 19 / 18 | 4.4 / 4.3 | 10 / 11 | 50 | 11[3] |
| | | 24 / 19 | 58 / 58 | 17 / 15 | 40 / 42 | 200 | |
| | | N/A | | | | | 10[4] |
| | | 26 / 27 | 61 / 69 | 13 / 13 | 30 / 34 | 50 | 01 |
| | | 49 / 45 | 115 / 115 | 27 / 23 | 61 / 61 | 200 | |
| | | 137 / 142 | 320 / 330 | 72 / 74 | 156 / 164 | 50 | 00 |
| | | 182 / 172 | 420 / 420 | 90 / 85 | 200 / 200 | 200 | |
| pad_i_hv | C | 0.5 / 0.5 | 1.9 / 1.9 | 0.3 / 0.3 | 1.5 / 1.5 | 0.5 | N/A |

[1] L>H signifies low-to-high propagation delay and H>L signifies high-to-low propagation delay.

[2] For input buffer timing, look at pad_i_hv.

[3] Can be used on the tester.

[4] This drive select value is not supported. If selected, it will be approximately equal to 11.

### 4.18.3    AC specification for CMOS090LP2fg library @ VDDE = 3.3 V

**Table 52. Functional pad AC type specifications**

| Name | Prop. delay (ns) L>H / H>L | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB, LSB |
| pad_msr_hv | 5.8 / 4.4 | 18 / 17 | 2.7 / 2.1 | 7.6 / 8.5 | 50 | 11 |
| | 16 / 13 | 46 / 49 | 11.2 / 8.6 | 30 / 34 | 200 | |
| | N/A | | | | | 10 |
| | 14 / 16 | 37 / 45 | 6.5 / 6.7 | 15.5 / 19 | 50 | 01 |
| | 27 / 27 | 69 / 82 | 15 / 13 | 38 / 43 | 200 | |
| | 83 / 86 | 200 / 210 | 38 / 38 | 86 / 86 | 50 | 00 |
| | 113 / 109 | 270 / 285 | 53 / 46 | 120 / 120 | 200 | |

**Table 52. Functional pad AC type specifications (continued)**

| Name | Prop. delay (ns) L>H / H>L | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB, LSB |
| pad_ssr_hv | 9.2 / 6.9 | 27 / 28 | 5.5 / 4.1 | 15 / 17 | 50 | 11 |
| | 30 / 23 | 81 / 87 | 21 / 16 | 57 / 63 | 200 | |
| | N/A | | | | | 10 |
| | 31 / 31 | 80 / 90 | 15.4 / 15.4 | 38 / 42 | 50 | 01 |
| | 58 / 52 | 144 / 155 | 32 / 26 | 82 / 85 | 200 | |
| | 162 / 168 | 415 / 415 | 80 / 82 | 190 / 190 | 50 | 00 |
| | 216 / 205 | 533 / 540 | 106 / 95 | 250 / 250 | 200 | |
| pad_i_hv | 0.5 / 0.5 | 3 / 3 | 0.4 / 0.4 | 1.5 / 1.5 | 0.5 | N/A |

## 4.18.4 AC specification for CMOS090_ddr library @ VDDE = 3.3 V

**Table 53. AC specifications at 3.3 V VDDE**

| Name | C | Prop. delay (ns) L>H / H>L | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select | Libraries |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | MSB, LSB | |
| pad_st_acc | C | 1.4/1.4 | 2.4/2.4 | 3.1/2.5 | 5.6/5.4 | 5 | 111 | 6MDDR |
| | | 1.7/1.7 | 2.7/2.7 | 0.9/1.1 | 1.7/2.0 | 20 | | |
| pad_st_dq | C | 1.4/1.4 | 2.4/2.4 | 3.1/2.5 | 5.6/5.4 | 5 | 111 | 6MDDR |
| | | 1.7/1.7 | 2.7/2.7 | 0.9/1.1 | 1.7/2.0 | 20 | | |
| pad_st_clk | C | 1.4/1.4 | 2.4/2.4 | 3.1/2.5 | 5.7/5.7 | 5 | 111 | 6MDDR |
| | | 1.6/1.6 | 2.6/2.6 | 1.1/1.3 | 2.3/2.3 | 20 | | |

## 4.18.5 AC specification for CMOS090_ddr library @ VDDE = 2.5 V

**Table 54. AC specifications at 2.5 V VDDE**

| Name | C | Prop. delay (ns) L>H / H>L | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select | Libraries |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | MSB, LSB | |
| pad_st_acc | C | 1.4/1.5 | 2.5/2.4 | 2.1/2.1 | 4.3/4.1 | 5 | 011 | 6MDDR |
| | | 1.7/1.7 | 2.8/2.7 | 0.6/0.7 | 1.1/1.3 | 20 | | |
| pad_st_dq | C | 1.4/1.5 | 2.5/2.4 | 2.1/2.1 | 4.3/4.1 | 5 | 011 | 6MDDR |
| | | 1.7/1.7 | 2.8/2.7 | 0.6/0.7 | 1.1/1.3 | 20 | | |
| pad_st_clk | C | 1.4/1.4 | 2.4/2.4 | 2.1/2.1 | 4.4/4.1 | 5 | 011 | 6MDDR |
| | | 1.1/1.6 | 2.7/2.7 | 0.6/0.7 | 1.6/1.8 | 20 | | |

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## 4.18.6  AC specification for CMOS090_ddr library @ VDDE = 1.8 V

**Table 55. AC electrical specifications at 1.8 V VDD**

| Name | C | Prop. delay (ns) L>H / H>L | | Rise/fall edge (ns) | | Drive load (pF) | Drive/slew rate select | Libraries |
| | | Min | Max | Min | Max | | MSB, LSB | |
|---|---|---|---|---|---|---|---|---|
| pad_st_acc | C | 1.4/1.4 | 2.4/2.4 | 0.6/1.0 | 2.7/2.6 | 5 | 000 | 6MDDR |
| | | 1.7/1.7 | 2.8/2.7 | 0.2/0.4 | 0.5/0.6 | 20 | | |
| | | 1.4/1.5 | 2.4/2.5 | 1.1/1.1 | 3.0/2.7 | 5 | 001 | |
| | | 1.7/1.7 | 2.8/2.8 | 0.4/0.4 | 0.7/0.7 | 20 | | |
| | | 1.4/1.5 | 2.4/2.4 | 1.0/1.1 | 2.9/2.7 | 5 | 010 | |
| | | 1.7/1.7 | 2.8/2.7 | 0.3/0.4 | 0.6/0.7 | 20 | | |
| | | 1.4/1.5 | 2.5/2.5 | 1.5/1.1 | 3.1/2.6 | 5 | 110 | |
| | | 1.7/1.8 | 2.8/2.8 | 0.4/0.4 | 0.7/0.6 | 20 | | |
| pad_st_dq | C | 1.4/1.4 | 2.4/2.4 | 0.6/1.0 | 2.7/2.6 | 5 | 000 | 6MDDR |
| | | 1.7/1.7 | 2.8/2.7 | 0.2/0.4 | 0.5/0.6 | 20 | | |
| | | 1.4/1.5 | 2.4/2.5 | 1.1/1.1 | 3.0/2.7 | 5 | 001 | |
| | | 1.7/1.7 | 2.8/2.8 | 0.4/0.4 | 0.7/0.7 | 20 | | |
| | | 1.4/1.5 | 2.4/2.4 | 1.0/1.1 | 2.9/2.7 | 5 | 010 | |
| | | 1.7/1.7 | 2.8/2.7 | 0.3/0.4 | 0.6/0.7 | 20 | | |
| | | 1.4/1.5 | 2.5/2.5 | 1.5/1.1 | 3.1/2.6 | 5 | 110 | |
| | | 1.7/1.8 | 2.8/2.8 | 0.4/0.4 | 0.7/0.6 | 20 | | |
| pad_st_clk | C | 1.4/1.4 | 2.4/2.4 | 0.4/0.6 | 2.7/2.7 | 5 | 000 | 6MDDR |
| | | 1.6/1.6 | 2.7/2.7 | 0.7/0.9 | 1.8/3.4 | 20 | | |
| | | 1.4/1.4 | 2.4/2.4 | 1.1/1.1 | 3.0/2.8 | 5 | 001 | |
| | | 1.7/1.7 | 2.7/2.7 | 0.3/0.4 | 1.0/1.1 | 20 | | |
| | | 1.4/1.4 | 2.4/2.4 | 0.9/1.1 | 3.0/2.8 | 5 | 010 | |
| | | 1.6/1.6 | 2.7/2.7 | 0.3/0.4 | 0.9/1.0 | 20 | | |
| | | 1.4/1.5 | 2.5/2.5 | 1.5/1.2 | 3.2/2.6 | 5 | 110 | |
| | | 1.7/1.8 | 2.7/2.7 | 0.4/0.4 | 1.1/1.2 | 20 | | |

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## 4.19  AC timing

### 4.19.1  IEEE 1149.1 interface timing

**Table 56. JTAG Interface Timing[1]**

| Num | Symbol | C | | Characteristic | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{JCYC}$ | $CC^2$ | D | TCK Cycle Time | 100 | — | ns | A1.1 |
| 2 | $t_{JDC}$ | $CC^2$ | D | TCK Clock Pulse Width (Measured at $V_{DD}/2$) | 40 | 60 | ns | A1.2 |
| 3 | $t_{TCKRISE}$ | $CC^2$ | D | TCK Rise and Fall Times (40% – 70%) | — | 3 | ns | A1.3 |
| 4 | $t_{TMSS}$, $t_{TDIS}$ | $CC^2$ | D | TMS, TDI Data Setup Time | 5 | — | ns | A1.4 |
| 5 | $t_{TMSH}$, $t_{TDIH}$ | $CC^2$ | D | TMS, TDI Data Hold Time | 25 | — | ns | A1.5 |
| 6 | $t_{TDOV}$ | $CC^2$ | D | TCK Low to TDO Data Valid | — | 35 | ns | A1.6 |
| 7 | $t_{TDOI}$ | $CC^2$ | D | TCK Low to TDO Data Invalid | 0 | — | ns | A1.7 |
| 8 | $t_{TDOHZ}$ | $CC^2$ | D | TCK Low to TDO High Impedance | — | 30 | ns | A1.8 |
| 9 | $t_{BSDV}$ | $CC^2$ | D | TCK Falling Edge to Output Valid | — | 35 | ns | A1.9 |
| 10 | $t_{BSDVZ}$ | $CC^2$ | D | TCK Falling Edge to Output Valid out of High Impedance | — | 50 | ns | A1.10 |
| 11 | $t_{BSDHZ}$ | $CC^2$ | D | TCK Falling Edge to Output High Impedance | — | 50 | ns | A1.11 |
| 12 | $t_{BSDST}$ | $CC^2$ | D | Boundary Scan Input Valid to TCK Rising Edge | 50 | — | ns | A1.12 |
| 13 | $t_{BSDHT}$ | $CC^2$ | D | TCK Rising Edge to Boundary Scan Input Invalid | 50 | — | ns | A1.13 |

[1]  These specifications apply to JTAG boundary scan only. JTAG timing specified at $V_{DD}$ = 3.0 V to 3.6 V, $T_A$ = -40 to 105 °C, and CL = 50 pF with SRC = 0b01.

[2]  Parameter values guaranteed by design.
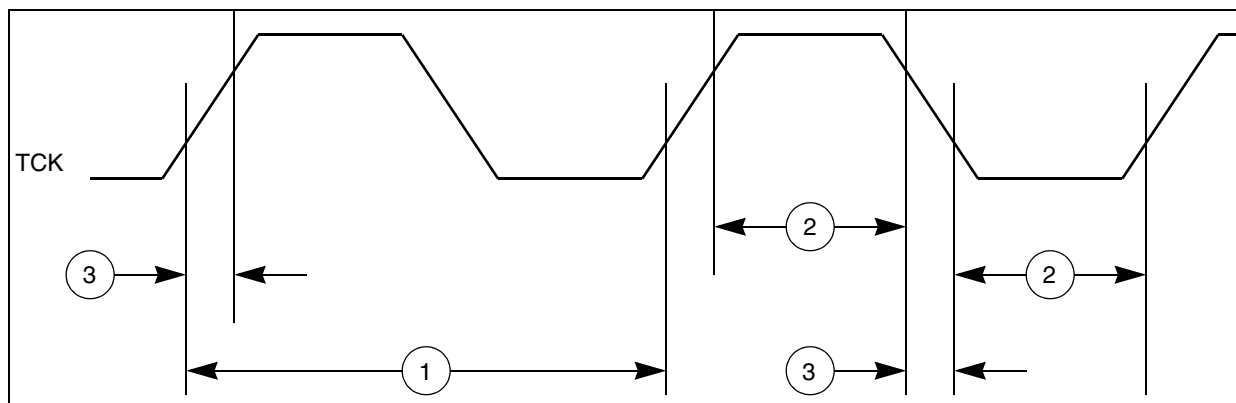


**Figure 17. JTAG Test Clock Input Timing**
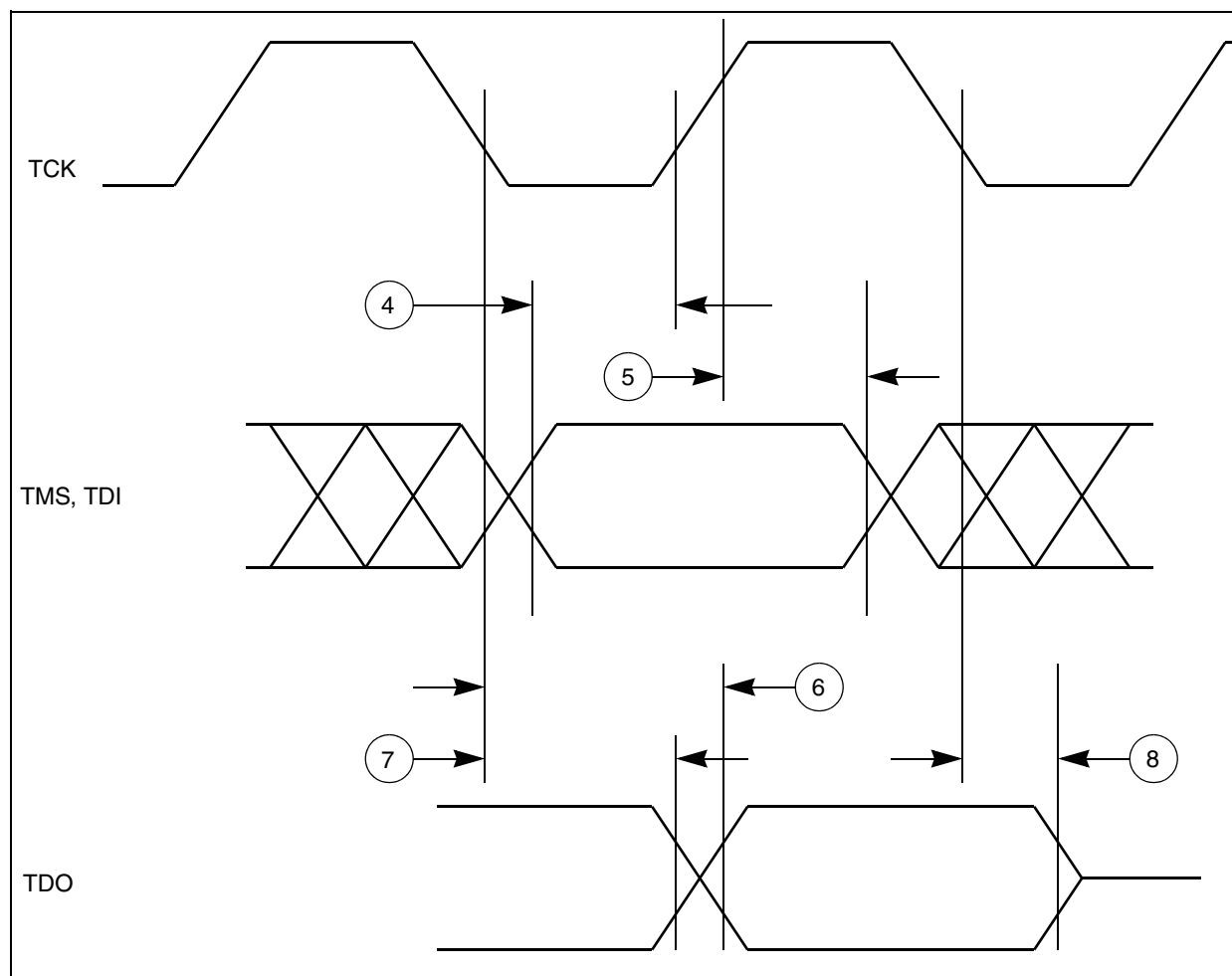
**Figure 18. JTAG Test Access Port Timing**
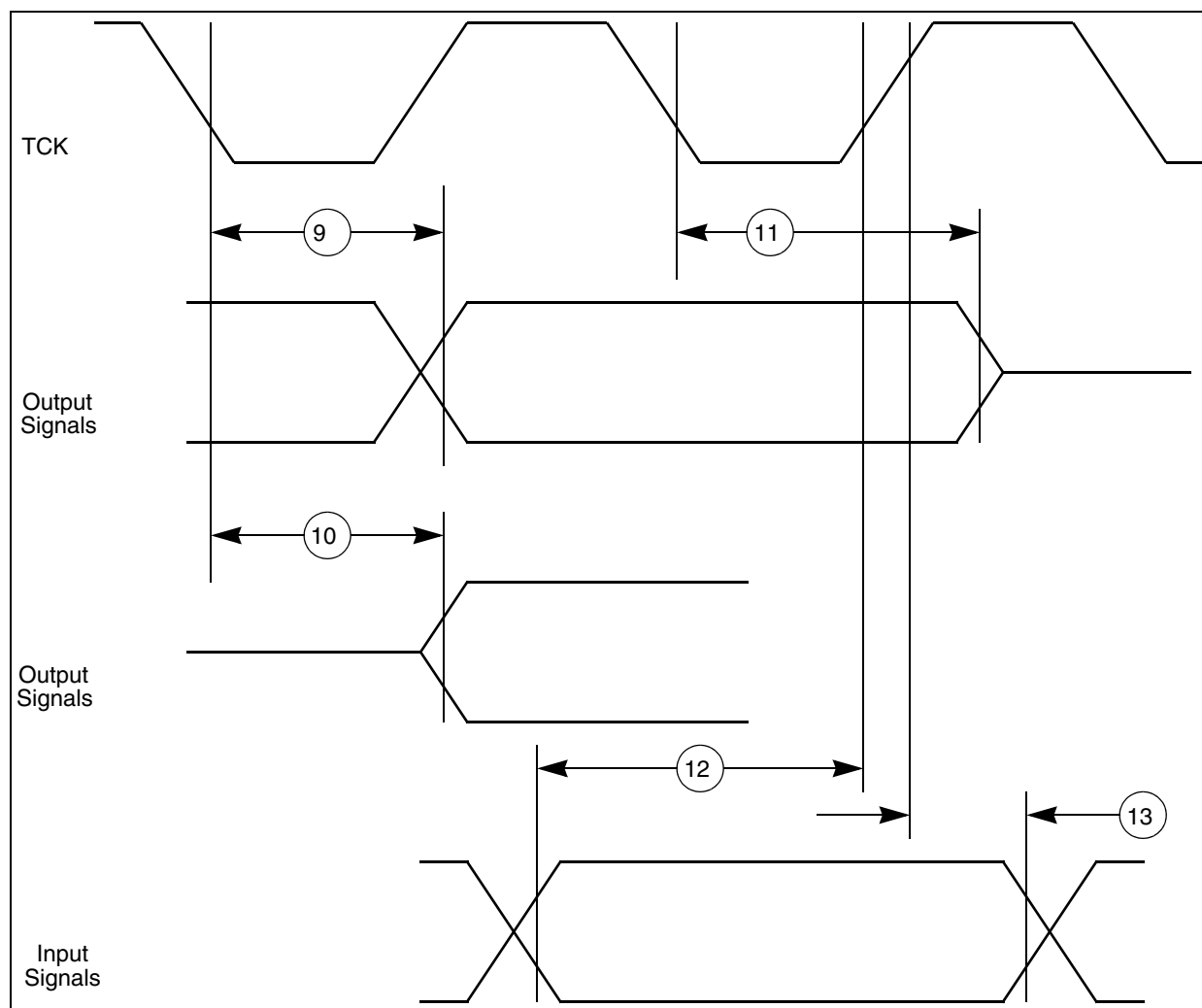
**Figure 19. JTAG Boundary Scan Timing**

## 4.19.2 Nexus Debug Interface

**Table 57. Nexus Debug Port Timing[1]**

| Num | Symbol | C | | Characteristic | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{MCYC}$ | CC[2] | D | MCKO Cycle Time | 15 | — | ns | A2.1 |
| 2 | $t_{MDC}$ | CC[2] | D | MCKO Duty Cycle | 40 | 60 | % | A2.2 |
| 3 | $t_{MDOV}$ | CC[2] | D | MCKO Low to MDO Data Valid[3] | 0.1 | 0.2 | $t_{MCYC}$ | A2.3 |
| 4 | $t_{MSEOV}$ | CC[2] | D | MCKO Low to $\overline{MSEO}$ Data Valid[3] | 0.1 | 0.2 | $t_{MCYC}$ | A2.4 |
| 5 | $t_{EVTOV}$ | CC[2] | D | MCKO Low to $\overline{EVTO}$ Data Valid[3] | 0.1 | 0.2 | $t_{MCYC}$ | A2.5 |
| 6 | $t_{EVTIPW}$ | CC[2] | D | $\overline{EVTI}$ Pulse Width | 4 | — | $t_{TCYC}$ | A2.6 |
| 7 | $t_{EVTOPW}$ | CC[2] | D | $\overline{EVTO}$ Pulse Width | 1 | — | $t_{MCYC}$ | A2.7 |
| 8 | $t_{TCYC}$ | CC[2] | D | TCK Cycle Time[4] | 100 | — | ns | A2.8 |
| 9 | $t_{TDC}$ | CC[2] | D | TCK Duty Cycle | 40 | 60 | % | A2.9 |
| 10 | $t_{NTDIS}$, $t_{NTMSS}$ | CC[2] | D | TDI, TMS Data Setup Time | 25 | — | ns | A2.10 |
| 11 | $t_{NTDIH}$, $t_{NTMSH}$ | CC[2] | D | TDI, TMS Data Hold Time | 5 | — | ns | A2.11 |
| 12 | $t_{JOV}$ | CC[2] | D | TCK Low to TDO Data Valid | 0 | 35 | ns | A2.12 |

[1] JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at $V_{DD}$ = 3.0 V to 3.6 V, $T_A$ = -40 to 105 °C, and CL = 50 pF (Cl=30 pF on MCKO), with SRC = 0b10 for MCKO and 0b11 for others.

[2] Parameter values guaranteed by design.

[3] MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.

[4] The system clock frequency needs to be three times faster that the TCK frequency.

### NOTE

Nexus Dual Data Rate is not supported. The timings are mentioned for dedicated pins on 416BGA. The max value for #2, 3 and 4 above, are 0.3 of tMCYC for shared nexus ports.
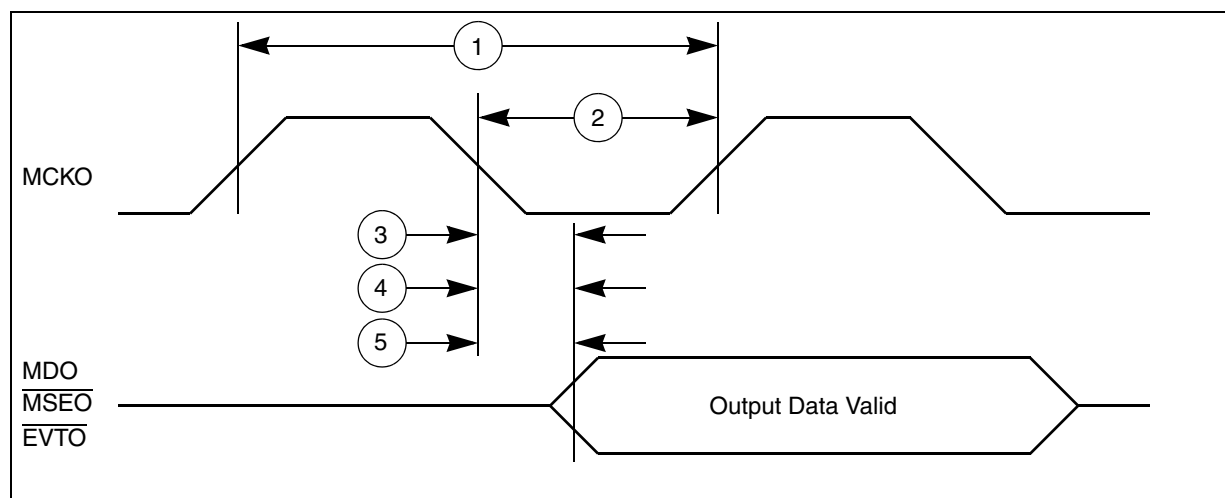


**Figure 20. Nexus Output Timing**

**MPC5645S Microcontroller Data Sheet, Rev. 14**
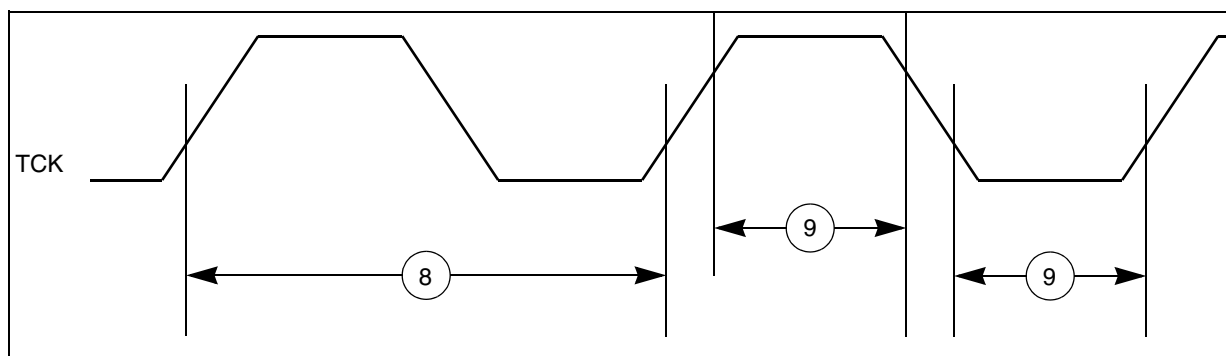
**Figure 21. Nexus TCK Timing**
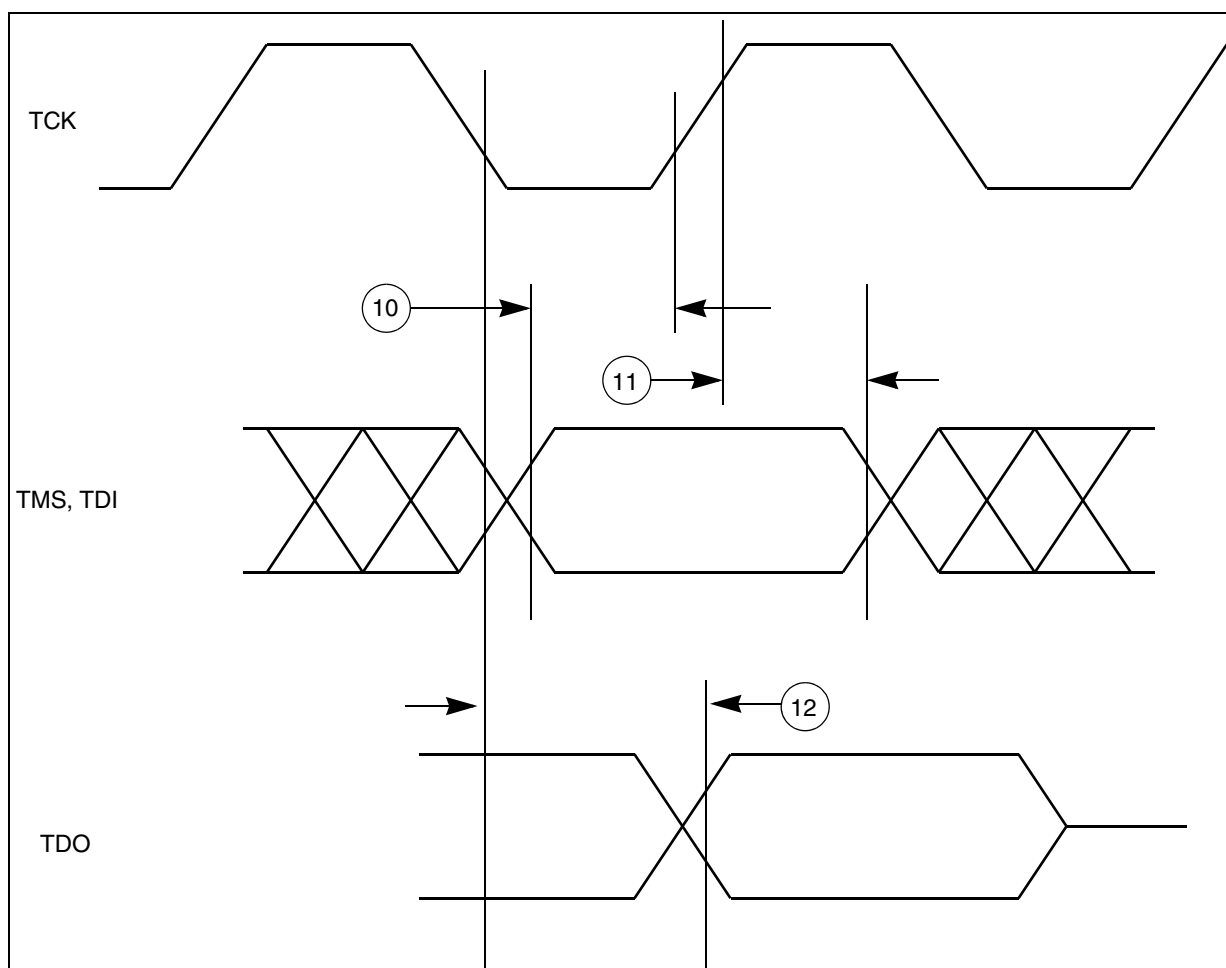


**Figure 22. Nexus TDI, TMS, TDO Timing**

## 4.19.3   Interface to TFT LCD Panels (DCU3 and DCULite)

Figure 23 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
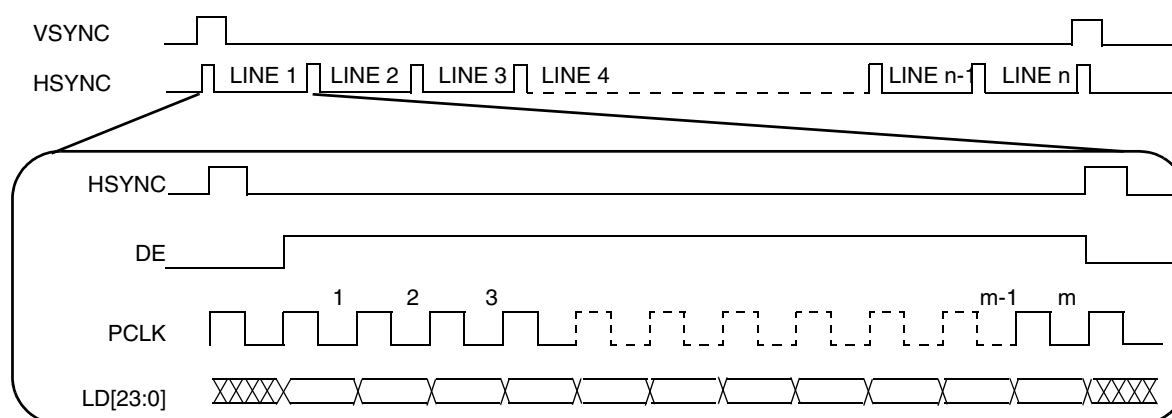


**Figure 23. TFT LCD interface timing overview[1]**

## 4.19.3.1 Interface to TFT LCD Panels—Pixel Level Timings

Figure 24 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high.

Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the DCU Clock Confide Register (DCCR) in the system clock module.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

---

1. In Figure 23, the "LD[23:0]" signal is "line data," an aggregation of the DCU's RGB signals—R[0:7], G[0:7] and B[0:7].

**Table 58. LCD interface timing parameters—horizontal and vertical**

| Num | Symbol | C | | Characteristic | Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| 1 | $t_{PCP}$ | CC[1] | D | Display pixel clock period | 31.25 | ns | A3.1 |
| 2 | $t_{PWH}$ | CC[1] | D | HSYNC pulse width | PW_H * $t_{PCP}$ | ns | A3.2 |
| 3 | $t_{BPH}$ | CC[1] | D | HSYNC back porch width | BP_H * $t_{PCP}$ | ns | A3.3 |
| 4 | $t_{FPH}$ | CC[1] | D | HSYNC front porch width | FP_H * $t_{PCP}$ | ns | A3.4 |
| 5 | $t_{SW}$ | CC[1] | D | Screen width | DELTA_X * $t_{PCP}$ | ns | A3.5 |
| 6 | $t_{HSP}$ | CC[1] | D | HSYNC (line) period | (PW_H + BP_H + FP_H + DELTA_X ) * $t_{PCP}$ | ns | A3.6 |
| 7 | $t_{PWV}$ | CC[1] | D | VSYNC pulse width | PWV * $t_{HSP}$ | ns | A3.7 |
| 8 | $t_{BPV}$ | CC[1] | D | VSYNC back porch width | BP_V * $t_{HSP}$ | ns | A3.8 |
| | $t_{FPV}$ | CC[1] | D | VSYNC front porch width | FP_V * $t_{HSP}$ | ns | A3.9 |
| | $t_{SH}$ | CC[1] | D | Screen height | DELTA_Y * $t_{HSP}$ | ns | A3.10 |
| | $t_{VSP}$ | CC[1] | D | VSYNC (frame) period | (PW_V + BP_V + FP_V + DELTA_Y ) * $t_{HSP}$ | ns | A3.11 |

[1] Parameter values guaranteed by design.
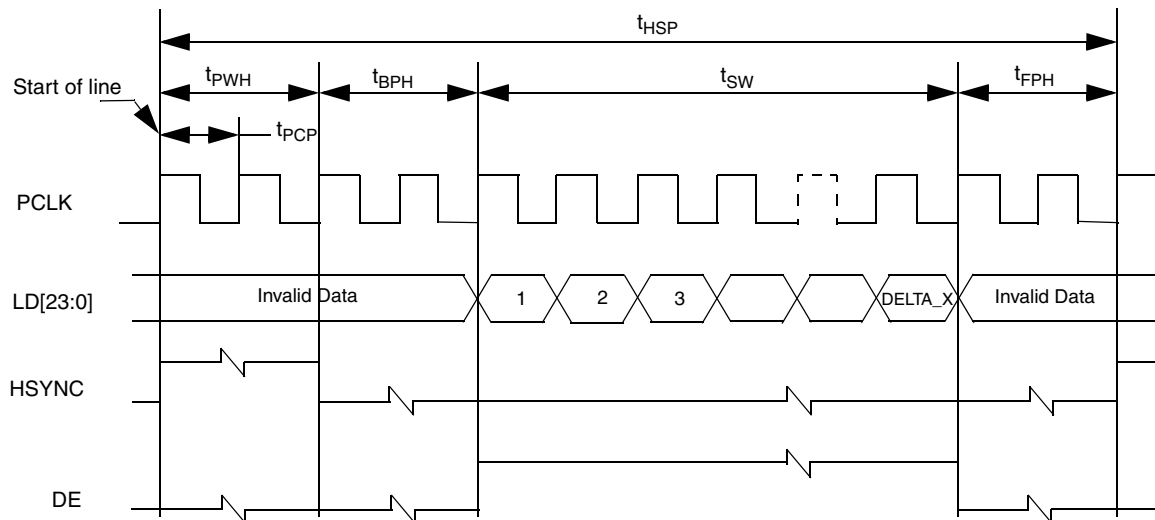


**Figure 24. Horizontal sync timing**
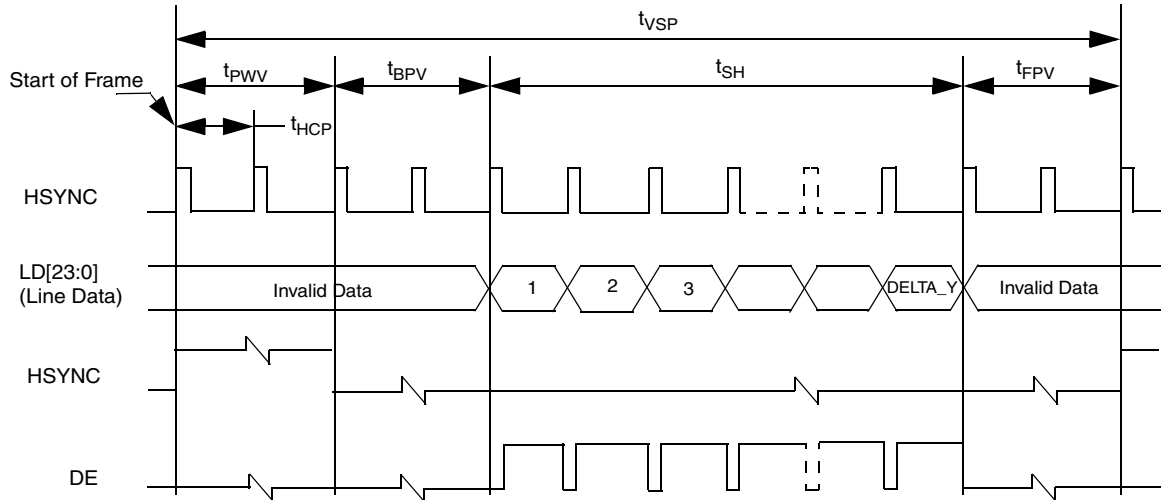
**Figure 25. Vertical sync pulse**

### 4.19.3.2 Interface to TFT LCD panels—access level

**Table 59. LCD Interface Timing Parameters[1,2,3,4]—Access Level**

| Num | Symbol | C | | Characteristic | Min. Value | Typical Value | Max. Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{CKP}$ | CC[5] | D | PDI Clock Period | 31.25 | — | — | ns | A3.12 |
| 2 | $t_{CHD}$ | CC[5] | D | Duty cycle | 40 | — | 60 | % | A3.13 |
| 3 | $t_{DSU}$ | CC[5] | D | interface data setup time | 6 | — | — | ns | A3.14 |
| 4 | $t_{DHD}$ | CC[5] | D | PDI interface data access hold time | 1 | — | — | ns | A3.15 |
| 5 | $t_{CSU}$ | CC[5] | D | PDI interface control signal setup time | 3 | — | — | ns | A3.16 |
| 6 | $t_{CHD}$ | CC[5] | D | PDI interface control signal hold time | 1 | — | — | ns | A3.17 |
| 7 | | CC[5] | D | TFT interface data valid after pixel clock | — | — | 6 | ns | A3.18 |
| 8 | | CC[5] | D | TFT interface HSYNC valid after pixel clock | — | — | 5 | ns | A3.19 |
| 9 | | CC[5] | D | TFT interface VSYNC valid after pixel clock | — | — | 5.5 | ns | A3.20 |
| 10 | | CC[5] | D | TFT interface DE valid after pixel clock | — | — | 5.6 | ns | A3.21 |
| 11 | | CC[5] | D | TFT interface hold time for data and control bits | 2 | — | — | ns | A3.22 |
| 12 | | CC[5] | D | Relative skew between the data bits | — | — | 3.7 | ns | A3.23 |

[1] The characteristics in this table are based on the assumption that data is output at +ve edge and displays latch data on -ve edge.

[2] Intra bit skew is less than 2 ns.

[3] Load CL = 50 pf for frequency up to 20 MHz.

[4] Load CL = 25 pf for display freq from 20 to 32 MHz.

[5] Parameter values guaranteed by design.

**MPC5645S Microcontroller Data Sheet, Rev. 14**
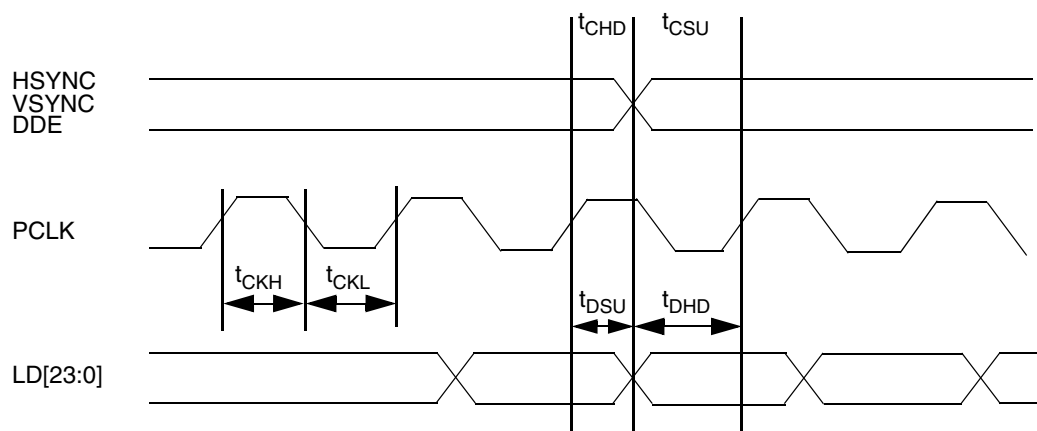
**Figure 26. LCD Interface Timing Parameters—Access Level**

## 4.19.4    RSDS Interface to TFT LCD Panels

**Table 60. RSDS Electrical Characteristics**

| Symbol | C | | Parameter | Conditions[1] | Value[2] | | | Unit | SpecID |
|--------|---|---|-----------|---------------|:---:|:---:|:---:|:---:|:---:|
| | | | | | Min | Typ | Max | | |
| AVDD | SR | D | Voltage on VSSE_A pin with respect to ground ($V_{SS}$) | — | 3.0 | 3.3 | 3.6 | V | A4.1 |
| $I_{DDTX}$ | SR | D | Current Consumption: RSDS Transmitter - Single Cell | — | — | 2.7 | — | mA | A4.2 |
| $I_{DDPD}$ | SR | D | Power Down Current | — | — | 10 | — | µA | A4.3 |
| $I_{DDBG}$ | SR | D | Current Consumption of Bandgap and buffer | — | — | 100 | — | µA | A4.4 |
| Fmax | SR | D | Data Frequency | — | — | 60 | 85 | MHz | A4.5 |
| $V_{OD}$ | SR | D | Differential Output Voltage | $R_L$ = 100 Ω | | 200 | 400 | mV | A4.6 |
| $V_{OFF}$ | SR | D | Offset Voltage | $V_{CM}$ +/-5% | 0.5 | 1.2 | 1.5 | V | A4.7 |
| $t_R$ / $t_F$ | SR | D | Output Rise / Fall times | 20% to 80%, $V_{OD}$=200mV, $C_L$ = 5pF | — | 500 | — | ps | A4.8 |
| $t_{Xdelay}$ | SR | D | Tx Delay | — | — | 3 | — | ns | A4.9 |
| | SR | D | Termination Resistance (external) | 5% variation | — | 100 | — | Ω | A4.10 |
| | SR | D | Transmitter Settling time | After power down, high to low | — | 10 | — | µs | A4.11 |
| | SR | D | Transmitter Delay | Data in to Tx out | — | 8 | — | ns | A4.12 |

[1]  $V_{DDA}$ = 3.3 V ± 10% $T_A$ = -40 to +105 °C, unless otherwise specified.
[2]  All values need to be confirmed during device validation.
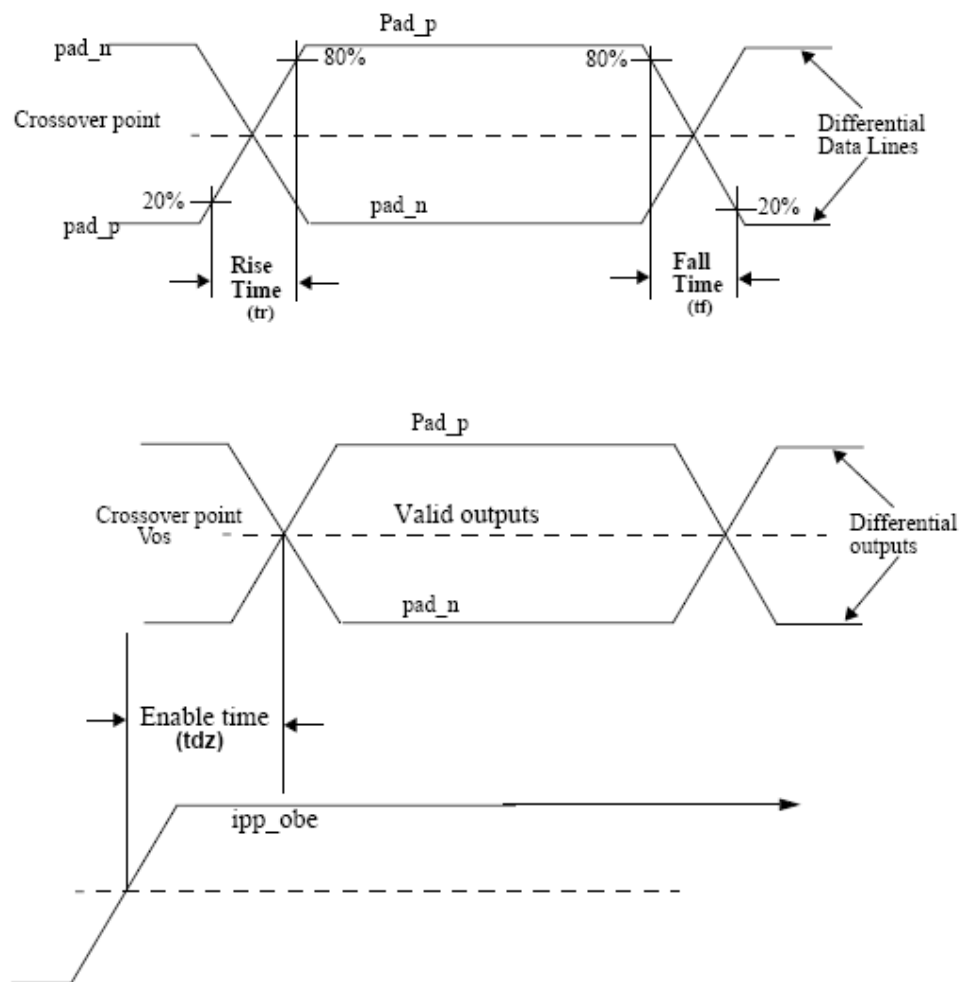
**Figure 27. TCON/RSDS Timing Diagram**

## 4.19.5  DRAM Interface

DDR Interface specification from 'MCD - 32 Bit Automotive MCU - CMOS090LP2' I/O Pad Specification Revision 1.5 - May14th 2008.

This device supports SDR, DDR1, DDR2 half and full strengths, as well as LPDDR half and full speeds. Table 61 shows the SRE settings for the different modes.

**Table 61. Pad mode configurations**

| ipp_sre[2:0] | Mode |
|---|---|
| 000 | 1.8V LPDDR Half Speed |
| 001 | 1.8V LPDDR Full Speed |
| 010 | 1.8V DDR2 Half Strength |
| 011 | 2.5V DDR1 |
| 100 | Not supported |
| 101 | Not supported |
| 110 | 1.8V DDR2 Full Strength |
| 111 | SDR |

**Table 62. LPDDR, DDR and DDR2 (DDR2-250) SDRAM timing specifications[1 2 3 4 5 6]**

**At recommended operating conditions with $V_{DD\_DR}$ of $\pm5\%$**

| No. | — | Symbol | | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | — | F | CC | Frequency of Operation (Clock Period)[7] | — | 125 | MHz |
| 2 | — | $V_{IX-AC}$ | CC | MCK AC differential crosspoint voltage | $V_{DD\_DR} \times 0.5 - 0.1$ | $V_{DD\_DR} \times 0.5 + 0.1$ | V |
| 3 | DD1 | $t_{SDCK}$ | CC | Clock period | 8 | — | ns |
| 4 | DD2 | $t_{SDCKH}$ | CC | HIGH pulse width [8] | 0.45 | 0.55 | tSDCK |
| 5 | DD3 | $t_{SDCKL}$ | CC | LOW pulse width[9] | 0.45 | 0.55 | tSDCK |
| 6 | DD4 | $t_{CMV}$ | CC | Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_CS[1:0] - Output Valid[9] | — | $(0.5 \times t_{SDCK}) + 1.5$ | ns |
| 7 | DD4.1 | $t_{CMS}$ | CC | Address, SD_CKE, SD_CAS, SD_RAD, SD_WE, SD_CS output setup (($t_{SDCK}$ - $t_{CMV}$ )[10] | 2.5 | — | ns |
| 8 | DD5 | $t_{CMH}$ | CC | Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_CS[1:0] - Output Hold | 2.0 | — | ns |
| 9 | DD6 | $t_{DQSS}$ | CC | Write Command to first DQS Latching Transition | — | WL + 0.20 x $t_{SDCK}$ | ns |
| 10 | DD7 | $t_{OS}$ | CC | Data and Data Mask Output Setup (DQ-->DQS) relative to DQS (DDR Write Mode)[11 12] | 1.0 | — | ns |

**At recommended operating conditions with $V_{DD\_DR}$ of $\pm5\%$ (continued)**

| No. | — | Symbol | | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| 11 | DD8 | $t_{OH}$ | CC | Data and Data Mask Output Hold (DQS-->DQ) relative to DQS (DDR Write Mode)[13] | 1.0 | — | ns |
| 12 | DD9, DD10 | $t_{IS}$ | CC | Input Data Skew relative to DQS[14] | -(0.25*$t_{SDCK}$ - 0.8) | 0.25*$t_{SDCK}$ - 0.8 | ns |

[1] $V_{DD\_DR}$ value is 1.8 V for DDR2 mode, 2.5 V for DDR1 mode, and 1.8 V for LPDDR mode.

[2] $C_Z$ at -40, 140, 25 °C.

[3] Measured with clock pin loaded with differential 100 ohm termination resistor.

[4] All transitions measured at mid-supply ($V_{DD\_DR}/2$).

[5] Measured with all outputs except the clock loaded with 50 ohm termination resistor to $V_{DD\_DR}/2$.

[6] Data input hold is derived from each DDR_DQS clock edge. It begins with a DDR_DQS transition and ends when the first data line becomes invalid.

[7] The DRAM interface operates at the same frequency as the internal system bus.

[8] Pulse width high plus pulse width low cannot exceed min and max clock period.

[9] Command output valid should be half the memory bus clock ($t_{SDCK}$) plus some minor adjustments for process, temperature, and voltage variations.

[10] This is alternate representation of $t_{CMV}$ parameter for clarity.

[11] This specification relates to the required input setup time of DDR memories. The mcu's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. DDR_DQ[31:24] is relative to DDR_DQS[3]; DDR_DQ[23:16] is relative to DDR_DQS[2], DDR_DQ[15:8] is relative to DDR_DQS[1] and DDR_DQ[7:0] is relative to DDR_DQS[0].

[12] The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

[13] This specification relates to the required hold time of DDR memories. DDR_DQ[31:24] is relative to DDR_DQS[3]; DDR_DQ[23:16] is relative to DDR_DQS[2], DDR_DQ[15:8] is relative to DDR_DQS[1] and DDR_DQ[7:0] is relative to DDR_DQS[0].

[14] Data input skew is derived from each DDR_DQS clock edge. It begins with a DDR_DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

Figure 28 shows the DDR SDRAM write timing.
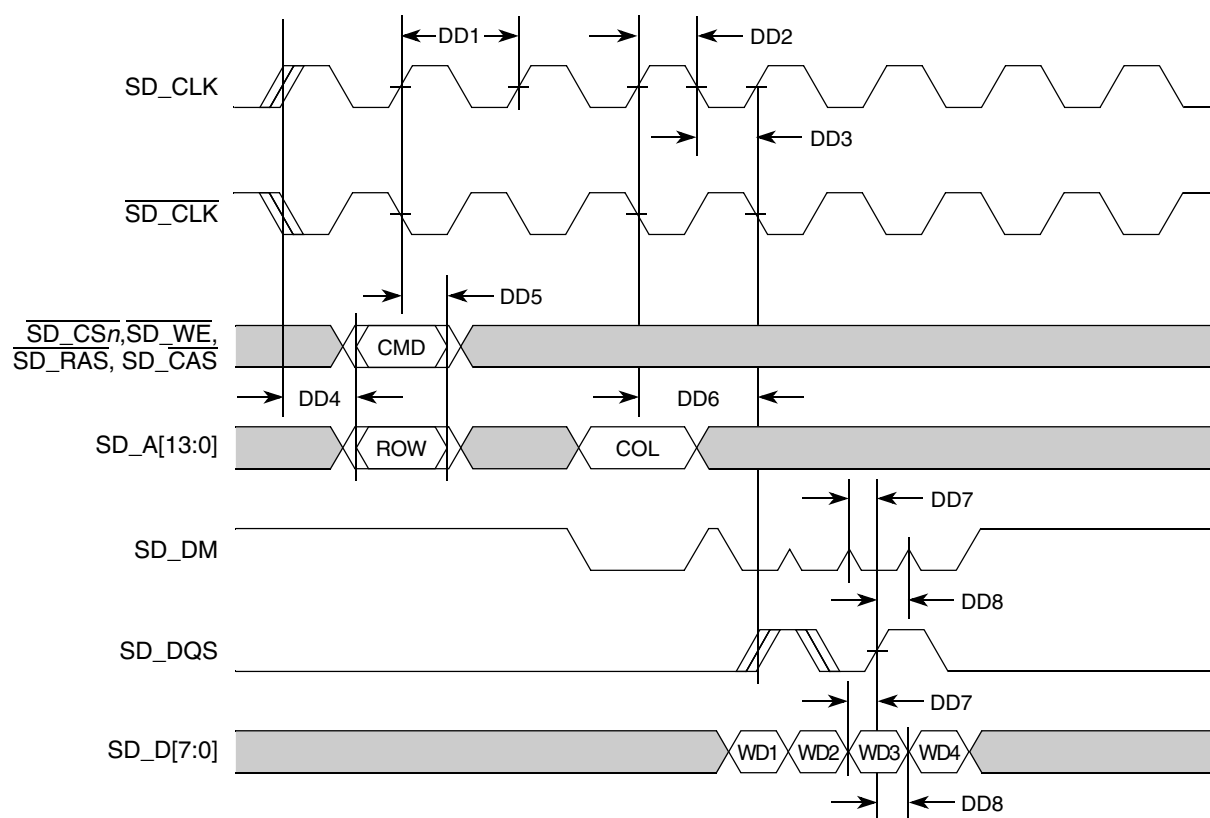


**Figure 28. DDR write timing**

Figure 29 and Figure 31 show the DDR SDRAM read timing.
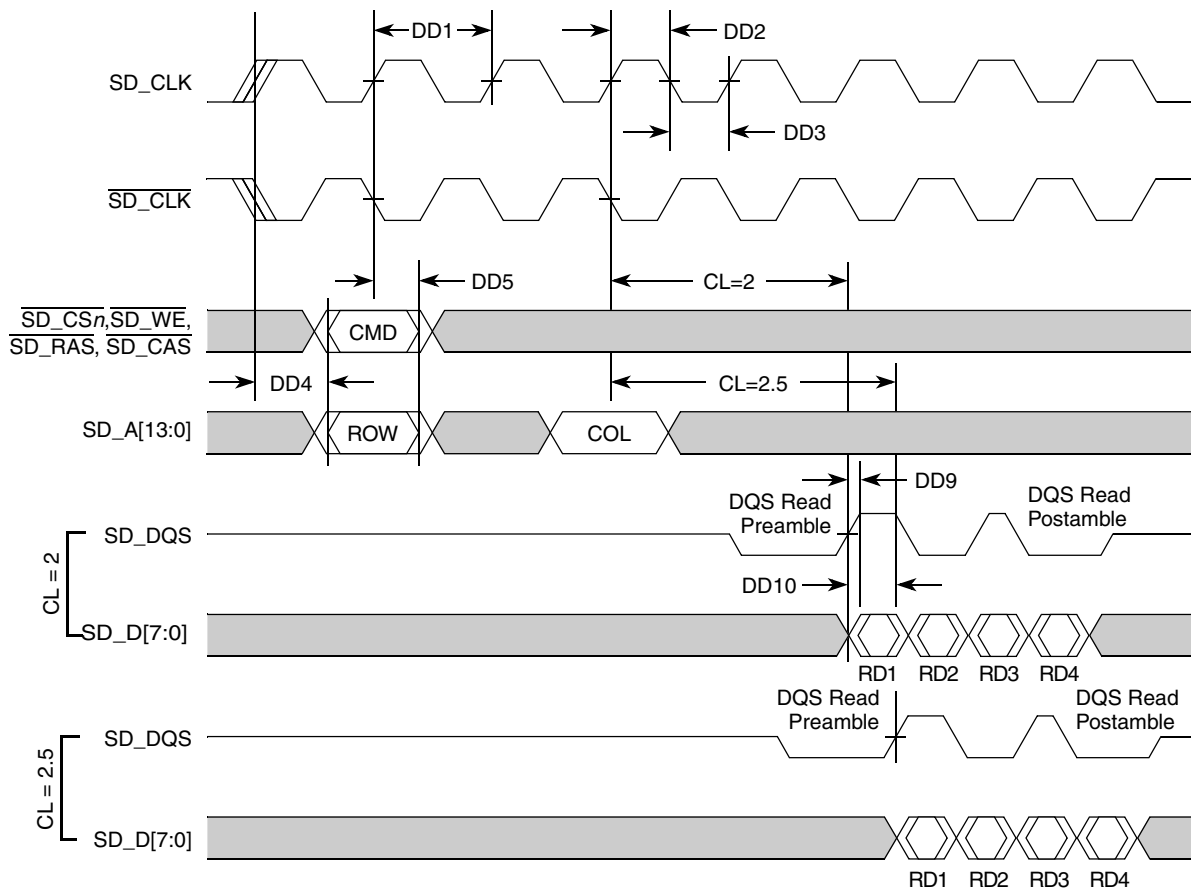


**Figure 29. DDR read timing**

Figure 30 provides the AC test load for the DDR bus.
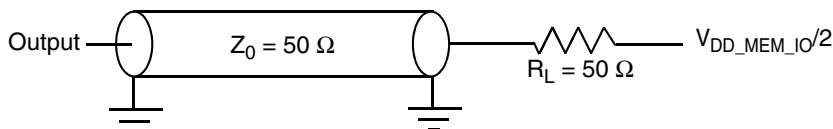


**Figure 30. DDR AC test load**

### 4.19.5.1    SDR Timings

Command and address follow the same timings as other modes. For SDRAM reads/Write, the timings mentioned in the following table apply.

**Table 63. SDR Timings**

| — | Symbol | C | Parameter | Min | Max | Units |
|---|--------|---|-----------|-----|-----|-------|
| DD1 | $t_{QVS}$ | C | Data output Valid (Write transaction) | — | $(0.5 \times t_{SDCK}) + 1.5$ | ns |
| DD1.1 | $t_{QS}$ | C | Data output setup $(t_{DSK} - DD1)$[1] | 2.5 | — | ns |
| DD2 | $t_{QH}$ | C | Data output Hold (Write transaction) | 2.0 | — | ns |
| DD3 | $t_{IS}$ | C | Data Input Setup (Read transaction) | — | 2.0 | ns |
| DD4 | $t_{IH}$ | C | Data input Hold (Read transaction) | — | 2.0 | ns |

[1] This is alternate representation for DD1 for better clarity.
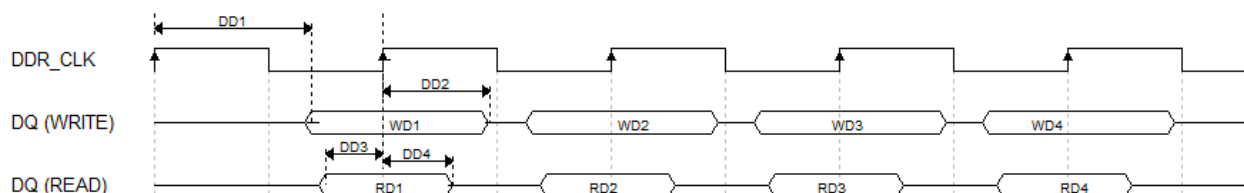


**Figure 31. SDR Read and Write Timings**

## 4.19.5.2    2.5 V DDR1

**Table 64. SSTL_2 Class II 2.5 V DDR DC Specifications**

| Symbol | C | Parameter | Condition | Min | Nom | Max | Units | Notes | SpecID |
|--------|---|-----------|-----------|-----|-----|-----|-------|-------|--------|
| vddet | P | I/O Supply Voltage | — | 2.30 | 2.50 | 2.70 | V | JESD8-9B | A5.1 |
| vdd | P | Core Supply Voltage | — | 1.08 | 1.20 | 1.32 | V | — | A5.2 |
| Vref(dc) | P | Input Reference Voltage | — | 1.13 | 1.25 | 1.38 | V | JESD8-9B | A5.3 |
| Vtt | P | Termination Voltage | — | Vref-0.04 | vref | Vref+0.04 | V | JESD8-9B | A5.4 |
| $V_{ih(dc)}$ | C | DC Input Logic High | — | Vref+0.15 | — | vddet+0.3 | V | JESD8-9B | A5.5 |
| $V_{il(dc)}$ | C | DC Input Logic Low | — | -0.3 | — | Vref-0.15 | V | JESD8-9B | A5.6 |
| $V_{ih(ac)}$ | C | AC Input Logic High | — | Vref+0.31 | — | — | V | JESD8-9B | A5.7 |
| $V_{il(ac)}$ | C | AC Input Logic Low | — | — | — | Vref-0.31 | V | JESD8-9B | A5.8 |
| $I_{in}$ | P | Pad input Leakage Current | — | — | — | +/-10 | µA | — | A5.9 |

Table 64. SSTL_2 Class II 2.5 V DDR DC Specifications (continued)

| Symbol | C | Parameter | Condition | Min | Nom | Max | Units | Notes | SpecID |
|--------|---|-----------|-----------|-----|-----|-----|-------|-------|--------|
| $V_{oh}$ | C | Output High Voltage Level | — | vddet-0.35 | — | — | V | — | A5.10 |
| $V_{ol}$ | C | Output Low Voltage Level | — | — | — | 0.35 | V | | A5.11 |
| $I_{oh(dc)}$ | C | Output min source dc current | Vout=Voh | -16.2 | — | — | mA | vddet = 2.3V Voh = 1.95V | A5.12 |
| $I_{ol(dc)}$ | C | Output min sink dc current | Vout=Vol | 16.2 | — | — | mA | vddet = 2.3V Vol = 0.35V | A5.13 |

The SSTL_2 differential input switch point is at vref = 0.50*vddet.

## NOTE

The JEDEC SSTL_2 specifications (JESD8-9B) for a SSTL interface for class II operation supersedes any specification in this document.

The SSTL_2 Class II output with ipp_sre[2:0] set to enabling SSTL_2 2.5V DDR1 mode, at the destination, have a rise/fall time (10%-90%) between 1 ns and 2 ns over process, voltage, and temperature driving a 70 ohm transmission line with 0.167 ns td terminated at the destination with 70 ohms to Vtt (0.5*vddet) with 4.0 pf, representing the DDR input capacitance.
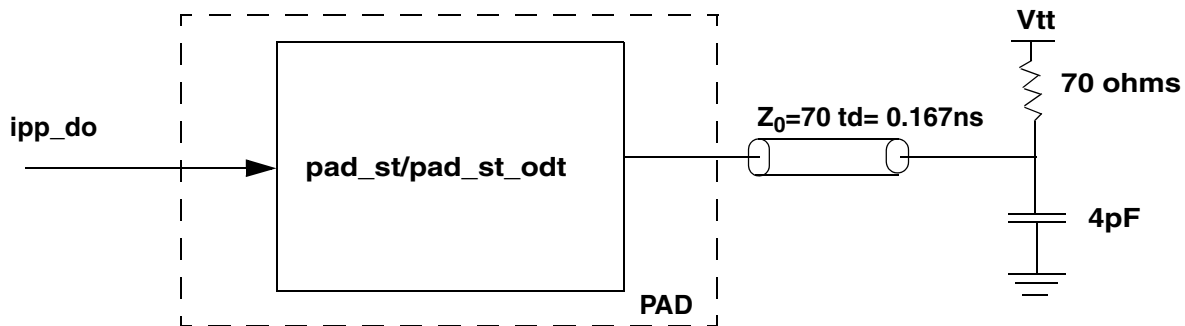


Figure 32. SSTL_2 CLass II Test Load

MPC5645S Microcontroller Data Sheet, Rev. 14

## 4.19.5.3    1.8 V DDR2

**Table 65. SSTL_18 Class II 1.8 V DDR2 DC Specifications**

| Symbol | C | Parameter | Condi-tion | Min | Nom | Max | Units | Notes | SpecID |
|---|---|---|---|---|---|---|---|---|---|
| vddet | P | I/O Supply Voltage | — | 1.7 | 1.8 | 1.9 | V | JESD8-15A | A5.14 |
| vdd | P | Core Supply Voltage | — | 1.08 | 1.2 | 1.32 | V | | A5.15 |
| Vref(dc) | P | Input Reference Volt-age | — | 0.833 | 0.9 | 1.0869 | V | JESD8-15A | A5.16 |
| Vtt | P | Termination Voltage | — | Vref-0.04 | Vref | Vref+0.04 | V | JESD8-15A | A5.17 |
| $V_{ih(dc)}$ | C | DC Input Logic High | — | Vref+0.125 | — | vddet+0.3 | V | JESD8-15A | A5.18 |
| $V_{il(dc)}$ | C | DC Input Logic Low | — | -0.3 | — | Vref-0.125 | V | JESD8-15A | A5.19 |
| $V_{ih(ac)}$ | C | AC Input Logic High | — | Vref+0.25 | — | — | V | JESD8-15A | A5.20 |
| $V_{il(ac)}$ | C | AC Input Logic Low | — | — | — | Vref-0.25 | V | JESD8-15A | A5.21 |
| $I_{in}$ | T | Pad input Leakage Current | — | — | — | +/-10 | µA | — | A5.22 |
| $V_{oh}$ | C | Output High Voltage Level | — | vddet-0.28 | — | — | V | — | A5.23 |
| $V_{ol}$ | C | Output Low Voltage Level | — | — | — | 0.28 | V | — | A5.24 |
| $I_{oh(dc)}$ | C | Output min source dc current | Vout=Voh | -13.4 | — | — | mA | JESD8-15A vddet = 1.7V Voh = 1.42V | A5.25 |
| $I_{ol(dc)}$ | C | Output min sink dc current | Vout=Vol | 13.4 | — | — | mA | JESD8-15A vddet = 1.7V Vol = 0.28V | A5.26 |

The SSTL_18 differential input switch point is at vref = 0.50*vddet.

Note that the Jedec SSTL_18 specifications (JESD8-15a) for a SSTL interface for class II operation supersedes any specification in this document.

The SSTL_18 Class II output with ipp_sre[2:0] set to enabling sstl_2 1.8V DDR2 mode, at the destination, have a rise/fall time (10%-90%) between 0.4 ns and 1.0 ns over process, voltage, and temperature driving a 70 ohm transmission line with 0.167 ns

td terminated at the destination with 70 ohms to Vtt (0.5*vddet) with 4.0 pf, representing the DDR2 input capacitance. See Figure 33. "SSTL_18 CLass II Test Load".

**Figure 33. SSTL_18 CLass II Test Load**
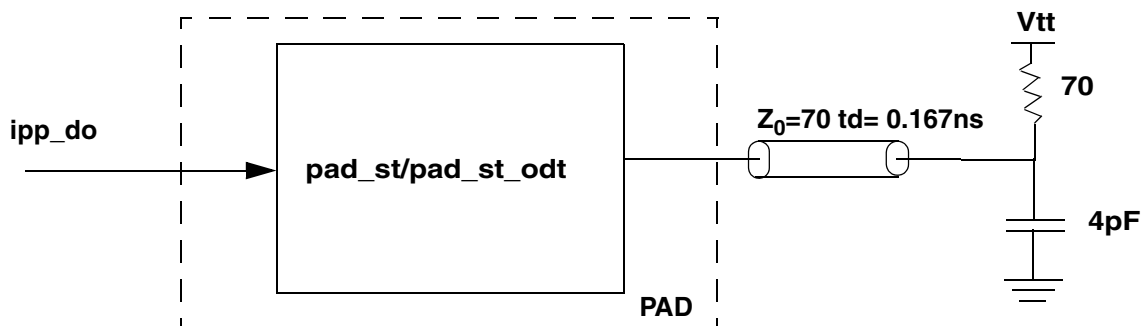


## 4.19.5.4    1.8V LPDDR

**Table 66. 1.8V LPDDR DC Specifications**

| Symbol | C | Parameter | Condition | Min | Nom | Max | Units | Notes | SpecID |
|--------|---|-----------|-----------|-----|-----|-----|-------|-------|--------|
| vddet | P | I/O Supply Voltage | — | 1.7 | 1.8 | 1.9 | V | JESD79-4 | A5.27 |
| vdd | P | Core Supply Voltage | — | 1.08 | 1.2 | 1.32 | V | — | A5.28 |
| Data Inputs (DQ, DM, DQS) | | | | | | | | | A5.29 |
| $V_{ih(dc)}$ | C | DC Input Logic High | — | vddet*0.7 | — | vddet+0.3 | V | JESD79-4 | A5.30 |
| $V_{il(dc)}$ | C | DC Input Logic Low | — | -0.3 | — | vddet*0.3 | V | JESD79-4 | A5.31 |
| $V_{ih(ac)}$ | C | AC Input Logic High | — | vddet*0.8 | — | vddet+0.3 | V | JESD79-4 | A5.32 |
| $V_{il(ac)}$ | C | AC Input Logic low | — | -0.3 | — | vddet*0.2 | V | JESD79-4 | A5.33 |
| Data Outputs (DQ, DQS) | | | | | | | | | A5.34 |
| $V_{oh}$ | C | Output High Voltage Level | Ioh=-0.1mA | vddet*0.9 | — | — | V | JESD79-4 | A5.35 |
| $V_{ol}$ | C | Output Low Voltage Level | Iol=0.1mA | — | — | vddet*0.1 | V | JESD79-4 | A5.36 |

Note that the final JEDEC LPDDR SDRAM specifications (JESD79-4) for LPDDR operation supersedes any specification in this document.

The SSTL_18 output with ipp_sre[2:0] set to enabling 1.8V LPDDR mode, at the destination, have a rise/fall time (10%-90%) between 0.4 ns and 1.0 ns over process, voltage, and temperature driving a 70 ohm transmission line with 0.167 ns td terminated at the destination with 70 ohms to Vtt (0.5*vddet) with 4.0 pf, representing the DDR input capacitance. See ""Figure 28.

## 4.19.6 Video Input Unit timing
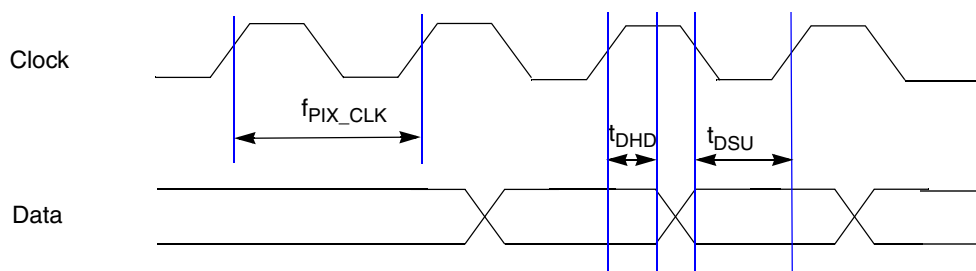


**Figure 34. VIU2 timing diagram**

**Table 67. VIU2 timing parameters**

| Parameter | C | Description | Min | Typ | Max | Unit | SpecID |
|-----------|---|-------------|-----|-----|-----|------|--------|
| $f_{PIX\_CK}$ | D | VIU2 pixel clock frequency | — | — | [1] | MHz | A6.1 |
| $t_{DSU}$ | D | VIU2 data setup time | 4 | — | — | ns | A6.2 |
| $t_{DHD}$ | D | VIU2 data hold time | 1 | — | — | ns | A6.3 |

[1]  PIX_CLK_PERIOD(min) =  C1 X IPG_CLK_PERIOD + C2 + J

where

C1  = Device parameter  = 2 (if Frequency Modulation is disabled), = 2.04 (if Frequency Modulation is enabled)

C2 = Device Constant = 1.98 ns

J = Max Jitter on PIX_CLK

**For example**: If IPG_CLK = 125 MHz, FM on PLL is disabled and Max Jitter on PIX_CLK is  (+-2ns), then the maximum frequency of VIU pixel clock will be: PIX_CLK_F = 1/(2x8 + 1.98 + 2)ns = 50.05 MHz

## 4.19.7 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Timing

**Table 68. IRQ and NMI Timing**

| Num | Symbol | C | | Characteristic | Min. Value | Max. Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{IPWL}$ | CC[1] | D | IRQ/NMI Pulse Width Low | 200 | — | ns | A7.1 |
| 2 | $t_{IPWH}$ | CC[1] | D | IRQ/NMI Pulse Width High | 200 | — | ns | A7.2 |
| 3 | $t_{ICYC}$ | CC[1] | D | IRQ/NMI Edge to Edge Time[2] | 400 | — | ns | A7.3 |

[1] Parameter values guaranteed by design.

[2] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.
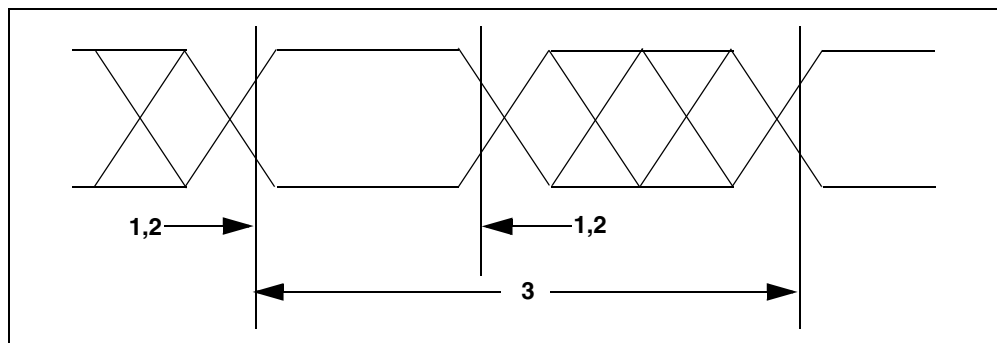


**Figure 35. IRQ and NMI Timing**

## 4.19.8 eMIOS timing

**Table 69. eMIOS timing[1]**

| Num | Symbol | C | | Characteristic | Min. value[2] | Max. value | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{MIPW}$ | CC[3] | D | eMIOS Input Pulse Width | 4 | — | $t_{CYC}$ | A8.1 |
| 2 | $t_{MOPW}$ | CC[3] | D | eMIOS Output Pulse Width | 1 | — | $t_{CYC}$ | A8.2 |

[1] eMIOS timing specified at $f_{SYS}$ = 64 MHz, $V_{DD12}$ = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, $T_A$ = -40 to 105 °C, and CL = 50 pF with SRC = 0b00.

[2] There is no limitation on the peripheral for setting the minimum pulse width, the actual width is restricted by the pad delays. Refer to the pad specification section for the details.

[3] Parameter values guaranteed by design.

## 4.19.9 FlexCAN timing

The CAN functions are available as TX pins at normal IO pads and as RX pins at the always on domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup if configured.

**Table 70. FlexCAN timing[1]**

| Num | Symbol | | C | Characteristic | Min. value | Max. value | Unit | SpecID |
|-----|--------|--------|---|----------------|------------|------------|------|--------|
| 1 | $t_{CANOV}$ | CC[2] | D | CTNX Output Valid after CLKOUT Rising Edge (Output Delay) | — | 22.48 | ns | A10.1 |
| 2 | $t_{CANSU}$ | CC[2] | D | CNRX Input Valid to CLKOUT Rising Edge (Setup Time) | — | 12.46 | ns | A10.2 |

[1] FlexCAN timing specified at $f_{SYS}$ = 64 MHz, $V_{DD12}$ = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, $T_A$ = -40 to 105 °C, and CL = 50 pF with SRC = 0b00.

[2] Parameter values guaranteed by design.

## 4.19.10 Deserial Serial Peripheral Interface (DSPI)

**Table 71. DSPI Timing[1]**

| Num | Symbol | C | | Characteristic | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{SCK}$ | $CC^2$ | D | SCK Cycle TIme[3,4] | 60[5] | — | ns | A11.1 |
| 2 | $t_{CSC}$ | $CC^2$ | D | PCS to SCK Delay[6] | - | — | ns | A11.2 |
| 3 | $t_{ASC}$ | $CC^2$ | D | After SCK Delay[7] | 20 | — | ns | A11.3 |
| 4 | $t_{SDC}$ | $CC^2$ | D | SCK Duty Cycle | $t_{SCK}/2$ −2ns | $t_{SCK}/2$ + 2ns | ns | A11.4 |
| 5 | $t_A$ | $CC^2$ | D | Slave Access Time (PCSx active to SOUT driven) | — | 25 | ns | A11.5 |
| 6 | $t_{DIS}$ | $CC^2$ | D | Slave SOUT Disable Time (PCSx inactive to SOUT High-Z or invalid) | — | 25 | ns | A11.6 |
| 7 | $t_{SUI}$ | $CC^2$ | D | Data Setup Time for Inputs<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA = 0)[8]<br>Master (MTFE = 1, CPHA = 1) | <br>20<br>10<br>5<br>35 | <br>—<br>—<br>—<br>— | <br>ns<br>ns<br>ns<br>ns | A11.7 |
| 8 | $t_{HI}$ | $CC^2$ | D | Data Hold Time for Inputs<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA = 0)[8]<br>Master (MTFE = 1, CPHA = 1) | <br>−4<br>10<br>26<br>−4 | <br>—<br>—<br>—<br>— | <br>ns<br>ns<br>ns<br>ns | A11.8 |
| 9 | $t_{SUO}$ | $CC^2$ | D | Data Valid (after SCK edge)<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA=0)<br>Master (MTFE = 1, CPHA=1) | <br>—<br>—<br>—<br>— | <br>15<br>20<br>30<br>15 | <br>ns<br>ns<br>ns<br>ns | A11.9 |
| 10 | $t_{HO}$ | $CC^2$ | D | Data Hold Time for Outputs<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA = 0)<br>Master (MTFE = 1, CPHA = 1) | <br>−15<br>5.5<br>0<br>−15 | <br>—<br>—<br>—<br>— | <br>ns<br>ns<br>ns<br>ns | A11.10 |

[1]  DSPI timing specified at VDDE_x = 3.0 V to 3.6 V, $T_A$ = -40 to 105 °C, and CL = 50 pF with SRC = 0b10.

[2]  Parameter values guaranteed by design.

[3]  The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate.

[4]  The actual minimum SCK Cycle Time is limited by pad performance.

[5]  Maximum clock possible is System clock/2.

[6]  The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK], program PSSCK=2 & CSSCK = 2.

[7]  The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

[8]  This delay value is corresponding to SMPL_PT=00b which is bit field 9 and 8 of DSPI_MCR register.
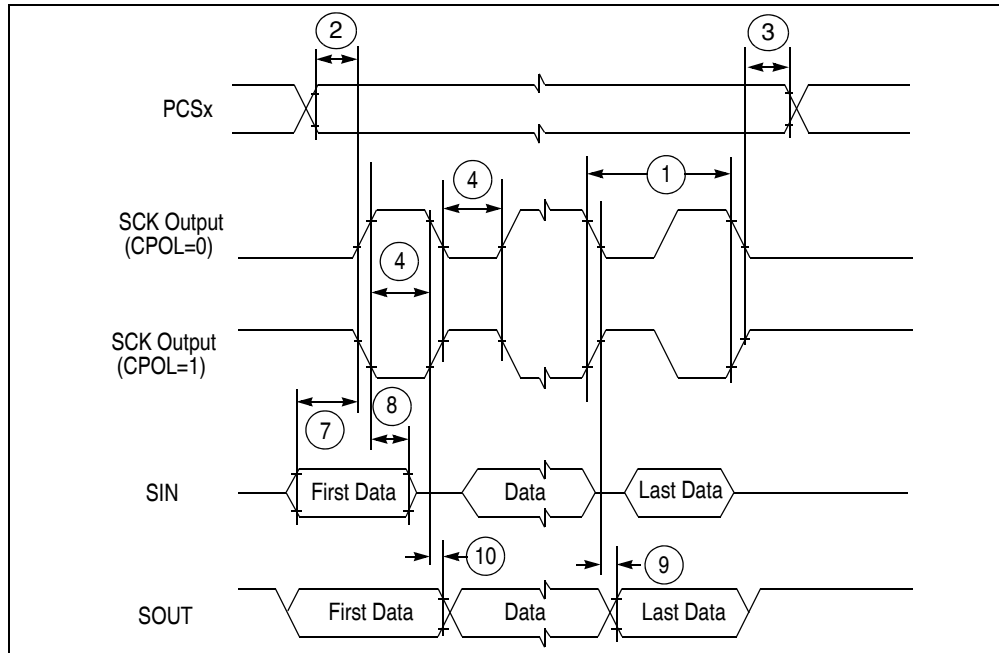
**Figure 36. DSPI Classic SPI Timing — Master, CPHA = 0**
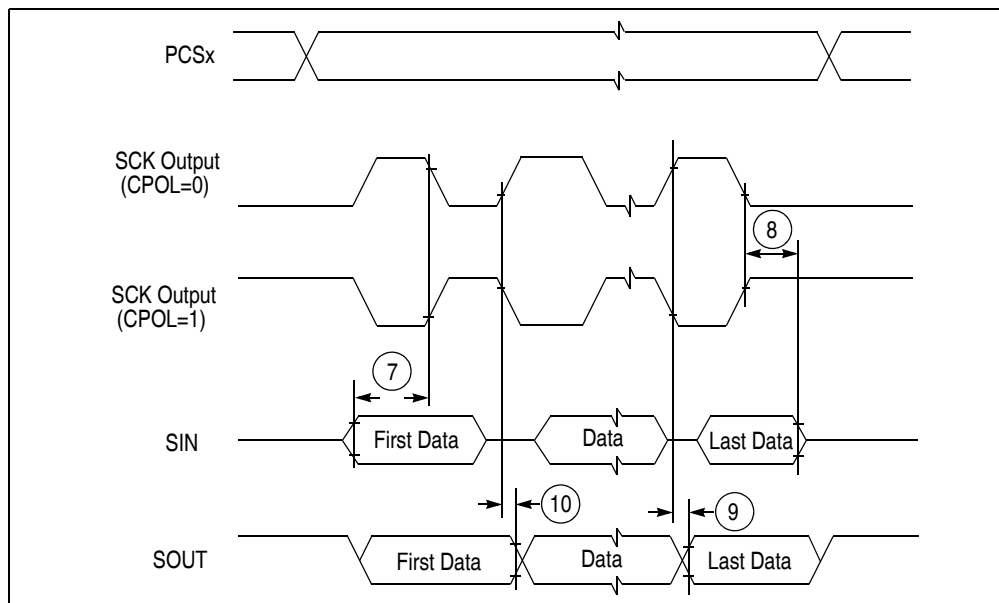


**Figure 37. DSPI Classic SPI Timing — Master, CPHA = 1**

**MPC5645S Microcontroller Data Sheet, Rev. 14**

NXP Semiconductors
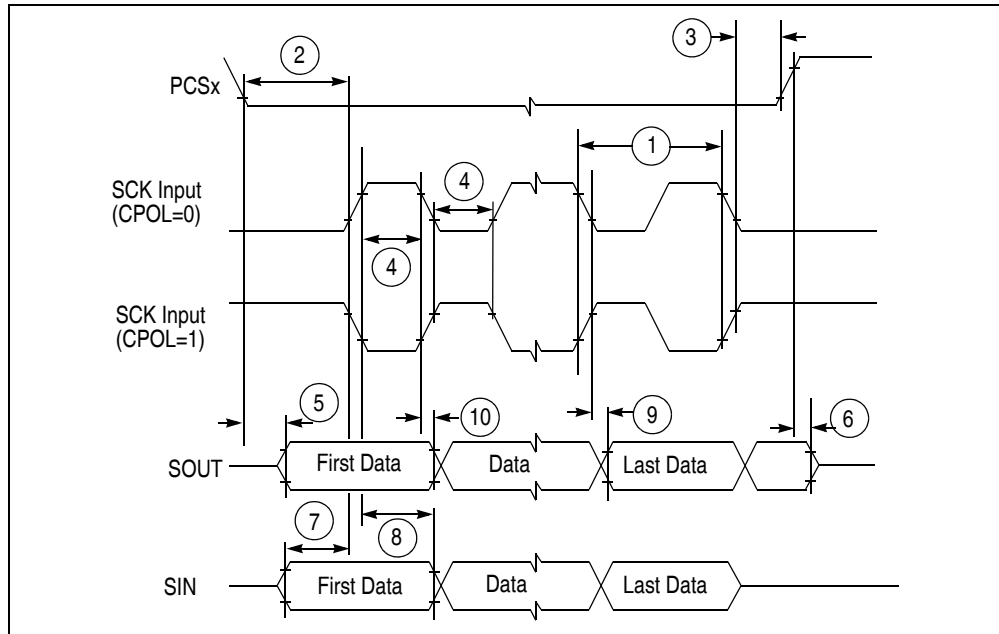
**Figure 38. DSPI Classic SPI Timing — Slave, CPHA = 0**
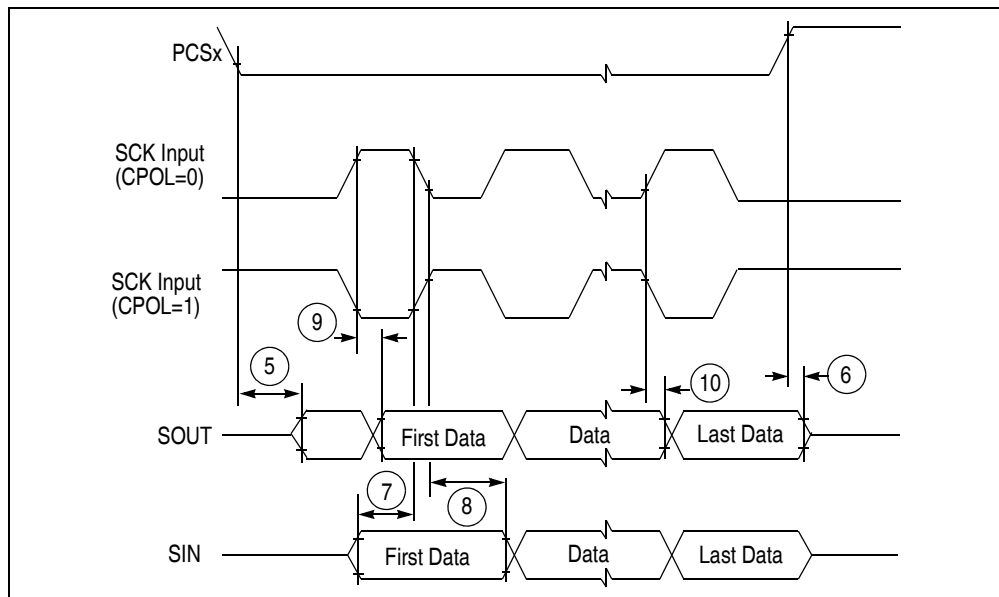


**Figure 39. DSPI Classic SPI Timing — Slave, CPHA = 1**
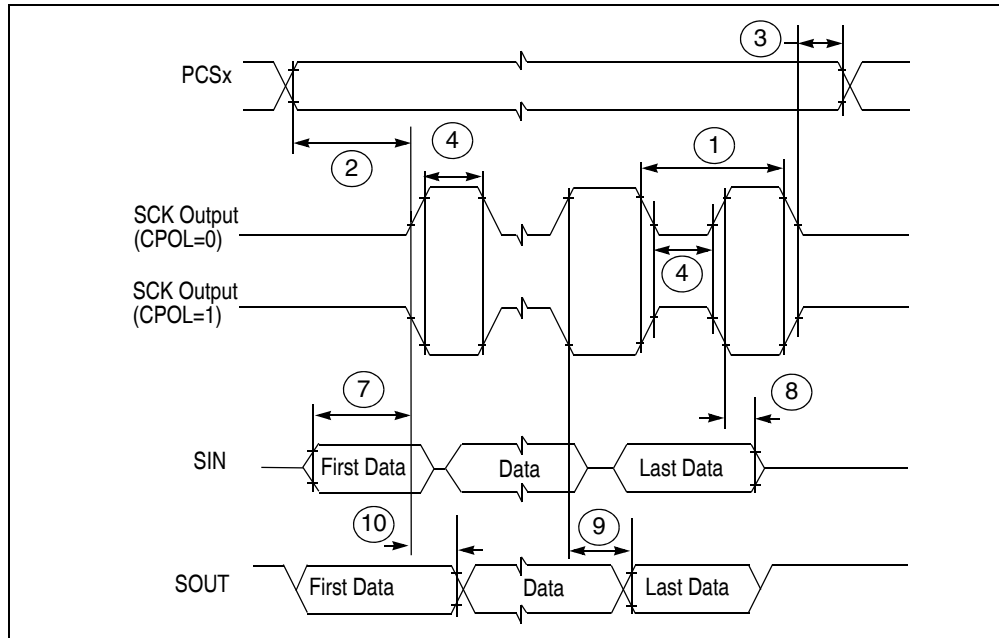
**Figure 40. DSPI Modified Transfer Format Timing — Master, CPHA = 0**
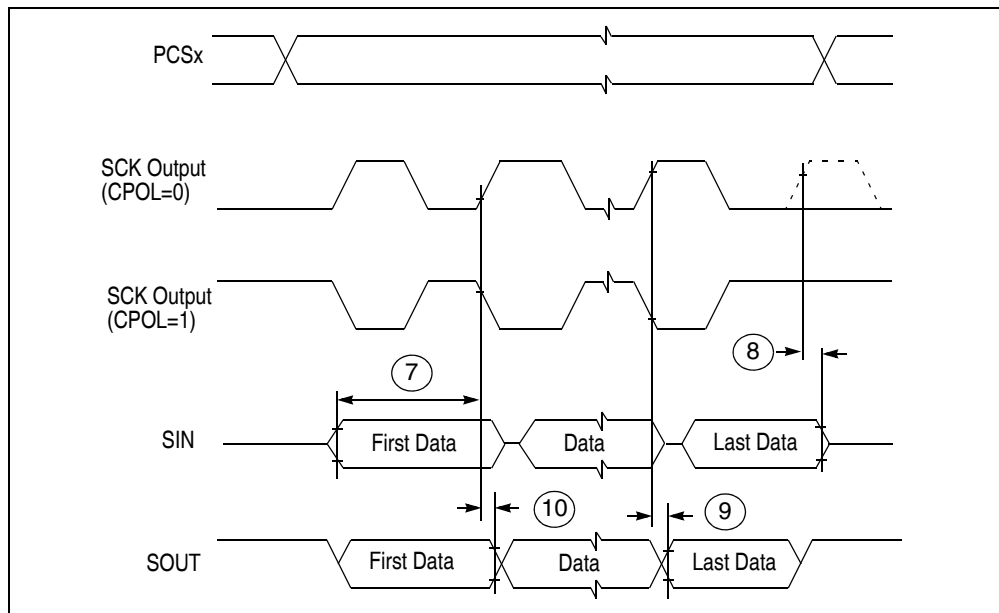


**Figure 41. DSPI Modified Transfer Format Timing — Master, CPHA = 1**

**MPC5645S Microcontroller Data Sheet, Rev. 14**

NXP Semiconductors
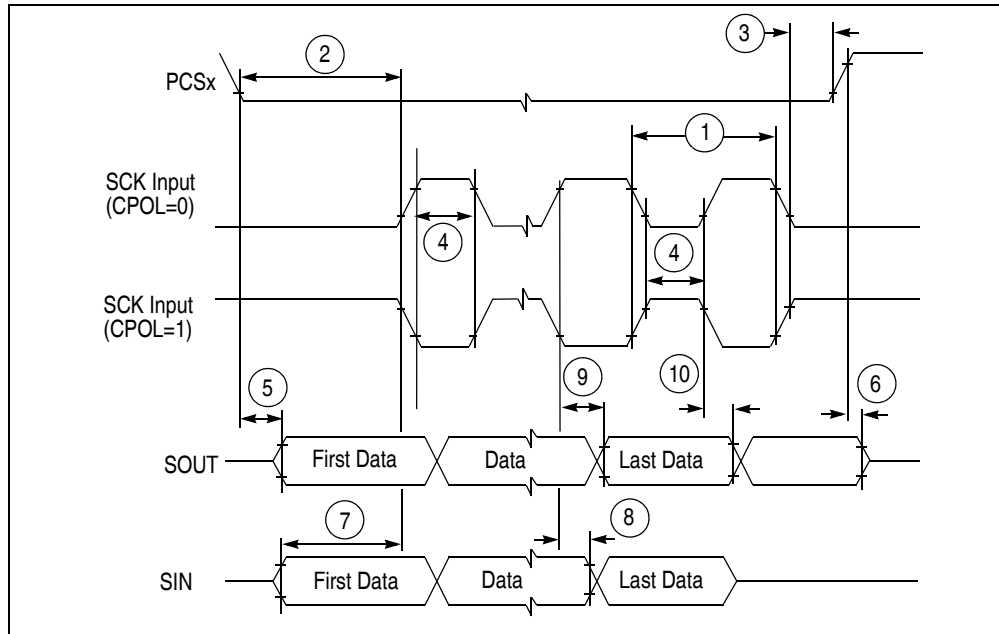
**Figure 42. DSPI Modified Transfer Format Timing — Slave, CPHA = 0**
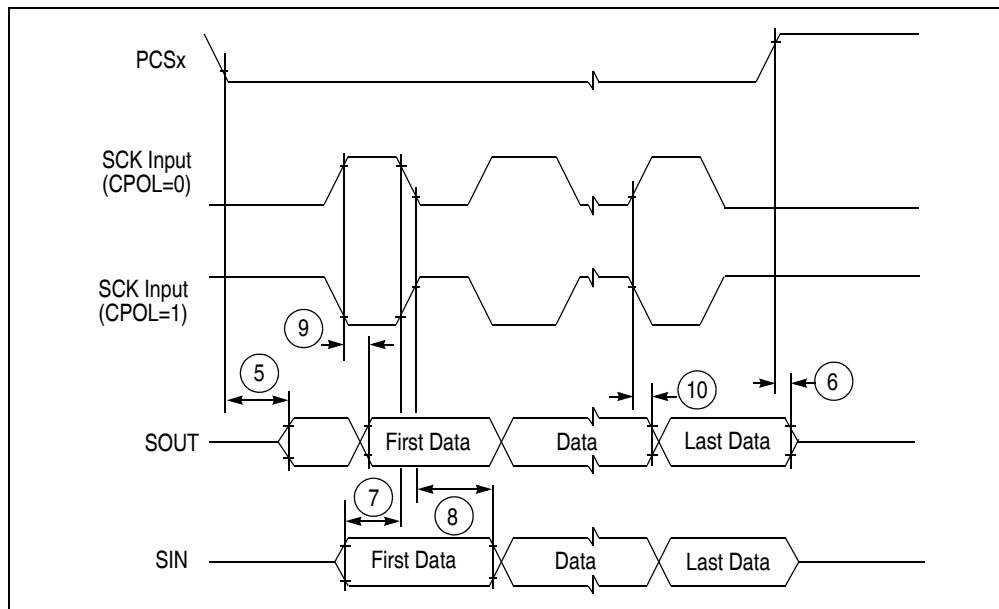


**Figure 43. DSPI Modified Transfer Format Timing — Slave, CPHA = 1**

## 4.19.11  I²C timing

**Table 72. I²C Input Timing Specifications—SCL and SDA**

| Num | Symbol | | C | Characteristic | Min. Value | Max. Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| 1 | — | CC[1] | D | Start condition hold time | 2 | — | IP-Bus Cycle[2] | A12.1 |
| 2 | — | CC[1] | D | Clock low time | 8 | — | IP-Bus Cycle[2] | A12.2 |
| 4 | — | CC[1] | D | Data hold time | 0.0 | — | ns | A12.3 |
| 6 | — | CC[1] | D | Clock high time | 4 | — | IP-Bus Cycle[2] | A12.4 |
| 7 | — | CC[1] | D | Data setup time | 0.0 | — | ns | A12.5 |
| 8 | — | CC[1] | D | Start condition setup time (for repeated start condition only) | 2 | — | IP-Bus Cycle[2] | A12.6 |
| 9 | — | CC[1] | D | Stop condition setup time | 2 | — | IP-Bus Cycle[2] | A12.7 |

[1]  Parameter values guaranteed by design.

[2]  Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

**Table 73. I²C Output Timing Specifications—SCL and SDA**

| Num | Symbol | | C | Characteristic | Min. Value | Max. Value | Unit | SpecID |
|---|---|---|---|---|---|---|---|---|
| 1[1] | — | CC[2] | D | Start condition hold time | 6 | — | IP-Bus Cycle[3] | A12.8 |
| 2[1] | — | CC[2] | D | Clock low time | 10 | — | IP-Bus Cycle[2] | A12.9 |
| 3[4] | — | CC[2] | D | SCL/SDA rise time | — | 99.6 | ns | A12.10 |
| 4[1] | — | CC[2] | D | Data hold time | 7 | — | IP-Bus Cycle[2] | A12.11 |
| 5[1] | — | CC[2] | D | SCL/SDA fall time | — | 99.5 | ns | A12.12 |
| 6[1] | — | CC[2] | D | Clock high time | 10 | — | IP-Bus Cycle[2] | A12.13 |
| 7[1] | — | CC[2] | D | Data setup time | 2 | — | IP-Bus Cycle[2] | A12.14 |
| 8[1] | — | CC[2] | D | Start condition setup time (for repeated start condition only) | 20 | — | IP-Bus Cycle[2] | A12.15 |
| 9[1] | — | CC[2] | D | Stop condition setup time | 10 | — | IP-Bus Cycle[2] | A12.16 |

[1]  Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

[2]  Parameter values guaranteed by design.

[3]  Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

[4]  Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.
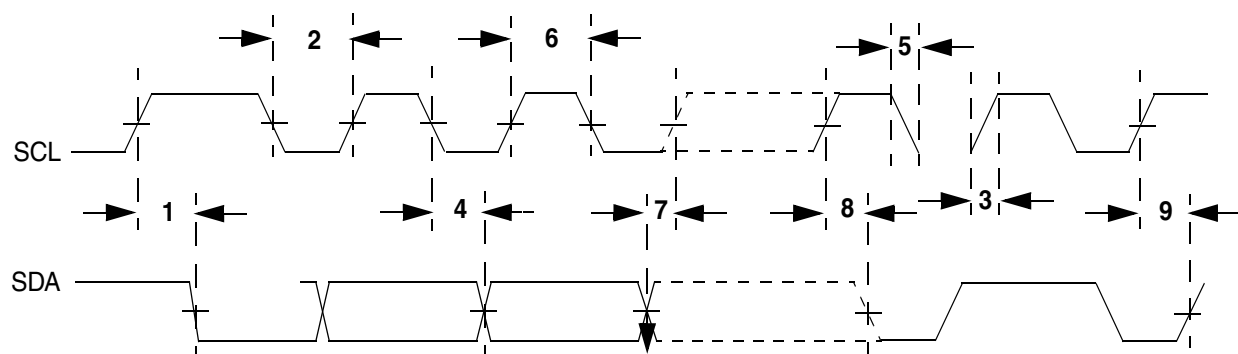
**Figure 44. I²C Input/Output Timing**

## 4.19.12 QuadSPI timing

The following notes apply to Table 74 and Table 75:

- All data is based on a negative edge data launch from MPC5645S and a positive edge data capture, as shown in the timing diagrams in this section.
- The supply conditions, over a temperature range of -45 °C to 125 °C/140 °C, are as follows:
  - IO voltage: 3.0 V, Core supply: 1.2 V
  - IO voltage: 3.3 V, Core supply: 1.2 V
  - IO voltage: 3.6 V, Core supply: 1.2 V
- The actual frequency at which the device can work will be a combination of this data and the clock pad profile.
- All measurements are considering 70% of VDDE levels for clock pin and 50% of VDDE level for data pins.
- Timings assume a setting of 0x0000_000x for QSPI_SMPR register (see the reference manual for details).
- A negative value of hold is an indication of pad delay on the clock pad (delay b/w actual edge capturing data in the device vs. edge appearing at the pin).
- Measurements are with a load of 50 pF on output pins
- The clock profile is measured at 30% to 70% levels of VDDE.

**Table 74. QuadSPI timing specifications, maximum temperature 125 °C**

| Symbol | C | | Parameter | Value | | | Unit | SpecID |
|--------|---|---|-----------|-------|-----|-----|------|--------|
| | | | | Min | Typ | Max | | |
| Tcq | CC | T | Clock to Q delay | — | — | 2.7 | ns | A13.1 |
| Ts | CC | T | Setup time for incoming data | 7.6 | — | — | ns | A13.2 |
| Th | CC | T | Hold time requirement for incoming data | 0 | — | — | ns | A13.3 |
| tr | CC | T | Clock pad rise time | 0.5 | 0.7 | 1.0 | ns | A13.4 |
| tf | CC | T | Clock pad fall time | 0.8 | 0.8 | 1.2 | ns | A13.5 |

The numbers in Figure 45 and Figure 46 correspond to events as described in Table 75.

**Table 75. QuadSPI timing events**

| Number | Event |
|--------|-------|
| 1 | Last address out |
| 2 | Address captured at flash memory |
| 3 | Data out from flash memory |
| 4 | Ideal data capture edge |
| 5 | Delayed data capture edge with QSPI_SMPR=0x0000_000X |
| 6 | Delayed data capture edge with QSPI_SMPR=0x0000_002X |
| 7 | Delayed data capture edge with QSPI_SMPR=0x0000_004X |
| 8 | Delayed data capture edge with QSPI_SMPR=0x0000_006X |
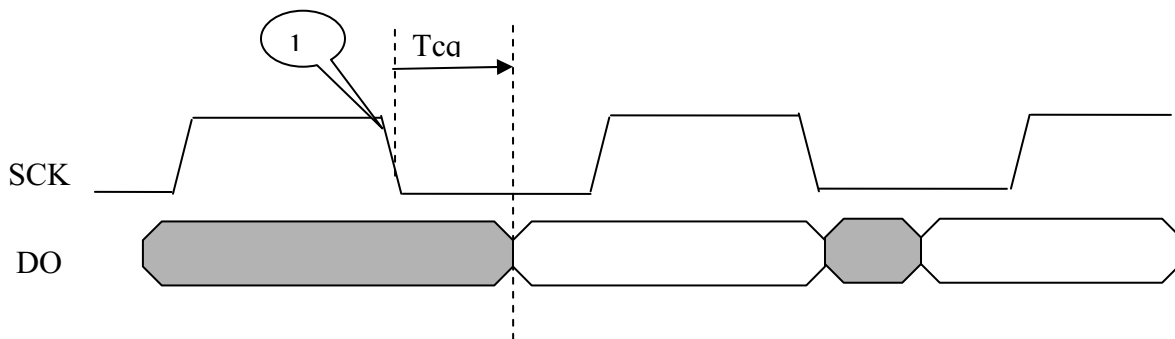


**Figure 45. QuadSPI output timing**
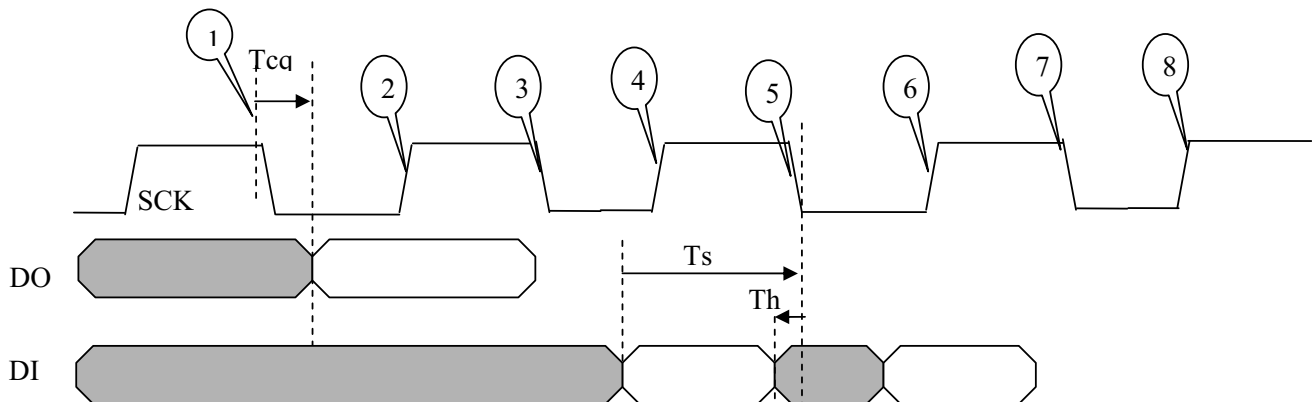


**Note:** Ts and Th correspond to QSPI_SMPR = 0x0000_000X.

**Figure 46. QuadSPI timing events**
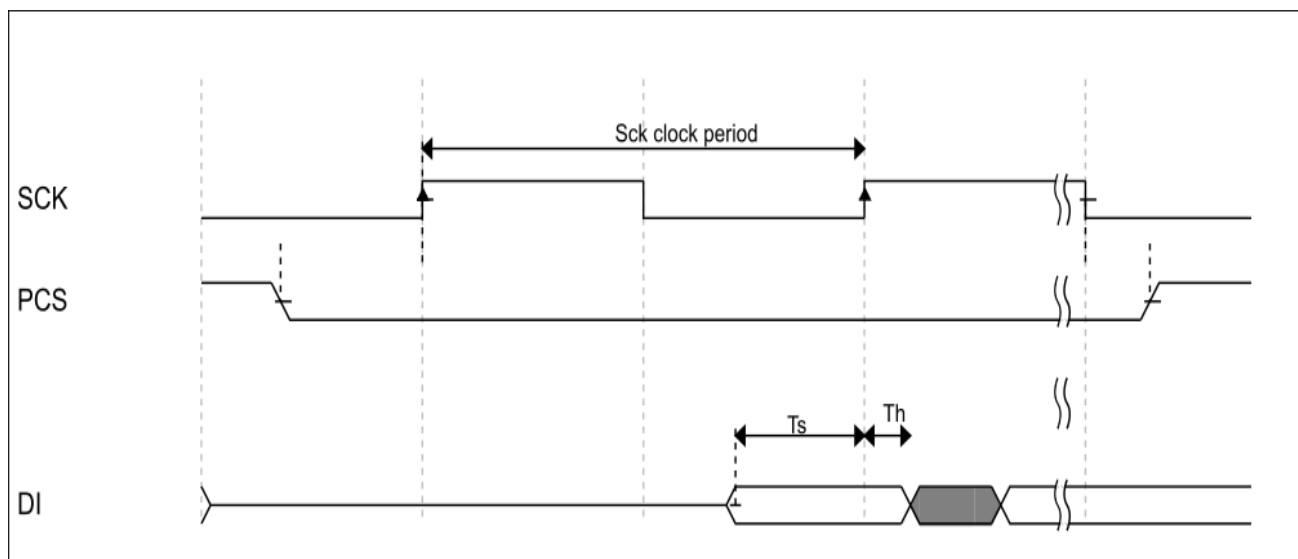
**Figure 47. QuadSPI input timing (SDR mode) diagram**

**NOTE**

The above figureis illustrative for a full cycle read timing only, actual capture edge should be inferred from Figure 46. "QuadSPI timing events".
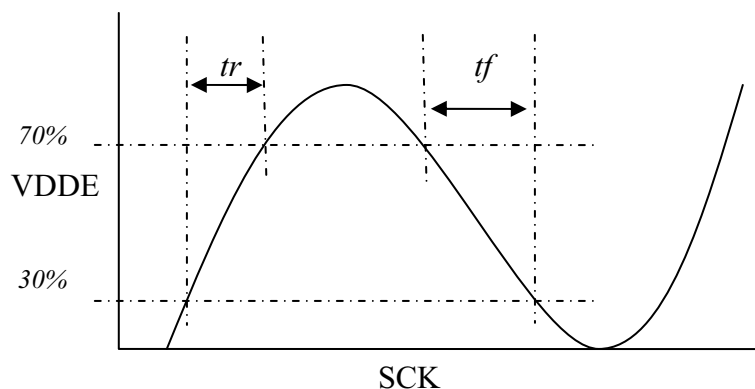


**Note:** tr and tf measured at 30% and 70% of VDDE

**Figure 48. QuadSPI clock profile**

## 4.19.13  TCON/RSDS timing

The following notes apply to Table 76:

- Measurement condition: vdde/vdd33 = 3.3 V ± 10%, vdd = 1.2 V ± 10%, vss/vsse = 0 V, T = –40–140 °C
- Termination: 100 Ω ± 5%
- VREFH_RSDS terminations of 47 µF

**Table 76. TCON/RSDS timing**

| Symbol | C | | Parameter | Condition | Value | | | Unit | SpecID |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | | Min | Typ | Max | | |
| $V_{OD}$ | CC | C | Differential output voltage | RSDS mode | 391 | — | 471 | mV | A14.1 |
| $V_{OS}$ | CC | C | Common mode voltage | 100 Ω termination between Pad_p and Pad_n | 1.17 | — | 1.4 | V | A14.2 |
| tr | CC | C | Rise time | Transition from 20% to 80% | 606 | — | 844 | ps | A14.3 |
| tf | CC | C | Fall time | Transition from 20% to 80% | 607 | — | 842 | ps | A14.4 |
| tplh | CC | D | Propagation delay, low to high | — | — | 2.65 | — | ns | A14.5 |
| tphl | CC | D | Propagation delay, high to low | — | — | 2.47 | — | ns | A14.6 |
| tdz | CC | D | Start-up time | — | — | 200 | — | μs | A14.7 |
| tskew[1][2][3] | CC | C | Skew between different RSDS lines | Max and min skew between clock and data pads | — | — | — | ps | A14.8 |

[1] There are eight programmable bits to provide 256 different skew numbers with various combinations of these bits.

[2] Default value of all the eight skew options are all "1".

[3] All "0" combination of eight bits is not valid.
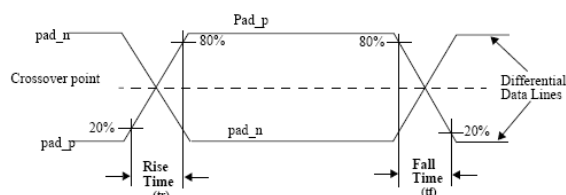


**Figure 49. Rise/fall transition, part 1**
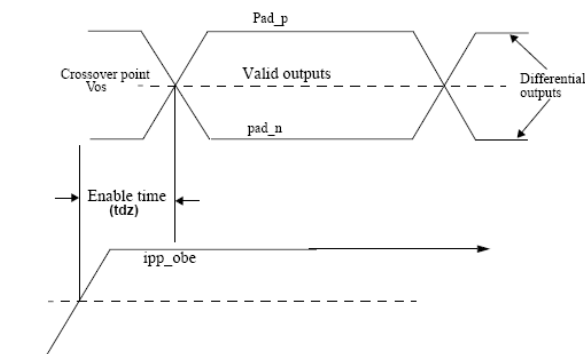


**Figure 50. Rise/fall transition, part 2**
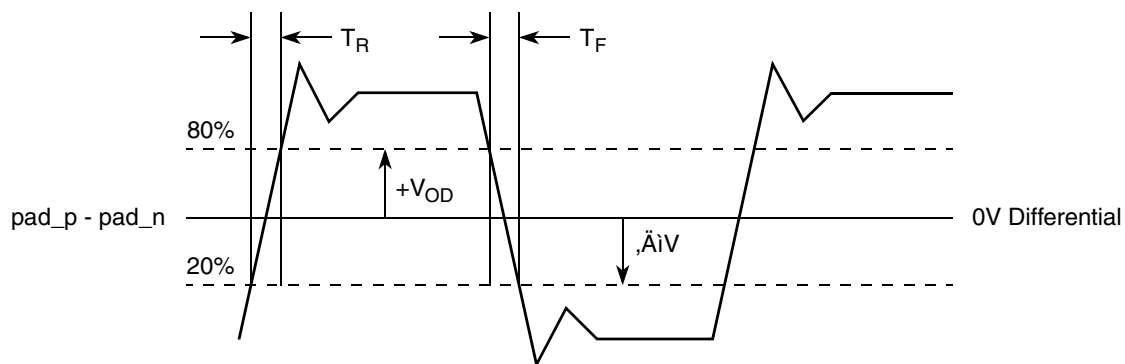
**Figure 51. Illustration of tr, tf, and V$_{OD}$**

# 5 Package mechanical data

## 5.1    176 LQFP



**Figure 52. LQFP176 Mechanical Drawing (Part 1 of 3)**

VIEW B

SECTION A—A
176 PLACES
ROTATED 90°CLOCKWISE

VIEW A

| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
|---|---|---|---|
| TITLE:<br><br>176 LD LQFP,<br>24 X 24 PKG, 0.5 PITCH, 1.4 THICK | DOCUMENT NO: 98ASS23479W | REV: C | |
| | CASE NUMBER: 1101-02 | 29 SEP 2009 | |
| | STANDARD: JEDEC MS-026 BGA | | |

**Figure 53. LQFP176 Mechanical Drawing (Part 2 of 3)**

NOTES:

1.   DIMENSIONS AND TOLERANCING PER ASME Y14.5M—1994.

2.   DIMENSIONS IN MILLIMETERS.

3.   DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE
     LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING
     LINE.

4.   DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

5.   THIS DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM C.

6.   THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS
     0.25 PER SIDE. THIS DIMENSIONS INCLUDE MOLD MISMATCH AND ARE DETERMINED
     AT DATUM PLANE H.

7.   THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION
     SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN
     PROTRUSION AND ADJACENT LEAD 0.07.

8.   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM
     AND 0.25 MM FROM THE LEAD TIP.

9.   DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE
     BODY.

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|---|---|---|---|
| TITLE:<br><br>176 LD LQFP,<br>24 X 24 PKG, 0.5 PITCH, 1.4 THICK | DOCUMENT NO: 98ASS23479W | REV: C | |
| | CASE NUMBER: 1101-02 | 29 SEP 2009 | |
| | STANDARD: JEDEC MS-026 BGA | | |

**Figure 54. LQFP176 Mechanical Drawing (Part 3 of 3)**

## 5.2   208 LQFP
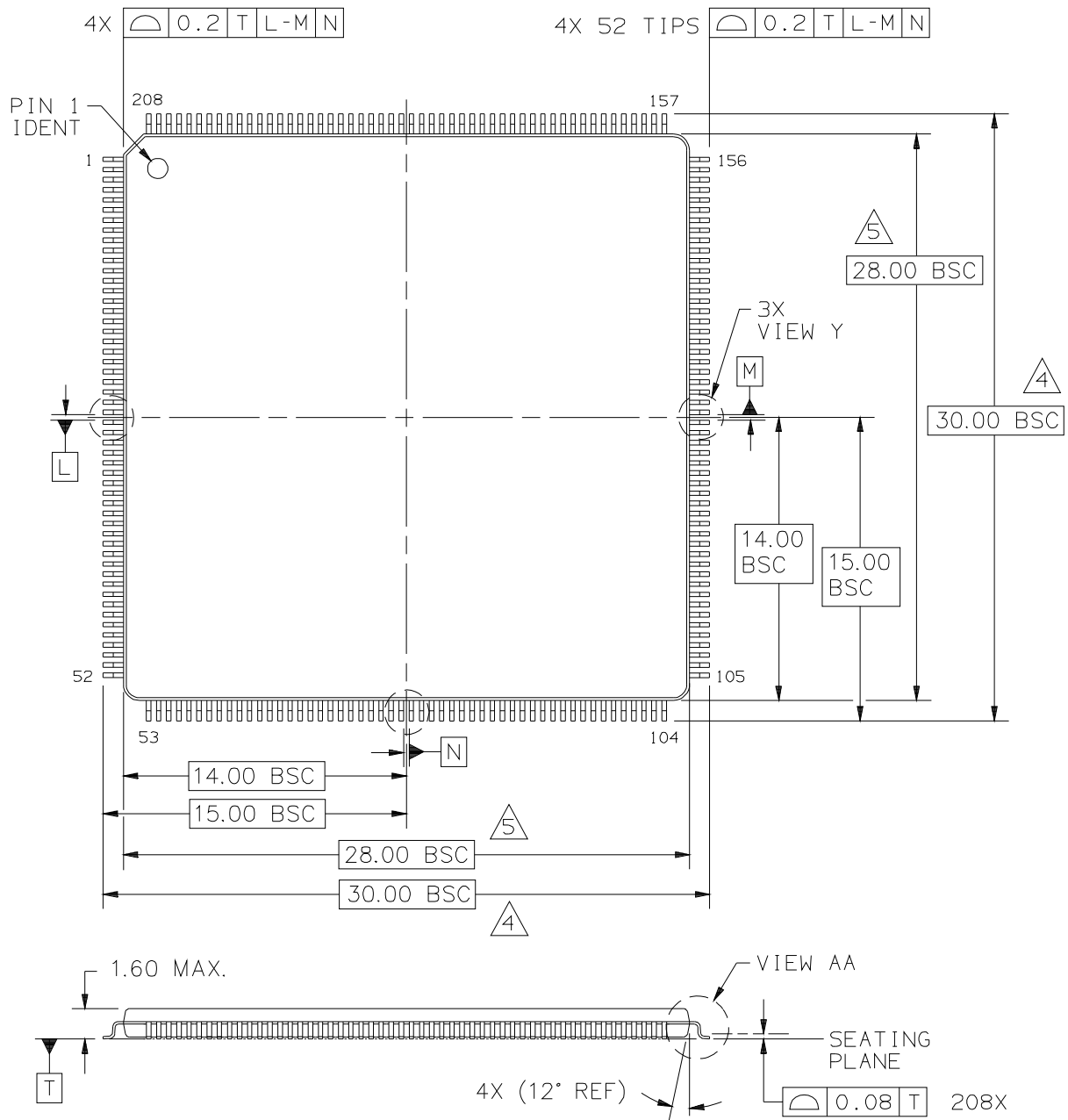
**Figure 55. LQFP208 Mechanical Drawing (Part 1 of 3)**

VIEW Y

SECTION AB-AB
ROTATED 90° CLOCKWISE
208 PLACES

VIEW AA

| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
|---|---|---|---|
| TITLE:<br>208 LD TQFP,<br>28 X 28 PKG, 0.50 PITCH, 1.4 THICK | DOCUMENT NO: 98ASS23458W | REV: C | |
| | CASE NUMBER: 998-01 | 20 MAY 2005 | |
| | STANDARD: JEDEC MS-026 BJB | | |

**Figure 56. LQFP208 Mechanical Drawing (Part 2 of 3)**

NOTES
1.    DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.

2.    DIMENSIONS IN MILLIMETERS.

3.    DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.

4.    DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM T.

5.    DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.  ALLOWABLE
      PROTRUSION IS 0.25 PER SIDE.  DIMENSIONS INCLUDE
      MOLD MISMATCH.

6.    DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION
      SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM
      SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

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|---|---|---|---|
| TITLE:<br><br>208 LD TQFP,<br>28 X 28 PKG, 0.50 PITCH, 1.4 THICK | DOCUMENT NO: 98ASS23458W | REV: C | |
| | CASE NUMBER: 998-01 | 20 MAY 2005 | |
| | STANDARD: JEDEC MS-026 BJB | | |

**Figure 57. LQFP208 Mechanical Drawing (Part 3 of 3)**

## 5.3    416 TEPBGA
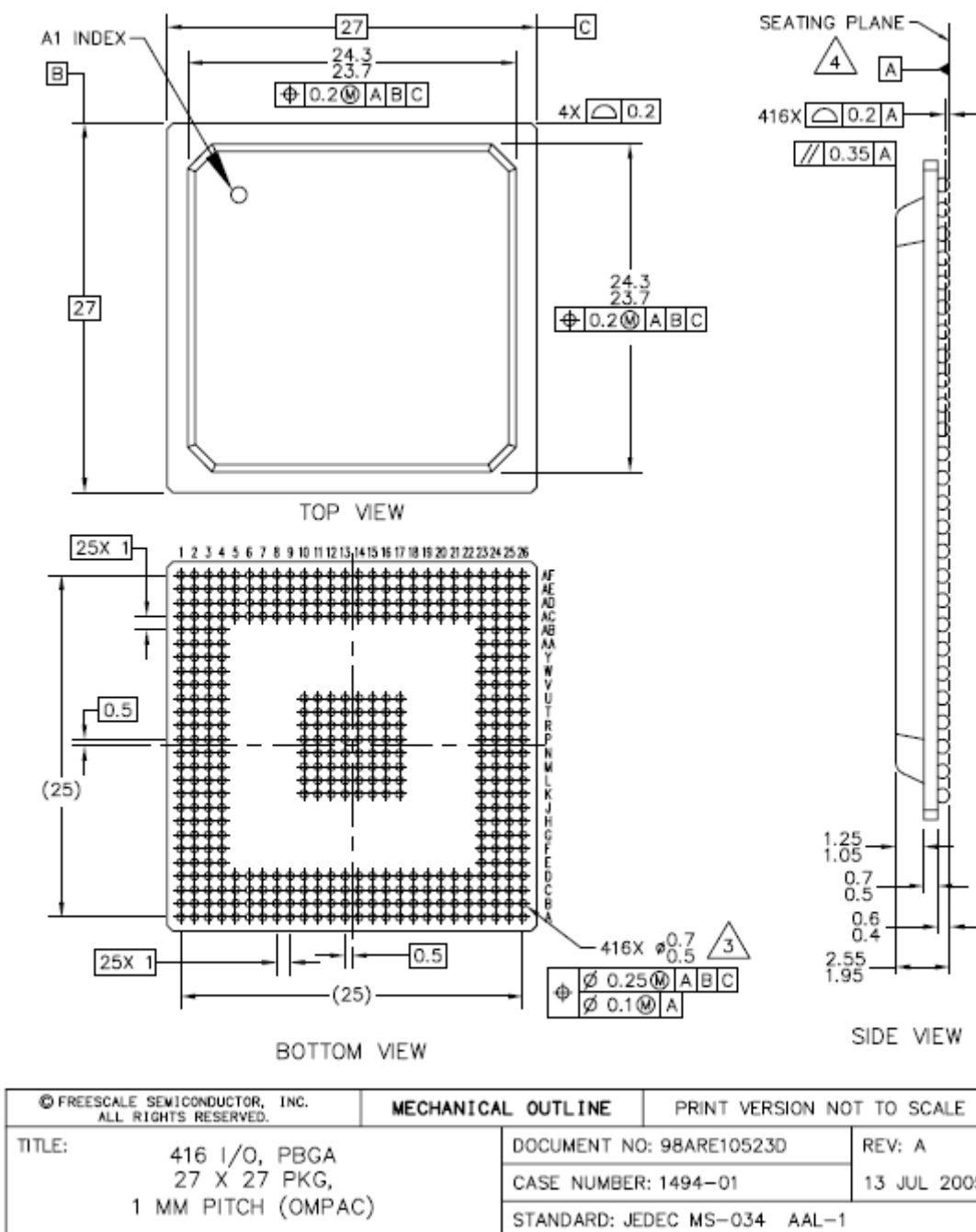


**Figure 58. 416 TEPBGA Mechanical Drawing (Part 1 of 2)**

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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|---|---|---|---|
| TITLE: 416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC) | DOCUMENT NO: 98ARE10523D | | REV: A |
| | CASE NUMBER: 1494−01 | | 13 JUL 2005 |
| | STANDARD: JEDEC MS−034   AAL−1 | | |

**Figure 59. 416 TEPBGA Mechanical Drawing (Part 2 of 2)**

# 6 Ordering information
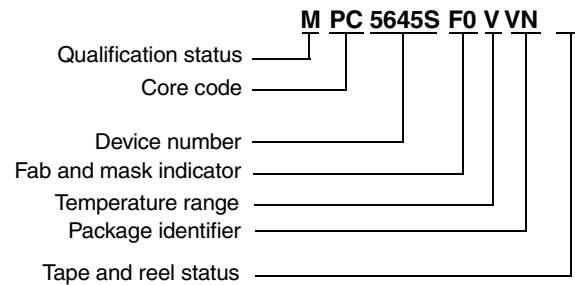


**Temperature range**

C = -40 C to 85 C
V = -40 C to 105 C

**Package identifier**

LU = 176 LQFP Pb-free
LT = 208 LQFP Pb-free
VU = 416 TEPBGA Pb-free

**Tape and reel status**

R = Tape and reel
(blank) = Trays

**Qualification status**

P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

**Note:** Not all options are available on all devices. Refer to Table 77.

**Figure 60. Commercial product code structure**

**Table 77. Orderable part number summary**

| Part number | Flash/SRAM | Package | Speed (MHz) |
|---|---|---|---|
| SPC5645SF1VLU | 2 MB/64 KB | 176 LQFP (Pb free) | 125 |
| SPC5645SF1VLT | 2 MB/64 KB | 208 LQFP (Pb free) | 125 |
| SPC5645SF1VVU | 2 MB/64 KB | 416 TEPBGA (Pb free) | 125 |

# 7 Revision history

**Table 78. Revision history**

| Revision (Date) | Description |
|---|---|
| 1 (06 Oct 2009) | Initial release. |
| 2 (7 Dec 2009) | Editorial changes.<br>Extensive modifications throughout the "Pinout and signal descriptions" section.<br>Revised the "Absolute maximum ratings" table.<br>Revised the "Recommended operating conditions (3.3 V)" table.<br>Revised the "Recommended operating conditions (5 V)" table.<br>In the "Voltage regulator electrical characteristics" section, changed "NJD2783" to NJD2873".<br>Revised the "Interface to TFT LCD panels" section. |
| 3 (3 Mar 2010) | Editorial changes.<br>Added the RoHS logo (indicating RoHS compliance).<br>Added a "SpecID" column to specification tables throughout the document.<br>In the device-comparison table:<br>• Revised the "Timed I/O" entry.<br>• Changed "Nexus 3" to "Nexus Class 3".<br>In the feature list:<br>• Revised the information for the TCON and RSDS interface.<br>• In the ADC entry, changed "20 internal channels" to "Up to 20 internal channels".<br>• In the QuadSPI entry, changed "quad modes of operation" to "quad IO serial flash memory".<br>• In the DCU3 and DCULite entry, changed "WVGA" to "XGA".<br>In the "Feature details" section:<br>• Revised some module abbreviations and names to be consistent with the rest of the documentation.<br>• In the GFX2D section, deleted "and Adobe Flash 7".<br>• In the QuadSPI section, changed "Maximum frequency 80 MHz" to "Maximum serial clock frequency 80 MHz"<br>• In the FlexCAN section, changed "The FlexCan modules offer" to "Each FlexCAN module offers".<br>• In the DCULite section, changed "WVGA" to "XGA".<br>In the 176-pin pinout, changed "MDD" to "MDO".<br>In the 208-pin pinout:<br>• For pin 105, changed "VDDE" to "VDDE_B".<br>• Renamed pin 145 (was VRSDS, is VREF_RSDS")<br>• For pin 148, changed "RSRS3+P" to "RSDS3P".<br>• For pin 160, changed "SCL_D" to "SCL_3".<br>• For pin 161, changed "SDA_D" to "SDA_3".<br>• For pin 178, changed "DCULITE_G8" to "DCULITE_G6".<br>In the 324-pin pinout:<br>• Renamed pin A1 (was VSS_DR, is VSS).<br>• Renamed pin B2 (was VDDE_DDR, is VDD_DR).<br>• Renamed pins D11 and J9 (were VDD33_DR, are VDDE_B).<br>Added the "Pad configuration during reset phases" section.<br>In the "Voltage supply pin descriptions" table:<br>• Renamed $V_{RSDS}$ to $V_{REF\_RSDS}$ and added a footnote about the pin's required termination.<br>• Added pin B2 to VDD_DR in the 324-pin package.<br>• Moved pins D11 and J9 to $V_{DDE\_B}$.<br>Revised the "System pin descriptions" table.<br>Replaced the entire "DRAM interface pin summary" table.<br>• In the "Nexus pins" table, added a PCR column. |

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Table 78. Revision history (continued)

| Revision (Date) | Description |
|---|---|
| 3 (continued) (3 Mar 2010) | Added the "VIU muxing" section.<br>Added the "System design information" section and a "Power-up sequencing" subsection.<br>In the "Recommended operating conditions (3.3 V)" table, revised footnotes 2 and 4.<br>In the "Recommended operating conditions (5.0 V)" table, revised footnotes 3 and 5.<br>Revised the text in the "Voltage regulator electrical characteristics" section.<br>Added meaningful content to the "DC electrical characteristics" section.<br>In the "Reset electrical characteristics" table, changed the specifications for $W_{FRST}$ (was max 40 ns, is max 70 ns) and $W_{NFRST}$ (was min 1000 ns, is min 400 ns).<br>Replaced the entire "Pad AC specifications" section.<br>Added meaningful content to the "Video Input Unit timing" section.<br>Added orderable part numbers.<br>Revised the "Commercial product code structure" figure. |
| 4 (24 Jun 2010) | Editorial changes and improvements.<br>In the device-comparison table, changed the GPIO count for the 176-pin package (was 127, is 128).<br>In the feature list:<br>• Changed "4 KB, 2-way instruction cache" to "4 KB, 2/4-way instruction cache".<br>• Changed "32 kHz crystal oscillator" to "32 KHz crystal oscillator".<br>• Changed "188 peripheral interrupt sources" to "181 peripheral interrupt sources".<br>• Changed "Primary FMPLL" to "Primary FMPLL (FMPLL0)".<br>• Changed "Auxiliary FMPLL" to "Auxiliary FMPLL (FMPLL1)".<br>• In the crossbar switch description, deleted the reference to AMBA.<br>• In the SGM description, changed "WAV file" to "PCM wave".<br>• Revised the RLE decoder description.<br>• In the SIUL description, deleted "resets".<br>• In the CMU section, changed "PLL" to "primary FMPLL (FMPLL0)".<br>In the feature details:<br>• Changed "32 kHz oscillator" to "32 KHz oscillator".<br>• Changed "128 KHz oscillator" to "128 kHz oscillator".<br>• Revised the "Low-power operation" section.<br>• In the ADC section, changed "0 to 5V common mode conversion range" to "0–5 V or 0–3.3 V common mode conversion range".<br>• Revised the DCU3 section.<br>• In the "On-chip graphics SRAM" section, added an entry for independent data buffers.<br>• In the MPU section, changed "Protection offered for 3 concurrent read ports" to "Protection offered for 4 concurrent read ports".<br>In the 176-pin pinout:<br>• Added content to indicate which functions are available only in this package.<br>• For pin 116, changed PD113 to PDI13.<br>• For pin 117, changed PD114 to PDI14.<br>• For pin 1, changed DCU_VSYNC_TCON2 to DCU_VSYNC.<br>• For pin 2, changed DCU_HSYNC_TCON1 to DCU_HSYNC.<br>• For pin 3, changed DCU_DE_TCON3 to DCU_DE.<br>• For pin 16, changed DCU_TAG_TCON3 to DCU_TAG.<br>• For pin 56, changed PDI0(VIU0) to PDI0_VIU0.<br>• For pin 57, changed PD11(VIU1) to PDI1_VIU1.<br>• For pin 58, changed PDI12(VIU2) to PDI2_VIU2.<br>• For pin 59, changed PDI3(VIU3) to PDI3_VIU3.<br>• For pin 148, deleted TCON0.<br>• For pin 155, deleted DCULITE_G7. |

**Table 78. Revision history (continued)**

| Revision (Date) | Description |
|---|---|
| 4 (continued) (24 Jun 2010) | In the 208-pin pinout:<br>• For pin 68, changed eMIOSA23 to eMIOS0[23].<br>• For pin 69, changed eMIOSA16 to eMIOS0[16].<br>• For pin 70, changed eMIOSA15 to eMIOS0[15].<br>• For pin 71, changed eMIOSA14 to eMIOS0[14].<br>In the 324-pin pinout:<br>• Added content to indicate which functions are available only in this package.<br>• Renamed pin J10 (was VSS_DR, is VSS).<br>In the "Voltage supply pin descriptions" table:<br>• Deleted the entry for VSS_DR.<br>• Added pin J10 to the VSS group in the 324-pin package.<br>Revised the "Nexus pins" table.<br>In the "Recommended operating conditions (3.3 V)" table, changed the specification for $TV_{DD}$ (was 0.25 V/μs, is 12 V/ms).<br>In the "Recommended operating conditions (5.0 V)" table, changed the specification for $TV_{DD}$ (was 0.25 V/μs, is 12 V/ms).<br>In the "FMPLL electrical characteristics" table, changed footnote 6 (was "$f_{CPU}$ 64 MHz can be achieved only at up to 105 °C", is "$f_{CPU}$ of 125 MHz can be achieved only at temperatures up to 105 °C with a maximum FM depth of 2%.".)<br>In the "DC specification for CMOS090LP2 library @ VDDE = 3.3 V" > "DC electrical specifications" table, deleted the specifications for Vih_pci and Vil_pci.<br>Revised the "Low power oscillator electrical characteristics" table.<br>In the "ADC electrical characteristics" table, changed "$V_{DD}$-0.1" to "$V_{DDE\_A}$–0.1" and "$V_{DD}$+0.1" to "$V_{DDE\_A}$+0.1".<br>Renamed "QuadSPI2 Timing" to "QuadSPI timing" and added meaningful content.<br>Added the "TCON/RSDS timing" section. |
| 5 (25 Feb 2011) | In the "Feature List" section:<br>• Changed RTC optional clocking from "main" to "fast" 4-16 MHz external oscillator.<br>• Changed CMU monitor feature from "main crystal oscillator" to "fast (4–16 MHz) external crystal oscillator".<br>In the "Feature details" section, changed "main oscillator" to "external oscillator" in the "System clocks and clock generation modules" section.<br>In the "Pad configuration during reset phases" section, changed "Main oscillator pads" to "Fast (4-16 MHz oscillator pads".<br>In the ""Voltage supply pin descriptions" table, changed $V_{DD\_DR}$ function from "DDR SDRAM interface supply" to "1.8V, 2.5V, and 3.3V SDRAM supply"<br>In the "System pin descriptions" table, specified an external capacitor value of 47pF in the footnote.<br>In the "Functional ports" section, added list of pad types.<br>In the "Power-up sequencing" section:<br>• Added list item that specifies VDDE_B and VDD33_DR are to be powered up first.<br>• Added VDD33_DR to the list of generic I/O or noise-free supplies.<br>• Added details to VREG HV list item.<br>• Changed post-list text regarding DDR to be a separate NOTE, and identified the 3.3V supply as VDD33_DR.<br>• Added power-up information to the LV supply (VDD12) list item.<br>• Added "Parameter classification" section and accompanying table.<br>Added "C" classification column and values to tables throughout the "Electrical characteristics" section. |

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**Table 78. Revision history (continued)**

| Revision (Date) | Description |
|---|---|
| 5 (continued) (25 Feb 2011) | In the "Absolute maximum ratings" table:<br>• Changed max value for $V_{DDE\_B}$ from 5.5V to 3.6 V.<br>• Changed max value for $V_{DD\_DR}$ from TBD to 3.6 V.<br>• Changed max value for $V_{RSDS}$ from TBD to 3.6 V.<br>• Changed max value for $V_{IN}$ from 5.5V to "$V_{DDmax}$ (VDDE max of that segment)".<br>• Removed "Relative to $V_{DD}$" condition for $V_{IN}$.<br>In the "Recommended operating conditions (3.3 V)" table:<br>• Changed min value for "$V_{DD}$" from 3.0 V to "$V_{DDmin}$".<br>• Changed max value for "$V_{DD}$" from 3.6 V to "$V_{DDmax}$".<br>• Changed $V_{DD}$ entry to include only $V_{DDE\_A}$, $V_{DDE\_B}$, $V_{DD\_DR}$, and $V_{DDM}$.<br>• Corrected error in $V_{DDE\_A}$ entry, changed reference in "parameter" column from $V_{DDE\_C}$ to $V_{DDE\_A}$.<br>• Added $V_{DD\_DR}$ to the $V_{DD}$ footnote.<br>In the "Recommended operating conditions (5.0 V)" table:<br>• Added footnote for $V_{DDE\_B}$ max values.<br>• Added footnote for $V_{DD\_DR}$ typ values.<br>• Changed min and max values for $V_{DD\_DR}$ from 4.5V and 5.5V to 3.0V and 3.6V, respectively.<br>• Changed max value for $V_{DD\_DR}$ (under "voltage drop" conditions) from 5.5V to 3.6V.<br>• Changed min and max values for $V_{DD}$ from 4.5V and 5.5V to $V_{DDmin}$ and $V_{DDmax}$, also referenced footnote 6.<br>• Removed VDDE_C and VDDE_E from the VDD "parameter" description and footnote, and added VDD_DR.<br>• Changed min and max values for $V_{DDE\_B}$ from 4.5V and 5.5V to 3.0V and 3.6V, respectively.<br>Removed the "Libraries" column from the DC specifications "library" tables.<br>Removed the 75Ω and 50Ω cases and added details on the 150Ω case in the "ODT DC electrical characteristics" table.<br>Changed the "Main oscillator electrical characteristics" section name to "Fast external crystal oscillator (4-16 MHz) electrical characteristics" and modified text and table name within the section appropriately.<br>Removed the "Full swing Pierce" condition and the relevant footnotes from the "Fast external crystal oscillator (4-16 MHz) electrical characteristics" table.<br>Changed the "Low power oscillator electrical characteristics" section name to "Slow external crystal oscillator (32 KHz) electrical characteristics" and modified the text, figure, and table names within the section appropriately.<br>Changed "main oscillator" to "fast external oscillator" in the "FMPLL electrical characteristics" table.<br>Updated parameters, conditions, and values in the "FMPLL electrical characteristics" table.<br>Changed the "Main RC oscillator electrical characteristics" section name to "Fast Internal RC oscillator (16 MHz) electrical characteristics" and modified the text and table name within the section appropriately.<br>Changed the "Low power RC oscillator electrical characteristics" section name to "Slow Internal RC oscillator (128 KHz) electrical characteristics" and modified the text and table name within the section appropriately.<br>Removed duplicate entry of TUEP in the "ADC electrical characteristics" table.<br>Removed pad_pci and pad_osc48 from the "Functional pad type AC specifications" table because they are not used.<br>Added new "Pad mode configurations" table to the "DRAM Interface" section.<br>Changed the 324-pin TEPBGA pinout to 416-pin TEPBGA.<br>Changed the 324-pin TEPBGA mechanical drawing to 416-pin TEPBGA. |

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**Table 78. Revision history (continued)**

| Revision (Date) | Description |
|---|---|
| 5 (continued) (25 Feb 2011) | In the "Operating mode summary" table:<br>• Changed the "RAM" column to "SRAM".<br>• Changed "STOP" for "16MHz IRC" from "OP" to "On".<br>• Changed "STOP" for "Graphics RAM" from "On" to "CG".<br>• Changed "STANDBY" for "128KHz IRC" from "OP" to "ON" (both cases).<br>Changed "324BGA" to "416BGA" in the "Nexus Development Interface (NDI)" section.<br>Updated all data in the "Thermal characteristics for 176-pin LQFP" table.<br>Updated all data in the "Thermal characteristics for 208-pin LQFP" table.<br>Changed "324" in the "Thermal characteristics for 324-pin TEPBGA" table title to "416".<br>Added Spec ID numbers to the "DC electrical specifications" tables throughout the "DC electrical specifications" section.<br>Updated the NOTE reference details in the "DC specification for CMOS090LP2 library @ VDDE = 3.3 V" and "DC specification for CMOS090LP2fg library @ VDDE = 5.0 V" sections.<br>Added Spec ID numbers to the "QuadSPI timing specifications" tables.<br>Added Spec ID numbers to the "TCON/RSDS timing" table.<br>Added values into the empty cells in the "TCON/RSDS timing" table.<br>In the "Orderable part number summary" table:<br>• Changed "324" to "416".<br>• Updated the part numbers.<br>Corrected presentation problem with the 176 LQFP figure. |
| 6 (09 Aug 2011) | Changed "324" to "416" in the "SC667108 device comparison" table.<br>Changed I/O direction for EXTAL from "O" to "I" in the "System pin descriptions" table.<br>Changed I/O direction for XTAL from "I" to "O" in the "System pin descriptions" table.<br>In the "$V_{DDE\_A}$" entry of the "Recommended operating conditions (3.3 V)" table, changed "$V_{SSE\_C}$" to "$V_{SSE\_A}$".<br>In the "$V_{DDE\_A}$" entry of the "Recommended operating conditions (5.0 V)" table, changed "VDDE_C" to "VDDE_A".<br>In the "$V_{DDE\_A}$" entry of the "Recommended operating conditions (3.3 V)" table, changed "$V_{SSE\_C}$" to "$V_{SSE\_A}$".<br>In the "$V_{SS}$" footnote of the "Recommended operating conditions (5.0 V)" table, changed "$V_{SSE\_C}$" to "$V_{SSE\_A}$".<br>Removed "QuadSPI timing specifications, maximum temperature 150 C" table.<br>Removed "DC electrical characteristics" table in "Low voltage domain power consumption" section and inserted a new table.<br>In the "Supply leakage" table, changed "spor" to "spcr".<br>Removed "pad_multv_hv" and "pull_hv" entries from "Functional pad type AC specifications" table.<br>Removed "pad_multv_hv", "pad_io_hv" and "lvds_ref_hv" entries from "Supply leakage" table.<br>Updated values in "VIU2 timing parameters" table.<br>Removed "pad_fsr" and "pad_pci" parameters from "Supply leakage" table.<br>Added Figure 28 - RSDS/TCON Timing Diagram<br>Added four tables in "DRAM interface" section. |

Table 78. Revision history (continued)

| Revision (Date) | Description |
|---|---|
| 7 (7 Feb 2012) | I$_{DDRUN}$ values updated in "DC electrical characteristics" table.<br>Min and max values of V$_{DD12}$ in "Voltage regulator electrical characteristics" table changed to 1.26 V and 1.29 V, respectively.<br>T$_B$ changed to T$_A$ for IDDHALT value in "DC electrical characteristics" table.<br>Removed ΔRCMTRIM values from "Fast internal RC oscillator (16 MHz) electrical characteristics" table.<br>Removed ΔRCMTRIM values from "Slow internal RC oscillator (128 KHz) electrical characteristics" table.<br>Changed max Tj to 140 C in "Recommended operating conditions (3.3V)" table.<br>Changed max Tj to 140 C in "Recommended operating conditions (3.3V)" table.<br>Changed max Tj to 140 C in "Voltage regulator electrical characteristics" table.<br>Changed spec limits on VDD12 Post-Trimming, from min=1.270, max = 1.28 to min = 1.145, max = 1.32, in "Voltage regulator electrical characteristics" table.<br>Added "Low-power voltage regulator electrical characteristics" table.<br>Added "Ultra low-power voltage regulator electrical characteristics" table.<br>Offset and gain error values changed to 0.5 and 0.6 Typ, respectively, in "ADC electrical characteristics" table.<br>Added "Power-up sequencing" and "Power-down sequencing" diagrams in "Power-up Sequencing" section.<br>Added "LPDDR, DDR and DDR2 (DDR2-250) SDRAM timing specifications" table in "DRAM Interface" section and removed specifications' tables for DDR1 mode, DDR2 mode and LPDDR mode.<br>Updated VLVDHV3H, VLVDHV3L, VLVDHV5H and VLVDHV5L values in "Low voltage monitor electrical characteristics" table.<br>Updated I$_{DDHALT}$ Typ and Max values in "DC electrical characteristics" table.<br>Changed P25 pin to VSS pin in "416 TEPBGA pinout" figure. |
| 8 (09 Aug 2012) | In "Absolute maximum Ratings" table, changed max value of V$_{DDPLL}$ from 1.32 V to 1.4 V.<br>In "DC Electrical Characteristics" table, updated max values of I$_{DDMAX}$, I$_{DDHALT}$, I$_{DDSTOP}$ and I$_{DDSTDBY1}$.<br>Removed 1.32 V value for V$_{DD}$, from "DC electrical specifications at 3.3 V VDDE", "DC electrical specifications at 2.5 V VDDE" and "DC electrical specifications at 1.8 V VDDE". |
| 9 (12 Sep 2012) | Added "Location of TCON Pins" table. |
| 10 (30 Jan 2013) | Updated Table 62.<br>Added "Section 4.19.5.1, "SDR Timings"" section.<br>Added a table note for "STOP mode current" entry in Table 22 in Section 4.7.3, "Low voltage domain power consumption"". |
| 11 (16 May 2013) | Added  Figure 7. "Pad output delay".<br>Added Table 38. "SMD pad electrical characteristics", Table 39. "SMD pad delays", and Table 40. "SSD electrical characteristics".<br>Changed Vdd max specification from 1.47 V to 1.32 V in Table 23. "DC electrical specifications", Table 30. "DC electrical specifications at 3.3 V VDDE", Table 32. "DC electrical specifications at 2.5 V VDDE", and Table 34. "DC electrical specifications for 1.8 V VDDE" |

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**Table 78. Revision history (continued)**

| Revision (Date) | Description |
|---|---|
| 12 (30 Oct 2014) | In  Figure 3. "208-pin LQFP pinout":<br>• "DCU_LITE_TAG" added and "DCU_TAG" removed for PK10.<br>• "DCU_TAG" added and "DCULITE_TAG" removed for PK11.<br>• "SDA_1" added for PL0.<br>• "SCL_1" added for PL1.<br>In Section 1.4.13, "Display Control Unit (DCU3)", added a feature "Support displays up to 800 x 480 pixel resolutions".<br>In  Figure 4. "416 TEPBGA package pinout", added MSEO2 pin in added in column 17, 3rd last row.<br>In Table 7. "Port pin summary":<br>• Updated "Function" and "Peripheral" entries for PL[0] and PL[1].<br>• For PB[7], PM[0], PM[8], and PM[12], changed PWMOA to PWMO.<br>• For PB[8], PB[10], and PM[7], changed PWMO to PWMOA.<br>In Section 3.1, "Power-up sequencing", added a note "Vreg bypass mode is for factory testing only".<br>Removed "Pad AC specifications (3.3 V, PAD3V5V = 1)" table and "Pad AC specifications (3.3 V, PAD3V5V = 1)" section.<br>Updated values of $V_{DDR}$ in Table 13. "Recommended operating conditions (5.0 V)" to 4.5-5.5 V.<br>Updated temperature in table note 7 of Table 22. "DC electrical characteristics", from 110 $^0$C to 105 $^0$C.<br>Updated Table 47. "Program and erase specifications" with following modifications:<br>• Added rows for 64KB and 256KB programming timings<br>• Updated timings for 16KB and 128KB programming timings<br>• Removed row for 32KB programming timings<br>Updated Figure 58. "416 TEPBGA Mechanical Drawing (Part 1 of 2)" and Figure 59. "416 TEPBGA Mechanical Drawing (Part 2 of 2)". |
| 13 (13 Apr 2015) | Added a note in Section 2.4.1, "Pad configuration during reset phases".<br>In Table 67. "VIU2 timing parameters", updated the max value of VIU2 pixel clock frequency. Added a table note for this entry.<br>In Section 1.3, "Feature list", updated from "Interrupt Controller (INTC) with 181 peripheral interrupt sources and eight software interrupts" to "Interrupt Controller (INTC) with 163 peripheral interrupt sources and eight software interrupts".<br>In Figure 60. "Commercial product code structure", updated the temperature range for "C" as -40 C to 85 C and for "V" as -40 C to 85/105 C.<br>Updated Table 77. "Orderable part number summary".<br>Following changes were made in Rev 12 of DS but were not captured in Rev 12's revision history:<br>• In Figure 2. "176-pin LQFP pinout", changed "MCK0" to "MCKO" for pin 174 and added "MSEO2" to pin 159<br>• In Table 7. "Port pin summary", added SDA_1 function and I2C1 peripheral for PL[0] port pin and added SCL_1 function and I2C1 peripheral for PL[1] port pin. |
| 14 (4 Aug 2020) | In Table 74. "QuadSPI timing specifications, maximum temperature 125 °C":<br>• Removed the Min and Typ values of Tcq and changed the Max value from 12.1 to 2.7.<br>• Removed the Typ and Max values of Ts.<br>• Removed the Typ and Max value and changed the Min value from -13 to 0 of Th.<br>Added Figure 47. "QuadSPI input timing (SDR mode) diagram".<br>Added a note below Figure 47. "QuadSPI input timing (SDR mode) diagram".<br>Renamed Figure 46. "QuadSPI timing events". |

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