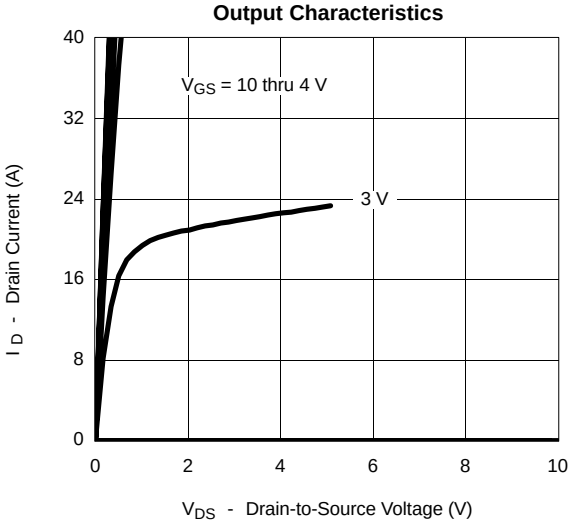
MOSFET SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[NO TAG]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[NO TAG]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 18 A		0.0077	0.0095	Ω
		V_{GS} = 4.5 V, I_D = 15 A		0.0115	0.014	
Forward Transconductance[NO TAG]	g_{fs}	V_{DS} = 15 V, I_D = 18 A		40		S
Diode Forward Voltage[NO TAG]	V_{SD}	I_S = 4.1 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[NO TAG]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 5.0 V, I_D = 18 A		15.5	23	nC
Gate-Source Charge	Q_{gs}			3.8		
Gate-Drain Charge	Q_{gd}			6		
Gate-Resistance	R_g		0.2	0.8	1.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		17	26	ns
Rise Time	t_r			14	21	
Turn-Off Delay Time	$t_{d(off)}$			39	60	
Fall Time	t_f			19	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 4.1 A, di/dt = 100 A/μs		50	80	

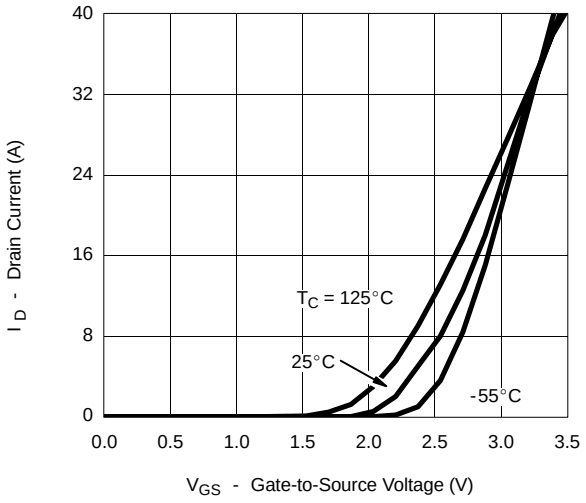
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics



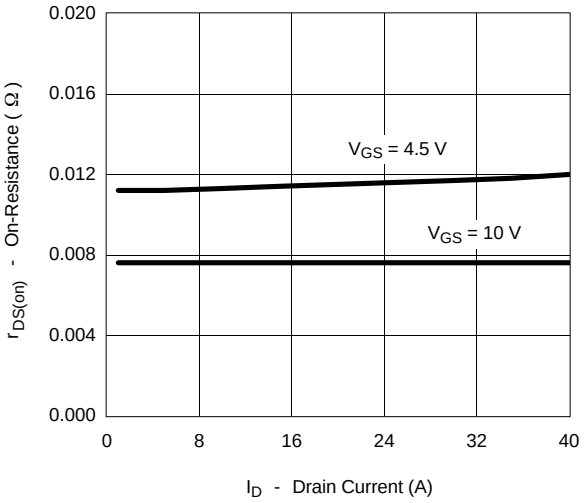
Transfer Characteristics



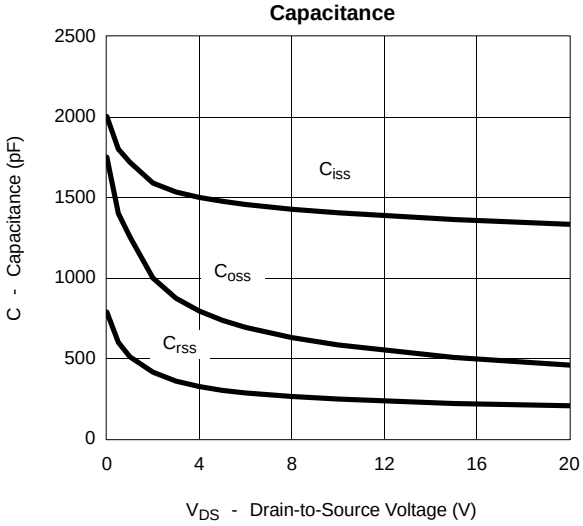
Document Number: 71624
S-31728—Rev. D, 18-Aug-03

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

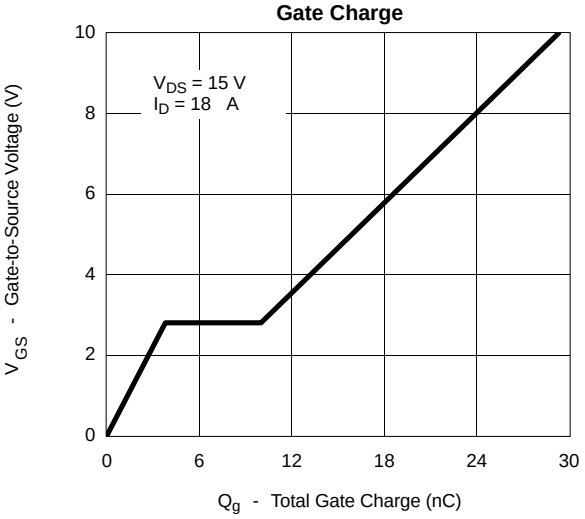
On-Resistance vs. Drain Current



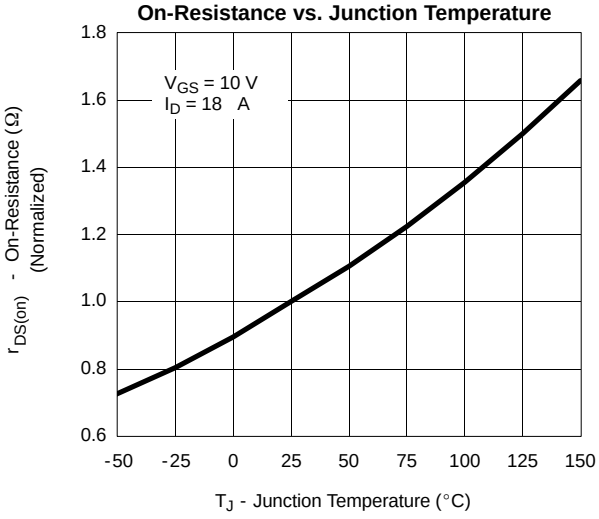
Capacitance



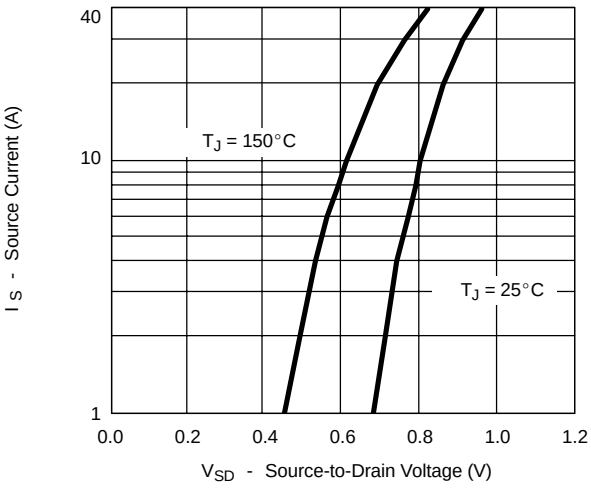
Gate Charge



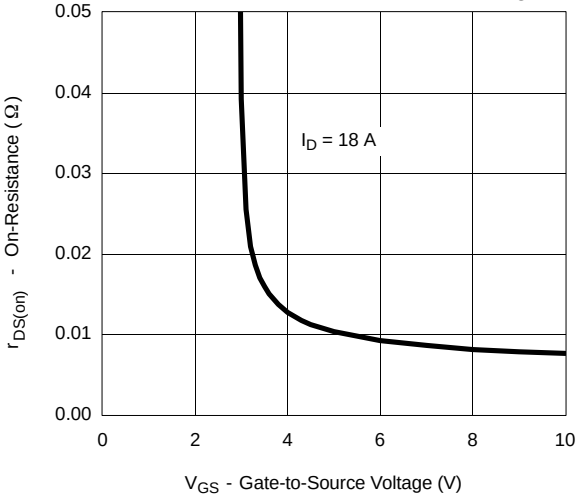
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

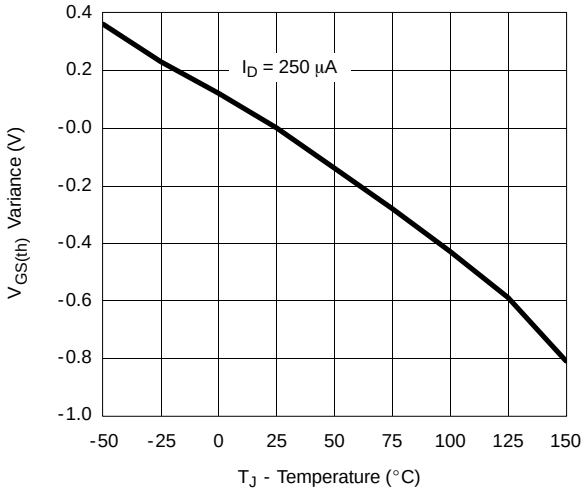


On-Resistance vs. Gate-to-Source Voltage

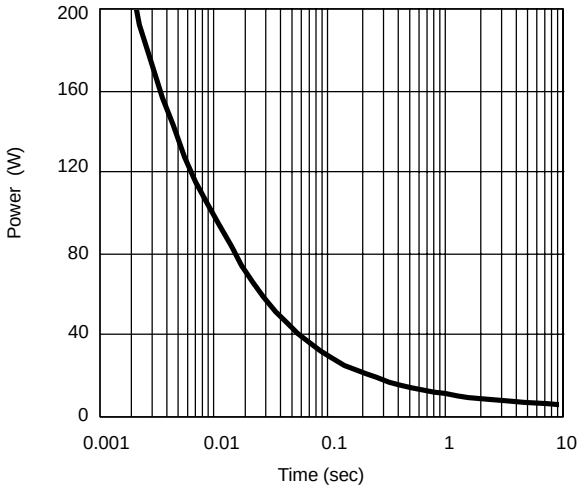


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

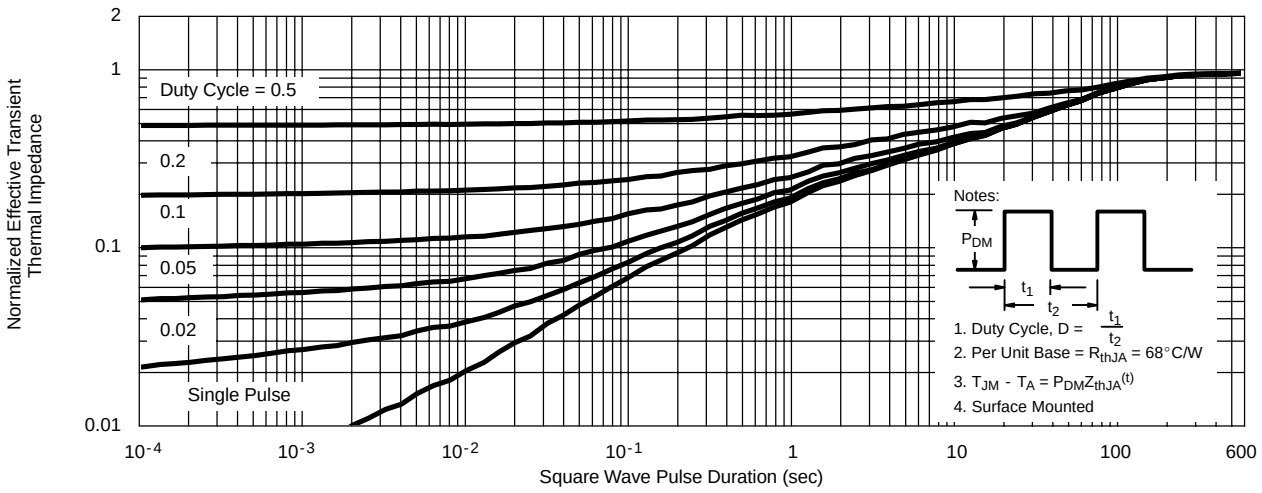
Threshold Voltage



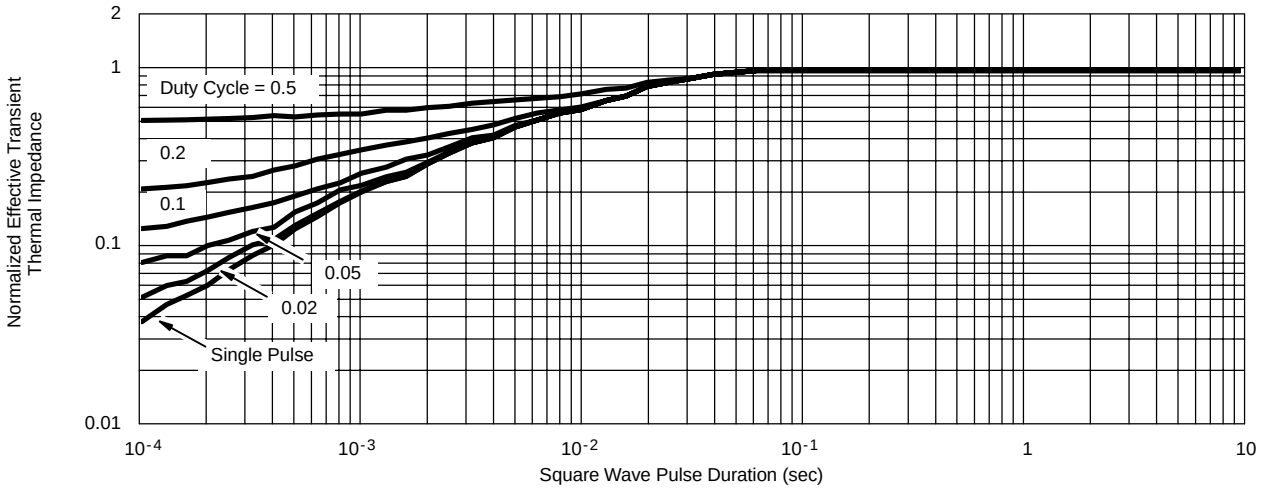
Single Pulse Power, Juncion-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.