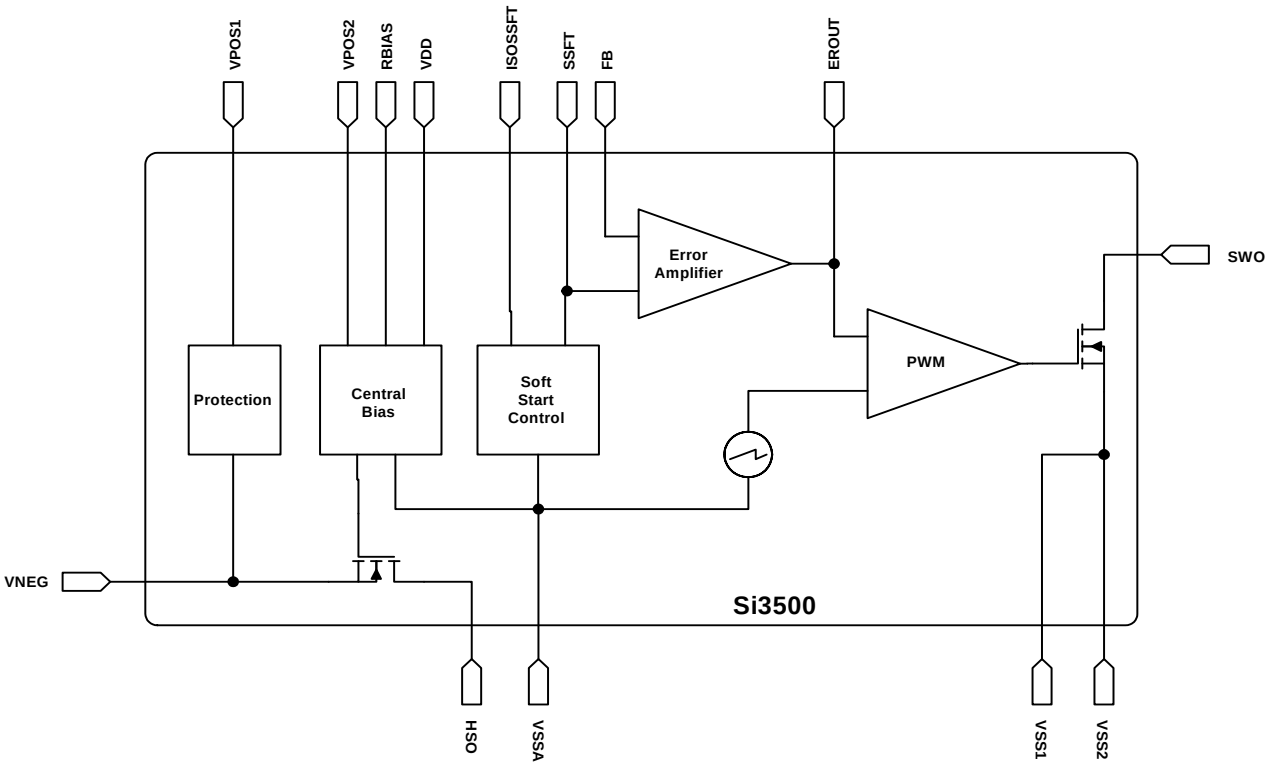
Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Description	Symbol	Min	Typ	Max	Units
VPOS – VNEG input voltage	VIN	42	—	57	V
Ambient Operating Temperature	T_A	–40	25	85	°C

Note: Unless otherwise noted, all voltages referenced to VNEG. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltage and ambient temperature unless otherwise noted.

Table 2. Absolute Maximum Ratings (DC)[1]

Type	Description	Rating	Unit
Voltage	VPOS	–0.3 to 60	V
	HSO	–0.3 to 60	V
	VSS1 or VSS2	–0.3 to 60	V
	SWO[2]	–0.3 to 60	V
Current	VPOS[3]	0 to 400	mA
	VDD	0 to 2	mA
	SWO	0 to 3	A
	VSS1, VSS2, or VSSA	0 to 400	mA
Ambient Temperature	Storage	–65 to 150	°C
	Operating	–40 to 85	°C

Notes:
1. Unless otherwise noted, all voltages referenced to VNEG. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. Averaged over the switching cycle.
3. VPOS is equal to VPOS1 and VPOS2 tied together for test condition purposes.

Table 3. Absolute Maximum Ratings (Transient)[1]

Type	Description	Rating	Unit
Voltage	VPOS[2]	–0.7 to 80	V
	HSO	–0.7 to 80	V
	VSS1, VSS2, or VSSA	–0.7 to 80	V
	SWO	–0.7 to 80	V
Current	VPOS[2]	–5 to 5	A

Notes:
1. Unless otherwise noted, all voltages referenced to VNEG. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. VPOS is equal to VPOS1 and VPOS2 tied together for test condition purposes.

Table 4. Surge Immunity Ratings[1,2]

Type	Description	Rating	Unit
ESD (System-Level)	Air discharge (IEC 61000-4-2)	–16.5 to 16.5	kV
	Contact discharge (IEC 61000-4-2)	–8 to 8	kV
ESD (CDM)	JEDEC (JESD22-C101C)	–750 to 750	V
ESD (HBM)	JEDEC (JESD22-A114E)	–2 to 2	kV
ESD (MM)	JEDEC (JESD22-A115A)	–150 to 150	V

Notes:
1. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. Care should be taken to follow layout guidelines.

Table 5. Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
Current Limit[1]	Inrush	—	140	—	mA
	Operating	400	525	—	mA
Hotswap FET On-Resistance + R_{SENSE}		0.5	—	1.5	Ω
Switcher Frequency		—	350	—	kHz
Maximum Switcher Duty Cycle	ISOSSFT connected to VDD	—	50	—	%
Switching FET On-Resistance		0.3	—	0.86	Ω
Regulated Feedback @ pin FB[2]	DC Avg.	—	1.23	—	V
Regulated Output Voltage Tolerance[2]	Output voltage tolerance @ VOUT	–5	—	5	%
VDD accuracy @ 0.8 mA	42 V ≤ VPOS ≤ 57 V	4.5	—	5.5	V
Softstart charging current	Non-isolated	—	25	—	µA
	Isolated	—	13	—	µA
Thermal Shutdown	Junction temperature	—	160	—	°C
Thermal Shutdown Hysteresis		—	—	25	°C

Notes:
1. At turn-on, before the HSO load capacitor is charged, the current limit is set at the inrush level. After the capacitor has been charged within ~1.25 V of VNEG, the operating current limit is engaged. This higher current limit remains active until the UVLO lower limit has been tripped or until the hotswap switch is sufficiently current-limited to cause a foldback of the HSO voltage.
2. Applies to non-isolated applications only (VOUT on schematic in Figure 1).

Table 6. Total Power Dissipation

Description	Condition	Min	Typ	Max	Units
Power Dissipation	VIN = 50 V, VOUT = 5 V, 2 A	—	0.7	—	W

Table 7. Package Thermal Characteristics

Parameter	Symbol	Test Condition	Typ	Units
Thermal resistance (junction to ambient)	θ_{JA}	Still air; assumes a minimum of nine thermal vias are connected to a 2 in^2 heat spreader plane for the package “pad” node (VNEG).	44	°C/W

2. Typical Application Schematics

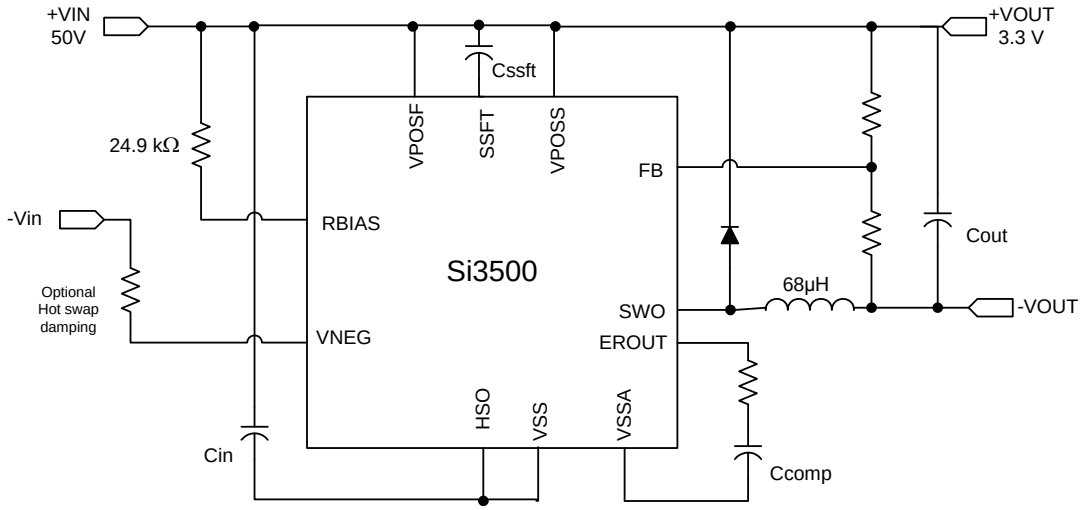

Figure 1. Schematic (Non-Isolated 3.3 V Output)*

***Note:** This is a simplified schematic. Refer to Si3452 reference design databases for complete application schematic.

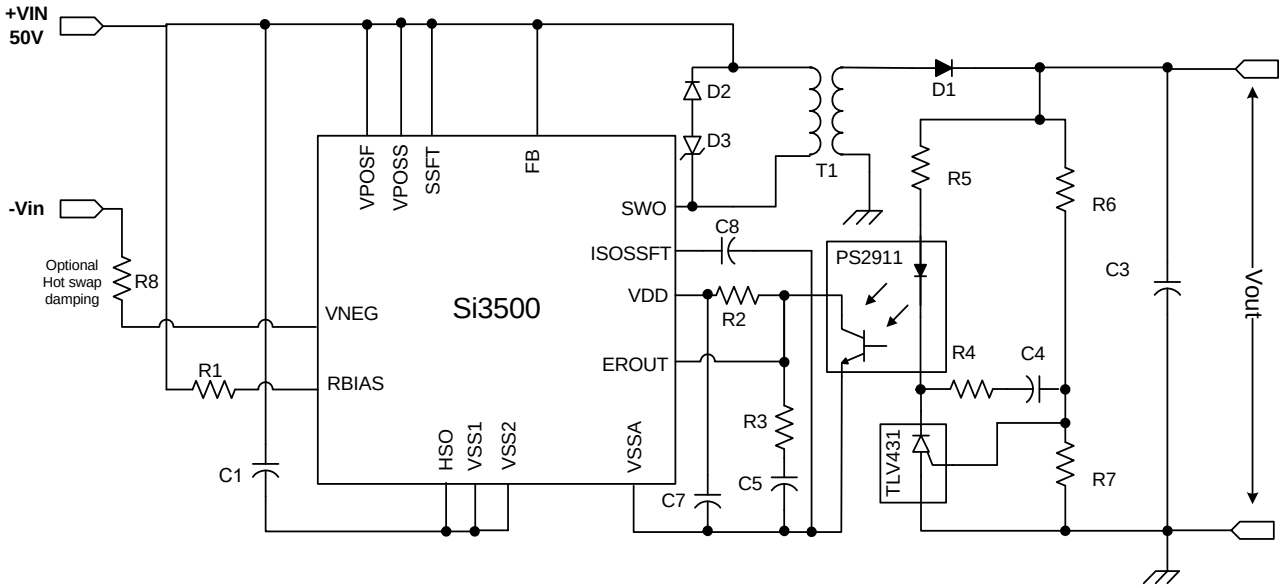

Figure 2. Schematic (Isolated 3.3 V Output)*

***Note:** This is a simplified schematic. Refer to Si3452 reference design databases for complete application schematic.

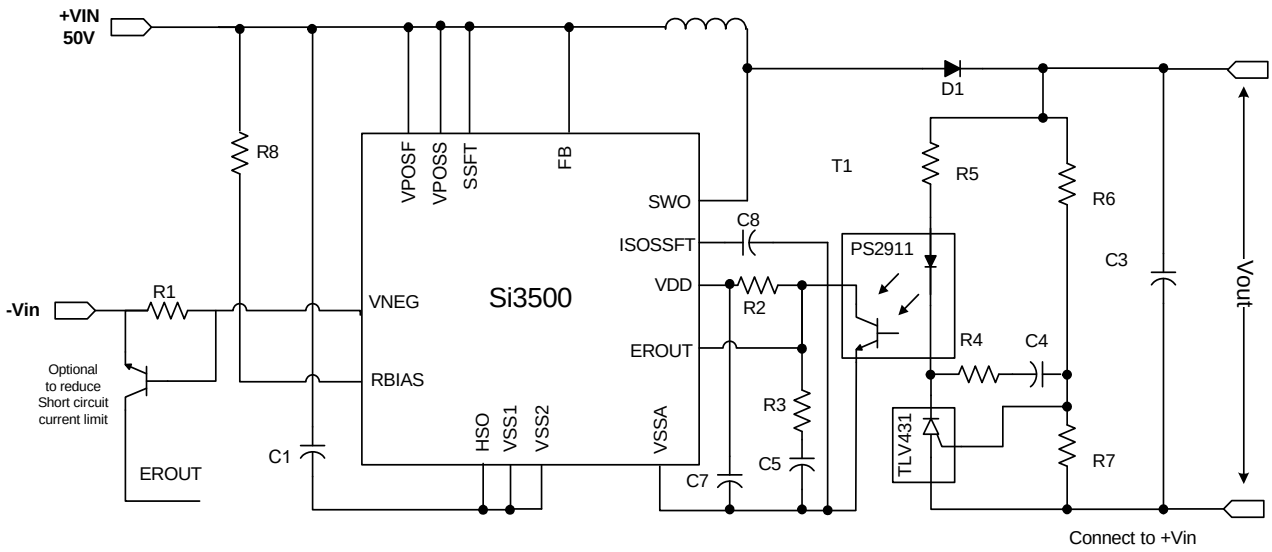

Figure 3. Schematic—Non-Isolated 3.3 V Output*

***Note:** This is a simplified schematic. Refer to Si3452 reference design databases for complete application schematic.

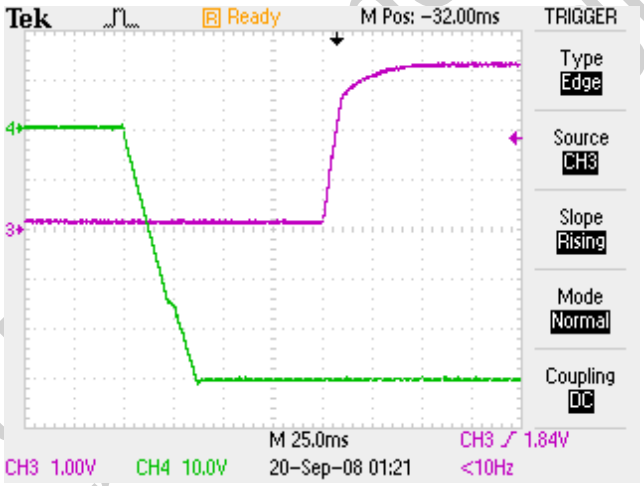

Figure 4. Startup Waveform for Current in Figure 3

3. Functional Description

3.1. Input Surge Protection

The Si3500 has a 65 V Zener diode clamp on the input between VPOS1 and VNEG. The diode is designed to limit the input voltage to less than 80 V for surges of up to 5 A and 50 µsec duration. This provides protection against hot plugging the input power supply.

If the input power supply is hot plugged and there is no surge limiting resistance, there can be an overshoot of input voltage due to lead inductance. For this reason, an optional surge limiting resistor of 2 Ω is recommended. This is particularly true if EMC reduction capacitor is placed directly across VPOS and VNEG.

3.2. Under Voltage Lockout

The Si3500 incorporates an undervoltage lockout (UVLO) circuit to monitor the line voltage and determine when to activate the integrated switching regulator. Before power is applied to the switching regulator, the hotswap switch output (HSO) pin is high-impedance and typically follows VPOS as the input is ramped (due to the discharged switcher supply capacitor). When the input voltage rises above the UVLO turn-on threshold (42 V maximum), the Si3500 turns on the internal hotswap power MOSFET. The switcher supply capacitor begins to charge up under the current limit control of the Si3500, and the HSO pin transitions from VPOS to VNEG. The Si3500 includes hysteresis in UVLO circuits to maintain power to the load until the input voltage falls below the UVLO turn-off threshold. Once the input voltage falls below 30 V (minimum), the internal hotswap MOSFET is turned off.

3.3. Dual Current Limit Hot Swap switch

The Si3500 implements dual current limits. While the hotswap MOSFET is charging the switcher supply capacitor, the Si3500 maintains a lower current limit. The switching regulator is disabled until the voltage across the hotswap MOSFET becomes sufficiently low, indicating the switcher supply capacitor is almost completely charged. When this threshold is reached, the switcher is activated, and the hotswap current limit is increased. This threshold also has hysteresis to prevent systemic oscillation as the switcher begins to draw current and the current limit is increased.

The Si3500 stays in a high-level current limit mode until the input voltage drops below the UVLO turn-off threshold or excessive power is dissipated in the hotswap switch. This dual-level current limit gives low current draw from the input power supply during normal start up with the higher current only occurring during fault conditions.

3.4. Switching Regulator

The Si3500 can be configured to provide output that is either more positive, more negative, or isolated from the positive terminal of the input power supply.

The application determines the converter topology. An isolated application will require a flyback transformer-based switching topology while a non-isolated application can use an inductor-based buck converter topology. In the isolated case, dc isolation is achieved through a transformer in the forward path and a voltage reference plus opto-isolator in the feedback path. The application circuit shown in Figure 2 is an example of such a topology. The non-isolated application in Figure 1 makes use of a single inductor as the energy conversion element, and the feedback signal is directly supplied into the internal error amplifier. The approach shown in Figure 3 is for a non-isolated application where the output is more positive than the input.

3.5. Switcher Startup

The switching regulator is disabled until the hotswap interface has charged the supply capacitor needed to filter the switching regulator's high-current transients. Once the supply capacitor is charged, the hotswap controller engages the internal bias currents and supplies used by the switcher. Additionally, the soft-start current begins to charge the external soft-start capacitor.

The voltage developed across the soft-start capacitor serves as the error amplifier's reference in the non-isolated application. Ramping this voltage slowly allows the switching regulator to bring up the regulated output voltage in a controlled manner. Controlling the initial startup of the regulated voltage restrains power dissipation in the switching FET and prevents overshoot and ringing in the output supply voltage.

In the isolated mode, a capacitor connected between pins ISOSSFT and VSSA slowly ramps the duty cycle clamp in the PWM circuit. Tie the ISOSSFT pin to VDD if not used.

3.6. Switching Regulator Operation

The switching regulator of the Si3500 is a constant-frequency, pulse-width-modulated (PWM) controller integrated with switching power FET optimized for the output power range of up to 10 W.

Once the hotswap interface has ensured proper turn-on of the switching regulator controller, the switcher is fully operational. An internal free-running oscillator and internal precision voltage reference are fed into the pulse-width modulator. The output of the error amplifier (either internal for non-isolated applications or external

for isolated applications) is also routed into the PWM and determines the slicing of the oscillator.

The PWM controls the switching FET drive circuitry. A significant advantage of integrating the switching power FET onto the same monolithic IC as the switching regulator controller is the ability to precisely adjust the drive strength and timing to the FET's sizable gate, resulting in high regulator efficiency. Furthermore, current-limiting circuitry prevents the switching FET from sinking too much current, dissipating too much power, and becoming damaged. Thermal overload protection provides a secondary level of protection.

The flexibility of the Si3500's switching regulator allows the system designer to realize either the isolated or non-isolated application circuitry using a single device. In operation, the integration of the switching FET allows tighter control and more efficient operation than a general-purpose switching regulator coupled with a general-purpose external FET.

4. Layout Guidelines

The following are general PCB layout considerations; reference designs are also available. Due to the unique high-voltage and high-power design considerations, Silicon Labs recommends that the reference designs be followed closely for both BOM and layout. Visit the Silicon Labs Technical Support web page and register to submit a technical support request, particularly if you are not closely following the recommended reference design.

Care must be taken to connect the thermal pad of the Si3500 to an appropriate heat spreader. For full-power applications, a 2 square in plane with at least 9 thermal vias is recommended. This heat spreader must be electrically connected to the negative input power supply.

Care must also be taken in layout to avoid EMI and EMC. Input and output filter capacitors are normally ceramic capacitors for high-frequency performance in parallel with electrolytic capacitors for load transient performance. The ceramic capacitors in particular should be placed so as to minimize radiation for the high-current paths of the switching regulator. The circular area of current flow with the FET on and FET off should be minimized. The direction of current flow with FET on and FET off should maintain a constant clockwise or counterclockwise rotation.

For EMI reduction, a 4 layer design with inner layers connected to the positive input and Vss (for isolated applications) or Vout (for non-isolated applications) is recommended. The high-current paths should not flow through these shield planes. Connection of the dc-to-dc converter high-current paths to the shield plane should be at a single point. Refer to the Si3452 reference design databases for additional layout guideline details.

5. Pin Descriptions

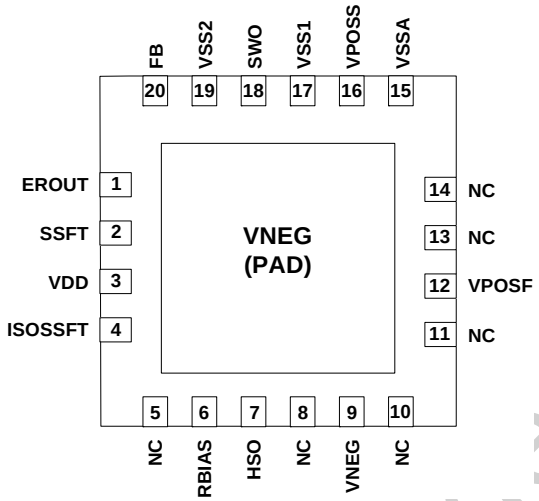

Table 8. Si3500 Pin Descriptions (Top View)

Pin#	Name	Description
1	EROUT	Error-amplifier output and PWM input; directly connected to opto-coupler in isolated or boost applications.
2	SSFT	Soft-start output pin ramps voltage across external soft-start capacitor to allow switcher to ramp output slowly.
3	VDD	5 V supply rail for switcher; provides drive for opto-coupler.
4	ISOSSFT	Isolated mode soft start enable input. Tie to VDD for non-isolated applications. Connect a 0.1 µF capacitor between this pin and VSSA for isolated applications.
5	NC	Do not connect (float).
6	RBIAS	A 25.5 kΩ resistor connected from this to VPOS sets up the bias currents of the Si3500.
7	HSO	Hotswap switch output; connects to VNEG through hotswap switch.
8	NC	Do not connect (float).
9, Pad	VNEG	Rectified high-voltage supply, negative rail. Must be connected to thermal PAD node (VNEG) on package bottom. This thermal pad must be connected to VNEG (pin #9) as well as a 2 in^2 heat spreader plane using a minimum of nine thermal vias.
10	NC	Do not connect (float).
11	NC	Do not connect (float).
12	VPOS1	High-voltage supply, positive rail (force node)
13	NC	Do not connect (float).
14	NC	Do not connect (float).
15	VSSA	Analog ground.

Table 8. Si3500 Pin Descriptions (Top View) (Continued)

16	VPOS2	High-voltage supply, positive rail sense node.
17	VSS1	Negative supply rail for switcher; externally tied to HSO.
18	SWO	Switching transistor output; drain of switching N-FET.
19	VSS2	Negative supply rail for switcher; externally tied to HSO.
20	FB	Regulated feedback input in non-isolated application.

6. Package Outline

Figure 5 illustrates the package details for the Si3500. Table 9 lists the values for the dimensions shown in the illustration.

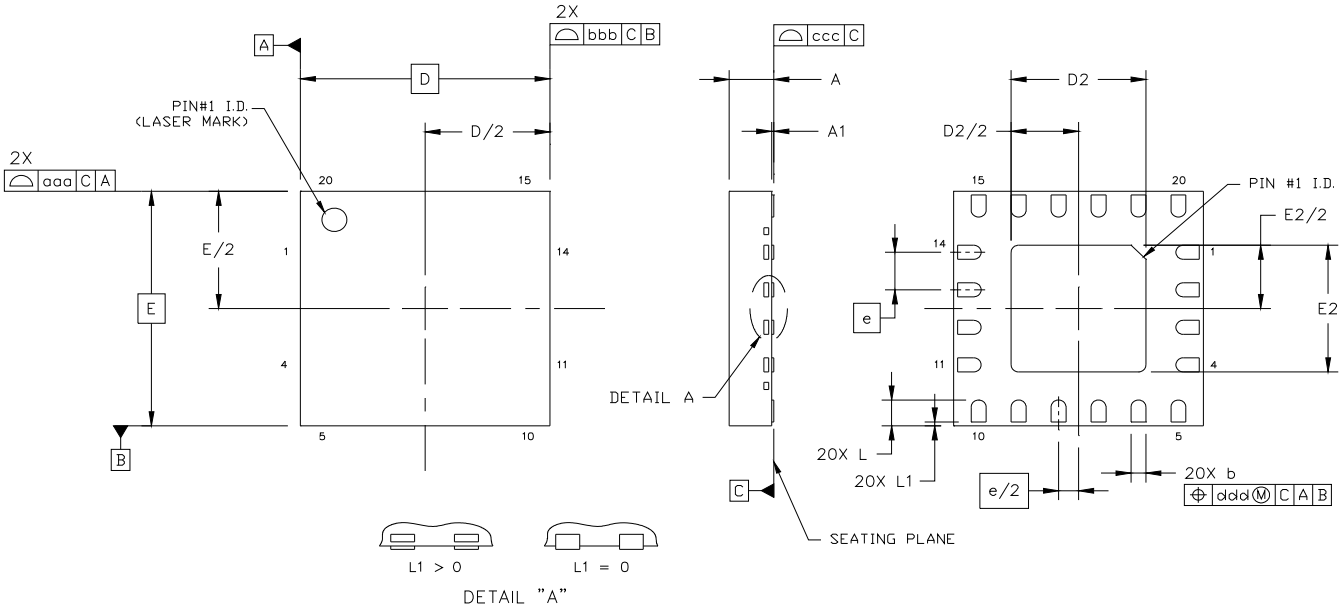

Figure 5. 20-Lead Quad Flat No-Lead Package (QFN)

Table 9. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D		5.00 BSC.	
D2	2.60	2.70	2.80
e		0.80 BSC.	
E		5.00 BSC.	
E2	2.60	2.70	2.80
L	0.50	0.55	0.60
L1	0.00	—	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHHB-1.

7. Recommended PCB Landing Pattern

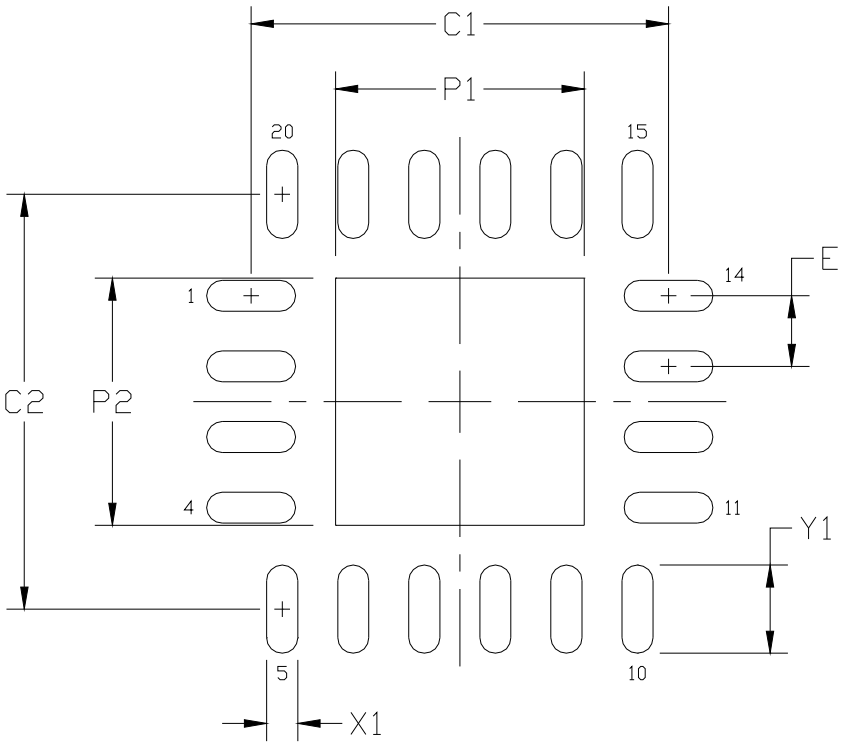

Figure 6. PCB Land Pattern

Table 10. PCB Land Pattern Dimensions

Symbol	Min	Nom	Max
P1	2.70	2.75	2.80
P2	2.70	2.75	2.80
X1	0.25	0.30	0.35
Y1	0.90	0.95	1.00
C1	4.70		
C2	4.70		
E	0.80		

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design:

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 m minimum, all the way around the pad.

Stencil Design:

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
8. A 2x2 array of 1.2 mm square openings on 1.4 mm pitch should be used for the center ground pad.

Card Assembly:

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. Ordering Guide

Part Number*	Package	Temp Range	Recommended Maximum Output Power
Si3500-A-GM	20-pin QFN, RoHS compliant	–40 to 85 °C	≤ 10 W
***Note:** Add an “R” at the end of the part number to denote tape and reel option.			

Document Change List

Revision 0.1 to Revision 1.0

- Updated revision number to 1.0 to reflect production status.
- Updated Table 4 on page 5.

Revision 1.0 to Revision 1.1

- Editorial changes in "4. Layout Guidelines" on page 10.

Revision 1.1 to Revision 1.2

- Added “Not Recommended for New Designs” watermark.

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