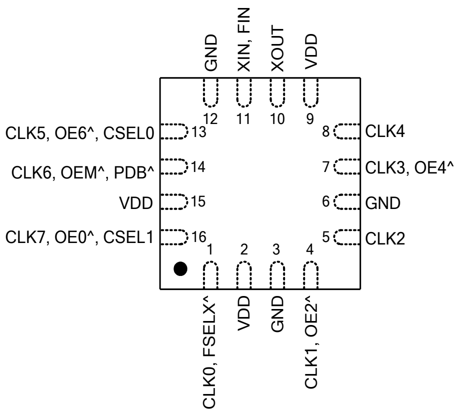
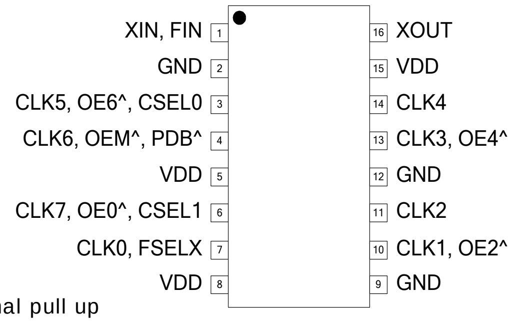
1.8V to 3.3V, PicoPLL, 3-PLL, 200MHz, 8 Output Clock IC

PIN CONFIGURATION



QFN Package

^ Denotes internal pull up



(T)SSOP Package

PACKAGE PIN ASSIGNMENT

Name	Package Pin #		Type	Description
	QFN-16L	(T)SSOP-16L		
CLK0, FSELX	1	7	B*	- Programmable Clock (CLK0) output or - CLK2 Frequency Switching (FSELX) input.
GND	3, 6, 12	2, 9, 12	P	GND connection.
VDD	2, 9, 15	5, 8, 15	P	VDD connection.
CLK1, OE2	4	10	B*	- Programmable Clock (CLK1) output or - Output Enable (OE) input for CLK2.
CLK2	5	11	O	Programmable Clock (CLK2) output.
CLK3, OE4	7	13	B*	- Programmable Clock (CLK3) output or - Output Enable (OE) input for CLK4.
CLK4	8	14	O	Programmable Clock (CLK4) output.
XOUT	10	16	O	Crystal output pin. Do Not Connect when using FIN.
XIN, FIN	11	1	I	Crystal or Reference Clock input.
CLK5, OE6, CSEL0	13	3	B*	- Programmable Clock (CLK5) output or - Output Enable (OE) input for CLK6 or - Configuration Switching input.
CLK6, OEM, PDB	14	4	B*	- Programmable Clock (CLK6) output, or - Output Enable Master (OEM) for all clock outputs, or - Power Down mode (PDB) input.
CLK7, OE0, CSEL1	16	6	B*	- Programmable Clock (CLK7) output or - Output Enable (OE) input for CLK0 or - Configuration Switching input.

* **Note**: All bidirectional buffers (I/Os) incorporate an internal 60KΩ pull up resistor when used as an input except when PDB mode is used. In configurations that use PDB, the PDB pin will have a 10MΩ pull up resistor.

1.8V to 3.3V, PicoPLL, 3-PLL, 200MHz, 8 Output Clock IC

KEY PROGRAMMING PARAMETERS

CLK[0:7] Output Frequency	Output Drive Strength	Programmable Input/Output
CLK[0,3,6] F_{VCOx} / (P*(1,2,4,8)), F_{REF} or F_{REF} / (P*(1,2,4,8)) CLK[1,4,7] F_{VCOx} / P CLK[2,5] F_{VCOx} / P, F_{REF} or F_{REF} / P Where F_{VCOx} = F_{REF} * M / R M = 11 bit R = 8 bit P = 5 bit (Odd/Even Divider)	Each output has three optional drive strengths to choose from. They are: • Low: 4mA • Std: 8mA (default) • High:16mA	Most pins are multi-function I/Os. In addition to CLK, they can be configured to perform as: • OE [0,2,4,6] – (Output Enable for individual I/Os) • OEM – (Master OE controlling all outputs) • CSEL[0:1] – (Device Configuration Switching) • FSELX – (CLK2 Frequency Switching) • PDB – (Power Down) • CLK[0:8] – (Output) • HiZ or Active Low disabled state

FUNCTIONAL DESCRIPTION

The PL613-01 is a highly featured, very flexible, advanced triple PLL design for high performance, low-power applications. The device accepts a low-cost fundamental crystal input of 10MHz to 40MHz or a reference clock input of 10MHz to 200MHz and is capable of producing 8 distinct output frequencies up to 200MHz. All 3-PLLs are fully programmable, with a total of five, 5-bit Post VCO, Odd/Even 'P-counter' dividers with additional 1, 2, 4 or 8 'Post P-counter' dividers to allow generating most demanding frequencies, easily. The outputs can be programmed to deliver the generated frequencies from the PLLs, or the reference input. Each bidirectional feature pin (I/O) on the PL613-01 incorporates a 60KΩ pull up resistor and can be configured to perform various functions. Usage of various design features of these products is mentioned in the following paragraphs.

PLL Programming

The three PLLs in PL613-01 are fully programmable. Each PLL is equipped with an 8-bit input frequency divider (R-Counter) and an 11-bit VCO frequency feedback loop (M-Counter) divider. The three PLL outputs are transferred to five 5-bit post VCO, Odd/Even dividers (P-Counter), as shown in the above diagrams. In addition, there are three optional (÷1, ÷2, ÷4 or ÷8) post P-Counter dividers, that can further divide the VCO frequency. In general, the PLL output frequency is determined by the following formula:

$$F_{OUT} = (F_{REF} * M)/(R * P)$$

For output calculations, please note that 'P' includes the 'P' counter bits plus the additional optional (÷1, ÷2, ÷4 or ÷8) dividers, if used.

CLKx (Clock Outputs)

There are a maximum of 8 outputs available on the PL613-01. Clock output frequencies can be configured as follows:

CLK[0,3,6]
- F_{VCOx} / (P*(1, 2, 4, 8))
- F_{REF} (Crystal or Reference Clock frequency)
- F_{REF} / (P*(1,2,4,8))

CLK[1, 7]
- F_{VCOx} / P

CLK[2, 4, 5]
- F_{VCOx} / P, F_{REF} or F_{REF} / P

Each output can be programmed with a 4mA, 8mA, or 16mA drive strength. The maximum output frequency is 200MHz @ 3.3V, 166MHz @ 2.5V or 110MHz @ 1.8V.

OE (Output Enable)

Four pins can be configured as OE inputs for controlling individual clock outputs, as shown in the table below:

OEx	Controls Output On CLK#
OE0	CLK0
OE2	CLK2
OE4	CLK4
OE6	CLK6

Note: Typical enable time is <500ns plus one clock period.

The OE feature can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode. The programming control for individual OEs is shown below:

OE Pin	OE Type (Programmable)	Osc	PLL	Output
0	0 (Default)	On	On	Hi Z
	1	On	On	Active '0'
1	Normal Operation (Default)			

OEM (Master Output Enable)

One pin can be configured to be a single Master OE (OEM) input pin that controls all the outputs of the PL613-01. In addition the state of the disabled outputs can be programmed to float (Hi Z) or to operate in the 'Active low' mode. The OEM Function operates on the following logic:

OEM Pin	OE Type (Programmable)	Osc	PLL	Output
0	0 (Default)	On	On	Hi Z
	1	On	On	Active '0'
1	Normal Operation (Default)			

Note: Typical enable time is <500ns plus one clock period.

Power-Down Control (PDB)

When activated, PDB 'Disables all the PLLs, the oscillator circuitry, counters, and all other active circuitry. PDB activation disables all outputs and the IC consumes <10μA of power. The PDB input incorporates a 10MΩ pull up resistor for normal operating condition.

The PDB feature can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode. The logic for PDB is shown below:

PDB Pin	PDB Type Program	Osc	PLL	Output
0	0 (Default)	Off	Off	Hi Z
	1	Off	Off	Active '0'
1	Normal Operation (Default)			

Note: Typical enable time from power down is <2ms.

On-The-Fly Configuration Switching (CSEL)

The PL613-01 can be programmed to allow switching between 4 different configurations, allowing for changes in the output frequencies. Many applications (i.e. video/audio) can use the same design footprint, but allow for configuration switching, adhering to various standards. CSEL0 and CSEL1 are used in the switching selection. These pins incorporate a 60kΩ pull up resistor for normal operating condition. The logic for configuration switching of the programmed parts is shown below:

CSEL1	CSEL0	Programmed Configuration
0	0	0
0	1	1
1	0	2
1	1	3 (Default)

Note: Typical enable time is <500μs.

On-The-Fly Output Frequency Switching Between Two Output Frequencies (FSELX)

The PL613-01 is equipped with the FSELX feature to allow frequency switching of two frequencies on one of the output pins. Frequencies assigned to CLK1 and CLK2 can be switched, when FSELX is activated, on CLK2 output. The logic for FSELX is shown below:

FSELX	CLK2 Output
0	Frequency 2
1 (default)	Frequency 1

Note: Typical enable time is <10ns plus one clock period.

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (>1 inch) as "striplines" or "microstrips" with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

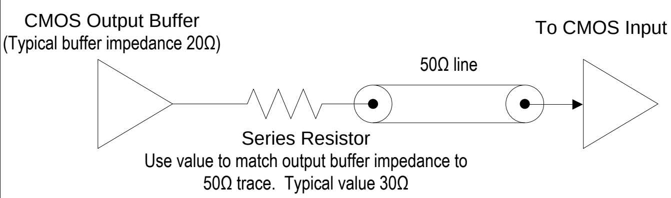
- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply

- Multiple V_{DD} pins should be decoupled separately for best performance.

- Addition of resistors in series with V_{DD} can help prevent noise from other board sources. Traditionally ferrite beads are also used for this purpose but with the PL613-01 the results are better when using resistors.

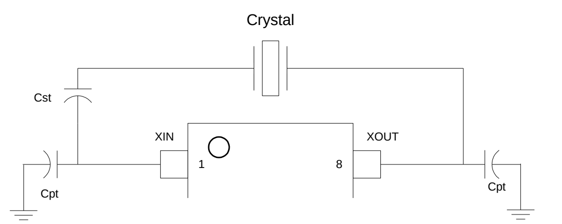
Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



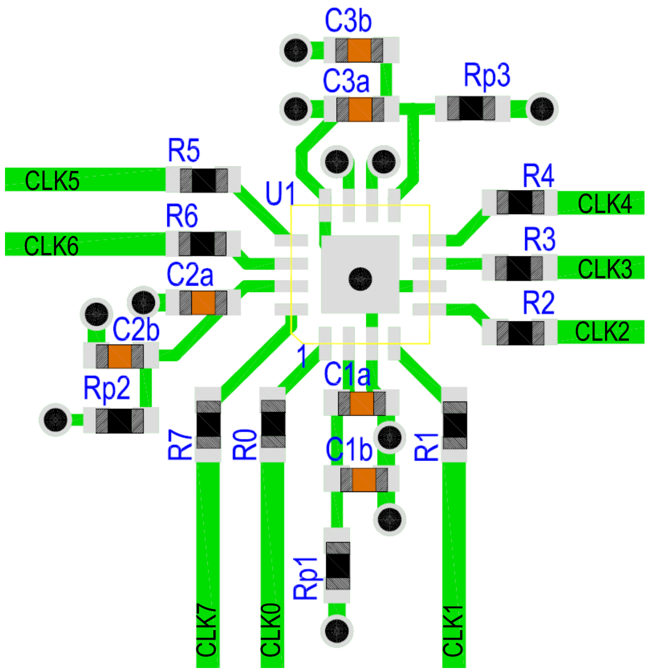
Crystal Tuning Circuit

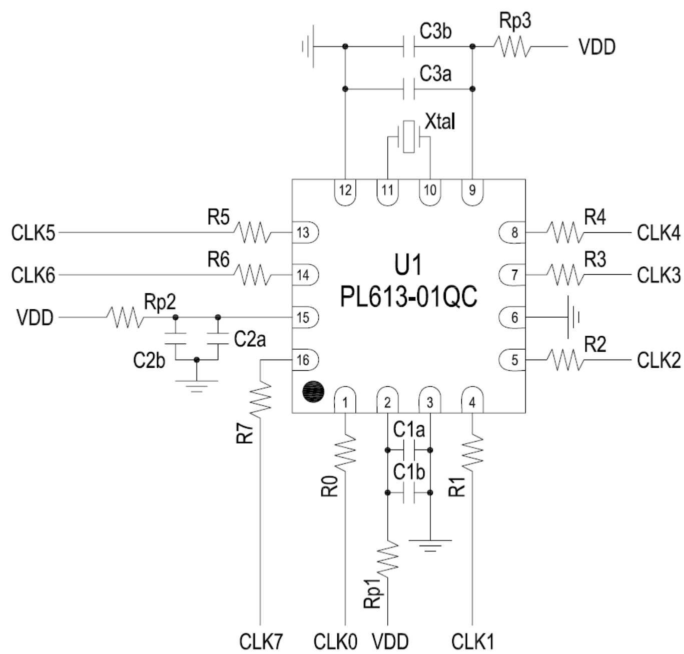
Series and parallel capacitors used to fine tune the crystal load to the circuit load.



CST – Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.
CPT – Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

LAYOUT EXAMPLE





U1 = PL613-01 in QFN-16L. In this example all 8 outputs are used.

C1a, C2a, C3a = 0.1µF and C1b, C2b, C3b = 1µF for Power Supply decoupling. The vias connected to the capacitors go to the ground plane inside the PCB.

R1p, R2p, R3p = 10Ω for Power Supply filtering. The power supply filter is a 1st order low pass filter with -3dB at 30KHz. It is important that the frequencies of the loop bandwidth of the PLLs are filtered properly. The loop bandwidth of the PLLs is in the range 100KHz to 1MHz, depending upon the programmed configuration. The vias connected to Rp1, Rp2 and Rp3 go to the VDD plane inside the PCB.

R0 ~ R7 = 30Ω for matching CLK0 ~ CLK7 outputs to the PCB trace impedance. Place the resistors as close as possible to the IC pins and design the traces to the target clock inputs as transmission lines (microstrip or stripline) for the best signal integrity and the lowest EMI.

When using ferrite beads instead of Rp1, Rp2 or Rp2, make sure the resonance frequency of the bead with the decoupling capacitors is below 50KHz, to not interfere with the PLL loop bandwidth. This requirement is difficult to fulfill so we recommend using the resistors Rp1, Rp2 and Rp3 for power supply filtering.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency (XIN)	Fundamental crystal	10		40	MHz
Input (FIN) Frequency	@ V_{DD} = 3.3V, ±10%	10		200	MHz
	@ V_{DD} = 2.5V, ±10%			166	
	@ V_{DD} = 1.8V, ±10%			110	
Input (FIN) Signal Amplitude	Internally AC coupled	0.8		V_{DD}	Vpp
Output Frequency	@ V_{DD} = 3.3V, ±10% (High Drive)	1		200	MHz
	@ V_{DD} = 2.5V, ±10% (High Drive)			166	
	@ V_{DD} = 1.8V, ±10% (High Drive)			110	
Settling Time	At power-up ($V_{DD} \geq$ 90% of operating V_{DD})			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load. Add one clock period to this measurement for a usable clock output.			500	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
V_{DD} Sensitivity	Frequency vs. V_{DD}, ±10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Duty Cycle	PLL driven output, @ V_{DD} /2, 15pF load, High Drive, over entire frequency range	45	50	55	%
Period Jitter* (10,000 samples)	Configuration dependant, with capacitive decoupling between V_{DD} and GND.		300		ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, V_{DD} = 3.3V	I_{DD}	All 8 outputs @ 20MHz No Load, V_{DD} = 3.3V		17	23	mA
Supply Current, V_{DD} = 2.5V	I_{DD}	All 8 outputs @ 20MHz No Load, V_{DD} = 2.5V		13.5	18	mA
Supply Current, V_{DD} = 1.8V	I_{DD}	All 8 outputs @ 20MHz No Load, V_{DD} = 1.8V		9.5	13	mA
Supply Current	I_{DD}	When PDB=0		10		μA
Operating Voltage	V_{DD}	Configured for 3.3V Operation	2.97	3.3	3.63	V
		Configured for 2.5V Operation	2.25	2.5	2.75	
		Configured for 1.8V Operation	1.62	1.8	1.98	
Output Low Voltage	V_{OL}	I_{OL} = +4mA Std Drive, 3.3V			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Std Drive, 3.3V	2.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V	4			mA
Output Current, Std Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V	16			mA

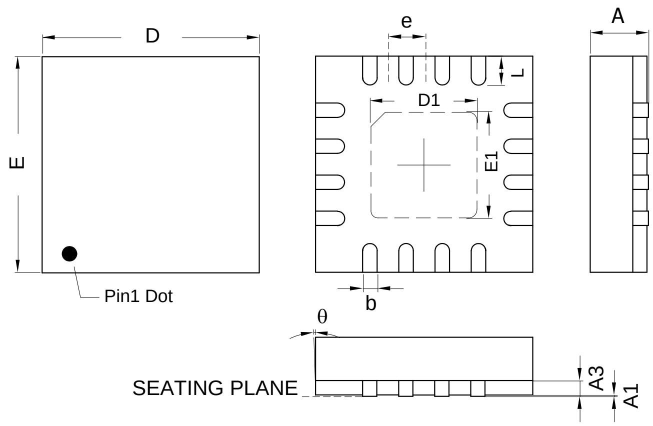
CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN	TYP	MAX	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		40	MHz
Crystal Loading Rating		$C_{L\ (xtal)}$		15		pF
Operating Drive Level				0.1	2	mW
Metal Can Crystal	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			40	Ω
Small SMD Crystal	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			60	Ω

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

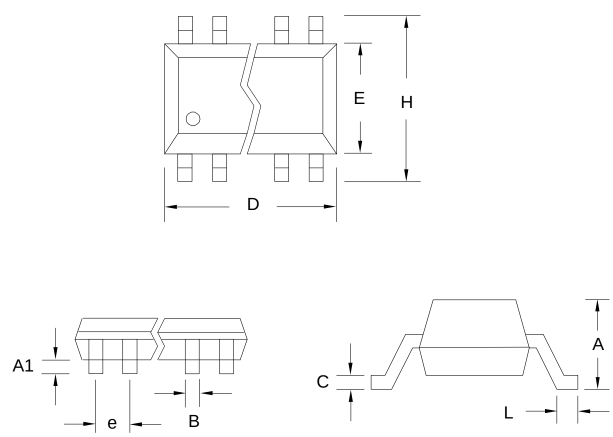
QFN-16L

Symbol	Dimension in MM	
	Min.	Max.
A	0.7	0.8
A1	0.05	0.05
A3	0.20	
b	0.18	0.30
D	3.00 BSC	
E	3.00 BSC	
D1	--	1.70
E1	--	1.70
L	0.30	0.50
e	0.50 BSC	



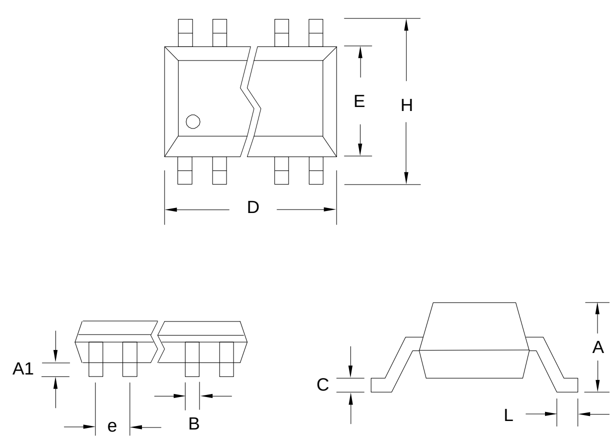
TSSOP-16L

Symbol	Dimension in MM	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
b	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.20	6.60
L	0.45	0.75
e	0.65 BSC	



SSOP-16L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.05	0.15
b	0.20	0.30
C	0.18	0.25
D	4.80	5.00
E	3.80	3.98
H	5.80	6.20
L	0.40	1.27
e	0.635 BSC	



1.8V to 3.3V, PicoPLL, 3-PLL, 200MHz, 8 Output Clock IC

ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL613-01-XXX X X X

PART NUMBER

3 DIGIT ID Code *
(will be assigned at
programming time)

PACKAGE TYPE
O=TSSOP-16L
Q=QFN-16L
X=SSOP-16L

NONE= TUBE
R=TAPE and REEL

TEMPERATURE
C=COMMERCIAL (0°C to 70°C)
I= INDUSTRIAL (-40°C to +85°C)

* Micrel will assign a unique 3-digit ID code for each approved programmed part number.

Part Number/Order Number	Marking†	Package Option
PL613-01-XXXOC	P613-01 XXX(I) LLLLL	16-Pin TSSOP (Tube)
PL613-01-XXXOC-R	P613-01 XXX(I) LLLLL	16-Pin TSSOP (Tape and Reel)
PL613-01-XXXQC-R	P61301 XXX(I) LLL	16-Pin QFN (Tape and Reel)
PL613-01-XXXXC	P613-01 XXX(I) LLLLL	16-Pin SSOP (Tube)
PL613-01-XXXXC-R	P613-01 XXX(I) LLLLL	16-Pin SSOP (Tape and Reel)

† **Marking Notes :**
1) The "I" after the three digit programming code will be marked for Industrial Temperature grade products only. Commercial grade products will not have a character in this position.
2) LLL represents the production lot number