2 Logic Symbol for BGA Package

Page 23, Chapter 1.2, Logic Symbol

Due to the slight difference (number of power supply and ground connections) between the TQFP package and the BGA package, a separate drawing is provided for the BGA.

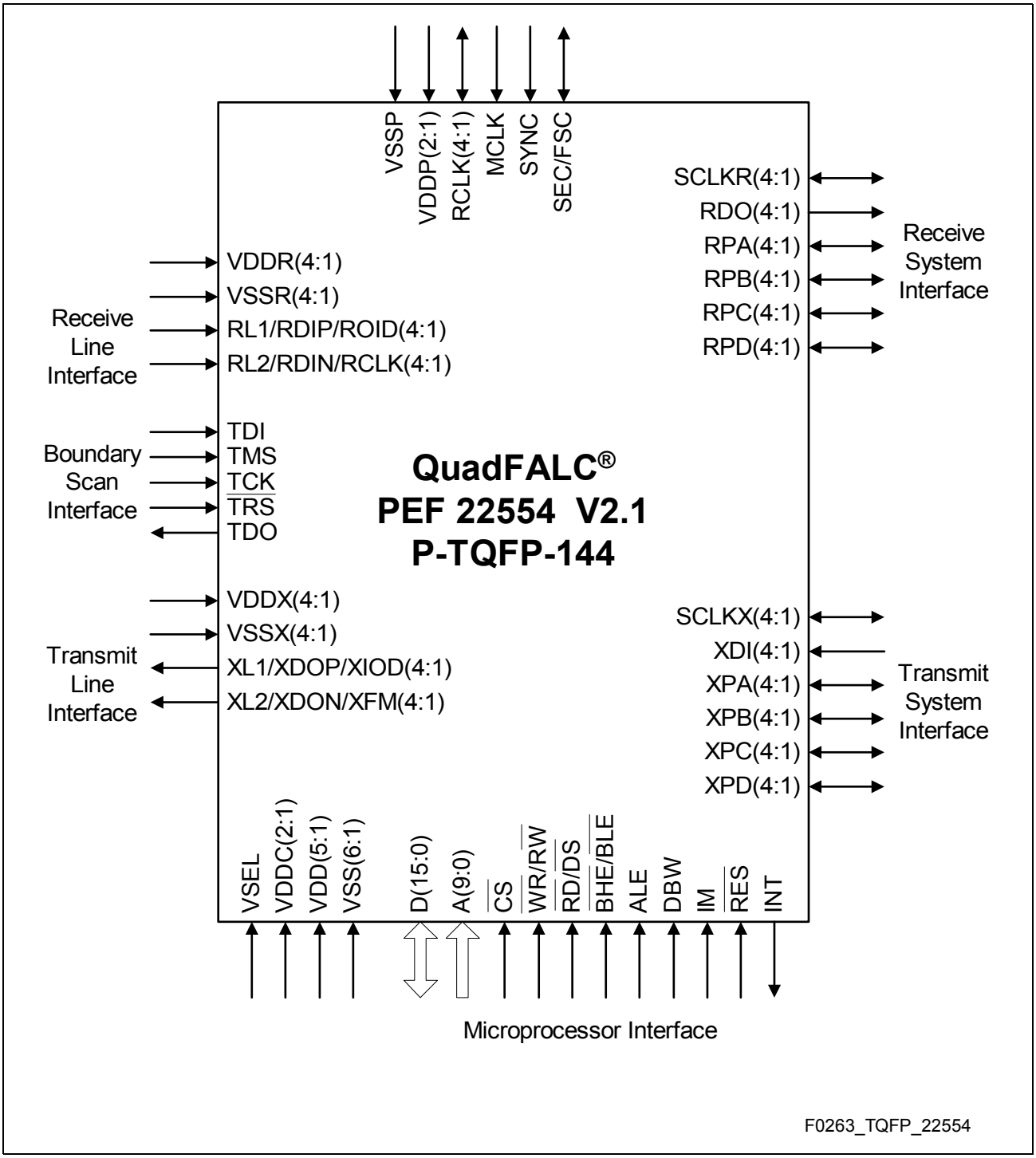

Figure 1 Logic Symbol (TQFP Package)

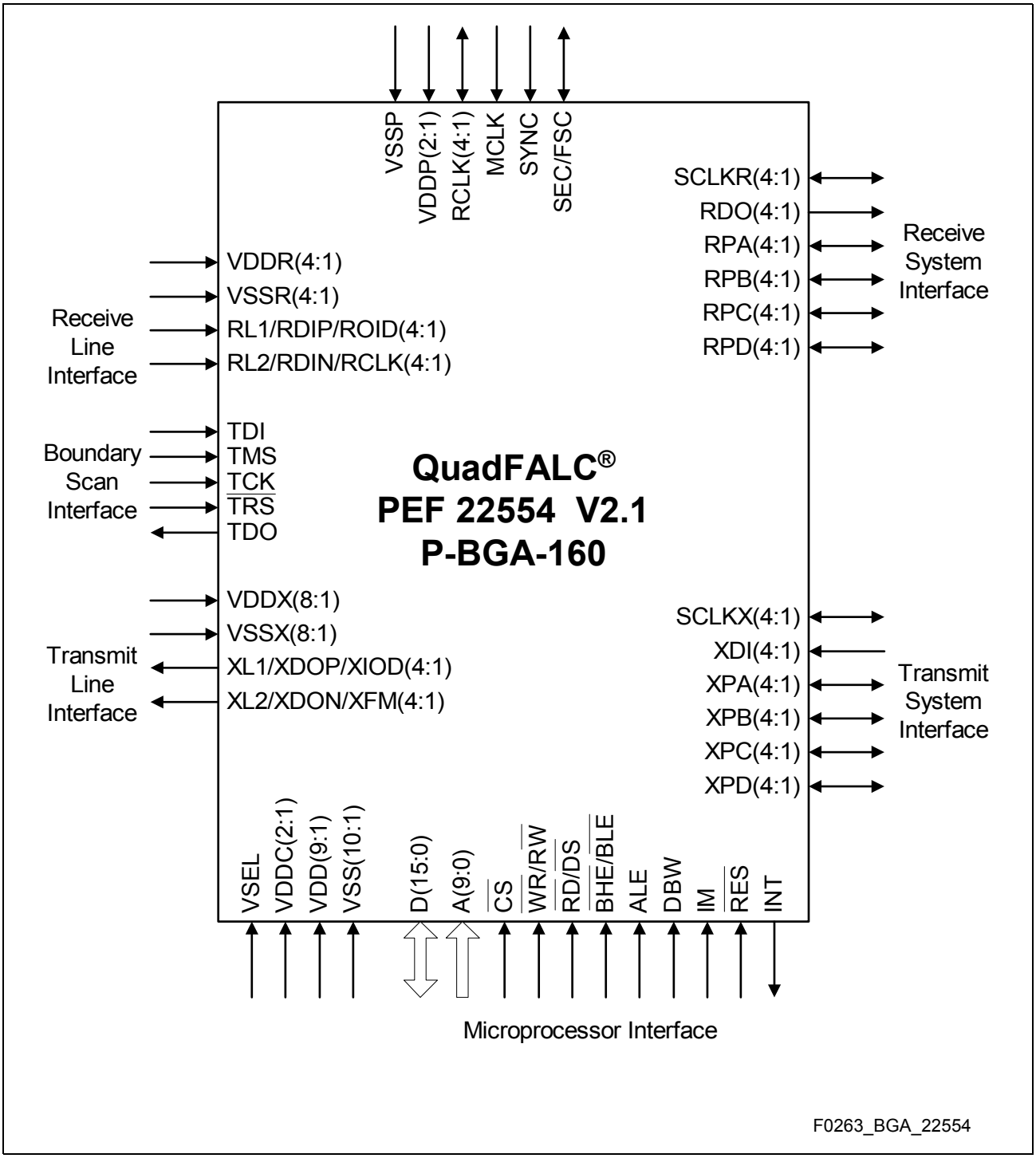

Figure 1A Logic Symbol (BGA Package)

3 JTAG Ball Names

Page 52, Chapter 2.2, Pin Definitions and Functions

The BGA ball numbers are missing for the JTAG pins. They are as shown below.

Table 5 Pin Definitions - Miscellaneous

Pin No.	Ball No.	Symbol	Input Output Supply	Function
Boundary Scan/Joint Test Access Group (JTAG)				
131	B6	$\overline{\text{TRS}}$	I + PU	**Test Reset** for Boundary Scan (active low). If not connected, an internal pullup transistor ensures high input level. If the JTAG boundary scan is not used, this pin must be connected to $\overline{\text{RES}}$ or V_{SS}.
112	D11	TDI	I + PU	**Test Data Input** for Boundary Scan If not connected an internal pullup transistor ensures high input level.
141	D5	TMS	I + PU	**Test Mode Select** for Boundary Scan If not connected an internal pullup transistor ensures high input level.
140	C4	TCK	I + PU	**Test Clock** for Boundary Scan If not connected an internal pullup transistor ensures high input level.
113	C11	TDO	O	**Test Data Output** for Boundary Scan

4 Boundary Scan

4.1 JTAG Instructions

Page 63, Chapter 3.4.2, Boundary Scan Interface

The TAP controller instruction codes 01010101_B and 01010100_B have been added. Both are reserved for device tests and shall not be used.

4.2 JTAG ID

Page 427, Chapter 11.4.2, JTAG Boundary Scan Interface

The correct Boundary Scan IDCODE field is:

0001 0000 0000 1000 1110 0000 1000 0011 (Version = 1_H, Part Number = $008E_H$)

5 RCLK Clock Multiplexing

Page 65/124, Chapter 4.1/5.1, Receive Path in E1 or T1/J1 Mode

Some details have been added to the figure showing the clock multiplexing options for RCLK.

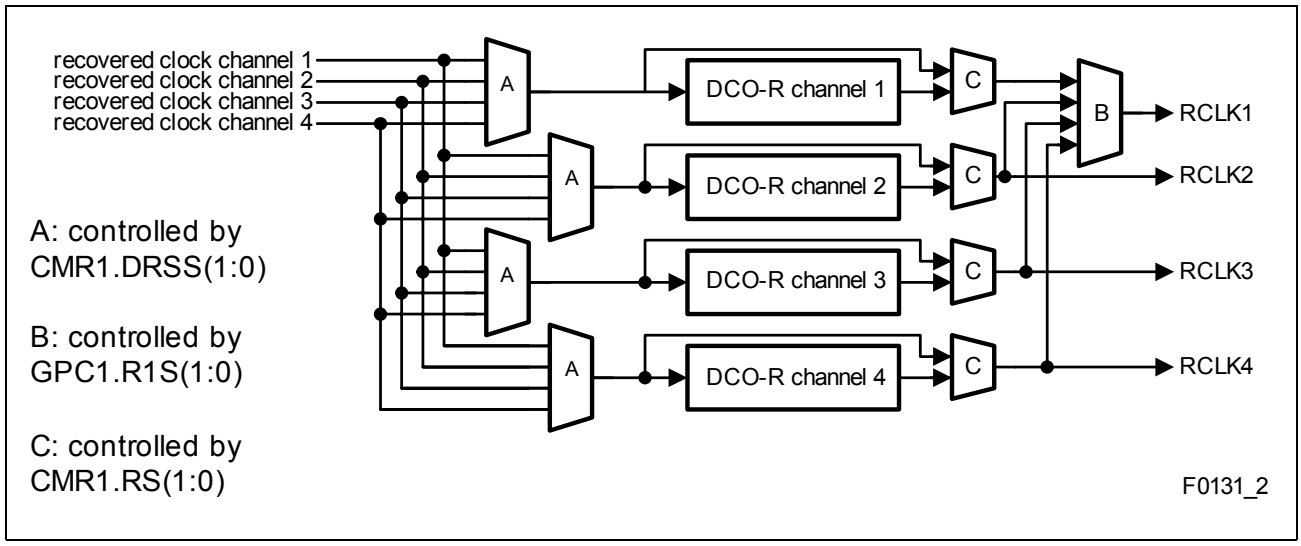

Figure 17/46 Receive Clock Selection (E1/T1/J1)

6 Bipolar Violation Detection

Page 68, Chapter 4.1.6, Receive Line Coding in E1 Mode

The HDB3 line code or the AMI coding is provided for the data received from the ternary or the dual rail interface. All code violations that do not correspond to zero substitution rules are detected, resulting in an increment of the 16-bit code violation counter. If a bit error causes a code violation that leads to a valid substitution pattern, this code violation is neither detected nor counted and the substitution pattern is replaced by the corresponding zero pattern.

In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with HDB3 or AMI postprocessing is provided. If CMI code is selected the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. In case of NRZ coding data is latched with the falling edge of signal RCLKI. The HDB3 code is used along with double violation detection or extended code violation detection (selectable by FMR0.EXZE). In AMI code all code violations are detected. ~~The detected errors increment the code violation counter (16 bits length).~~

Page 127, Chapter 5.1.6, Receive Line Coding in T1/J1 Mode

The B8ZS line code or the AMI (ZCS, zero code suppression) coding is provided for the data received from the ternary or the dual rail interface. All code violations that do not correspond to zero substitution rules are detected, resulting in an increment of the 16-bit code violation counter. If a bit error causes a code violation that leads to a valid substitution pattern, this code violation is neither detected nor counted and the substitution pattern is replaced by the corresponding zero pattern. ~~The detected errors increment the code violation counter (16 bits length).~~

7 Signaling Marker Diagrams

Page 180/181, Chapter 5.5.2, Transmit System Interface

The following diagrams have been modified for clarity.

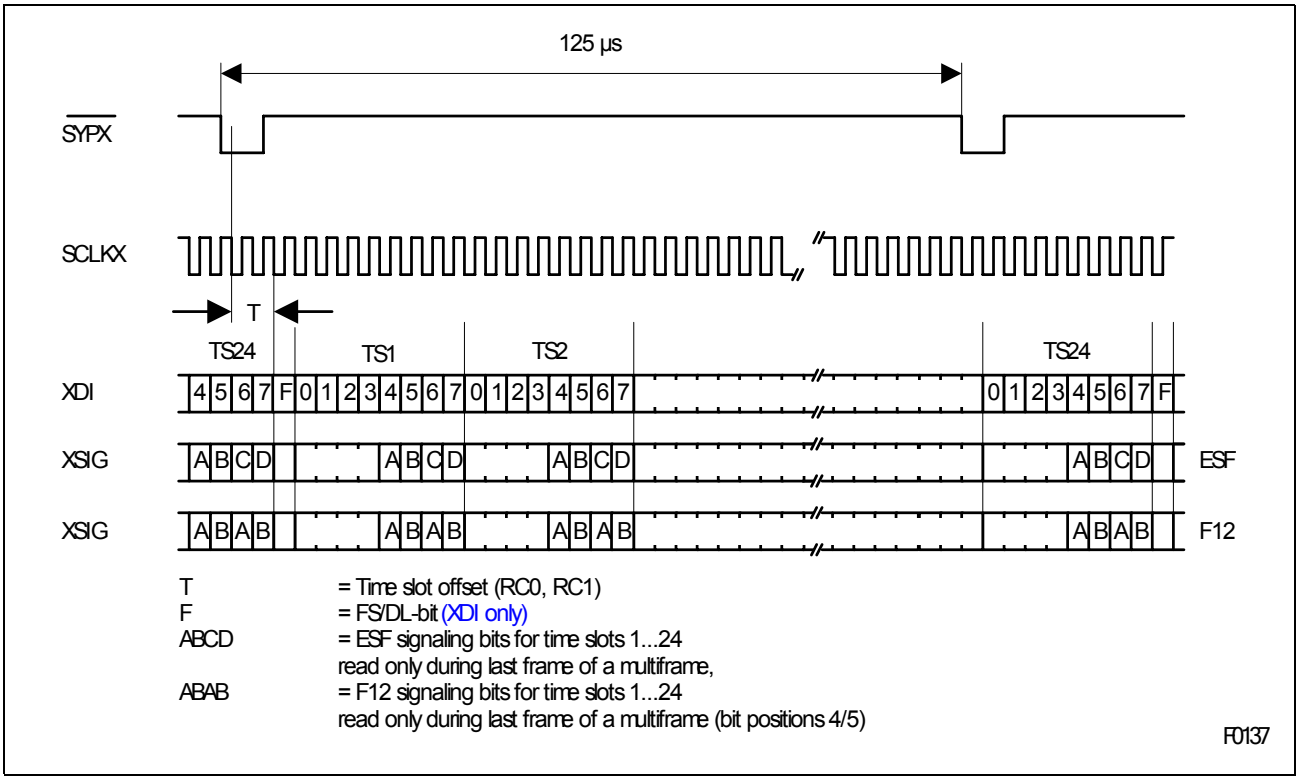

Figure 71 1.544 MHz Transmit Signaling Highway (T1/J1)

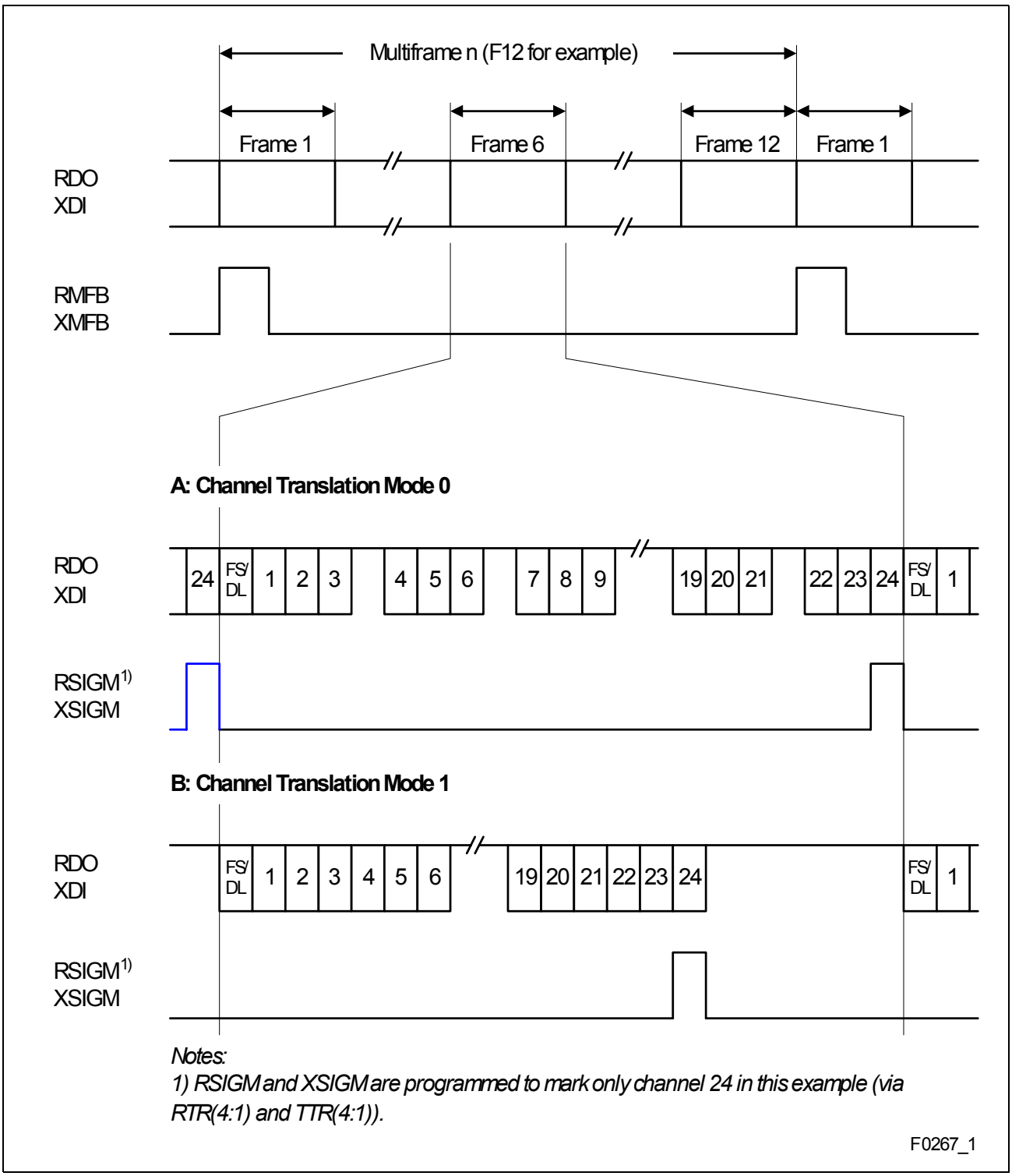

Figure 72 Signaling Marker for CAS/CAS-CC Applications (T1/J1)

8 Clock Mode Selection

Page 194/200, Chapter 6.3 and Chapter 7.3, Device Initialization E1 and T1/J1

The following text has been added:

The clock mode must be programmed according to the selected MCLK frequency *before* any XL1/2 output is enabled (while the outputs are not yet activated by selection of the line coding). Otherwise the output pulse width might not match the pulse mask requirements.

Page 277, Chapter 9.2 and Page 384, Chapter 10.2, Clock Mode Register programming for E1 and T1/J1

The following text has been added/corrected (for E1 and T1/J1 operation):

Attention: Write operations to GCM5 and/or GCM6 register initiate a PLL reset (see below) and must be performed before any port configuration is done. If this is not possible set LIM~~0~~1.DRS (if not set) of every channel separately before writing to these registers and reset LIM~~0~~1.DRS (if it was not set before) after these write operations.

9 Device Initialization

Page 192, Table 46, Initial Values after Reset (E1)

The second row shall read:

2.048 ~~8.192~~ MHz system clocking rate...

Page 194, Table 47, Initialization Parameters (E1)

The row “Framing additions” shall read:

RC0~~RC1~~.ASY4, RC0~~RC1~~.SWD

10 HDLC Handling

Page 221/321, Chapter 9.2/10.2, Register bit CMDR.RMC

Confirmation from CPU to QuadFALC that the current frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released. While the FIFO is empty, RMC *must not* be set. If RMC is given while RFIFO is already cleared, the next incoming data block is cleared instantly, although interrupts are generated. This might lead to incorrect software behaviour.

11 Port RMFB Configuration

Page 269/375, Chapter 9.2/10.2, Register Description, PC(4:1)

The following text has been added:

RMFB is only valid, if the receive buffer is not bypassed.

12 Port RSIG Configuration

Page 270/376, Chapter 9.2/10.2, Register Description, PC(4:1)

The following text has been added:

RSIG is only valid, if the receive buffer is not bypassed.

13 Port XMFS Configuration

Page 270/376, Chapter 9.2/10.2, Register Description, PC(4:1)

The following text has been added:

The activity level of port XMFS can be selected to be active high or active low by programming PC5.CXMFS. This bit *must not* be set, if XMFS is not enabled as an input. XMFS input selection is done by programming one of the Transmit Multifunction Ports, using registers PC4(4:1).XPC(3:0).

Note: XMFS must not be used together with SYPX on different Multifunction Ports.

14 Port $\overline{\text{RFSP}}$ Configuration

Page 376, Chapter 10.2, Register Description, PC(4:1) in T1/J1 mode

The description of register bit PC(4:1).RPC(2:0) = 111 in T1/J1 mode shall read as:

“This marker is active low for ~~488~~ 648 ns with a frequency of 8 kHz.”

15 Absolute Maximum Ratings

Page 420, Chapter 11.1, Absolute Maximum Ratings

The allowed voltage range has been increased. The following values and the text below the table have changed:

Parameter	Symbol	Limit Values	Unit
IC supply voltage (pads, digital)	V_{DD}	– ~~0.3~~ 0.5 to ~~3.6~~ 4.5	V
IC supply voltage (core, digital)	V_{DDC}	– 0.3 to 2.4	V
IC supply voltage PLL (analog)	V_{DDP}	– ~~0.3~~ 0.5 to ~~3.6~~ 4.5	V
IC supply voltage receive (analog)	V_{DDR}	– ~~0.3~~ 0.5 to ~~3.6~~ 4.5	V
IC supply voltage transmit (analog)	V_{DDX}	– ~~0.3~~ 0.5 to ~~3.6~~ 4.5	V
Voltage on any pin with respect to ground[1)]	V_{PAD}	– ~~0.3~~ 0.5 to ~~3.6~~ 4.5	V
Voltage on RL1/RL2 with respect to ground	$V_{RL1/RL2}$	– 0.8 to 4.5	V

1) except V_{DDC} and $V_{RL1/RL2}$

Attention: ***Absolute Maximum Ratings are stress ratings only, and functional operation and reliability under conditions beyond those defined in the normal operating conditions is not guaranteed. Stresses above the maximum ratings are likely to cause permanent damage to the device while extended exposure to conditions outside the operating range may have an impact on component life time.***

16 DC Characteristics

Page 422/423, Chapter 11.3, DC Characteristics

The transmitter output maximum leakage value and receiver maximum input voltage have been changed.

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Transmitter leakage current	I_{TL}		~~15.0~~ 30.0	µA	XL1/2 = V_{DDX}; XPM2.XLT = 1
			~~15.0~~ 30.0	µA	XL1/2 = V_{SSX}; XPM2.XLT = 1
Receiver peak voltage of a mark (at RL1 or RL2)	V_{R12}	-0.45 -0.75[1)]	3.8 4.1[1)]	V	RL1, RL2; RZ signals only[2)]
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_R		~~V_{DDR} +0.3~~ 4.00 4.63[1)]	V	RL1, RL2; RZ signals only[2)]

1) Limit values must only be applied during T1 pulse over-/undershoot according to ANSI T1.403-1999.

2) RZ = return to zero

17 System Interface Marker Timing (Receive)

Page 437, Chapter 11.4.6, AC Characteristics, System Interface

The timing figure has been modified for clarity. The timing values have been corrected.

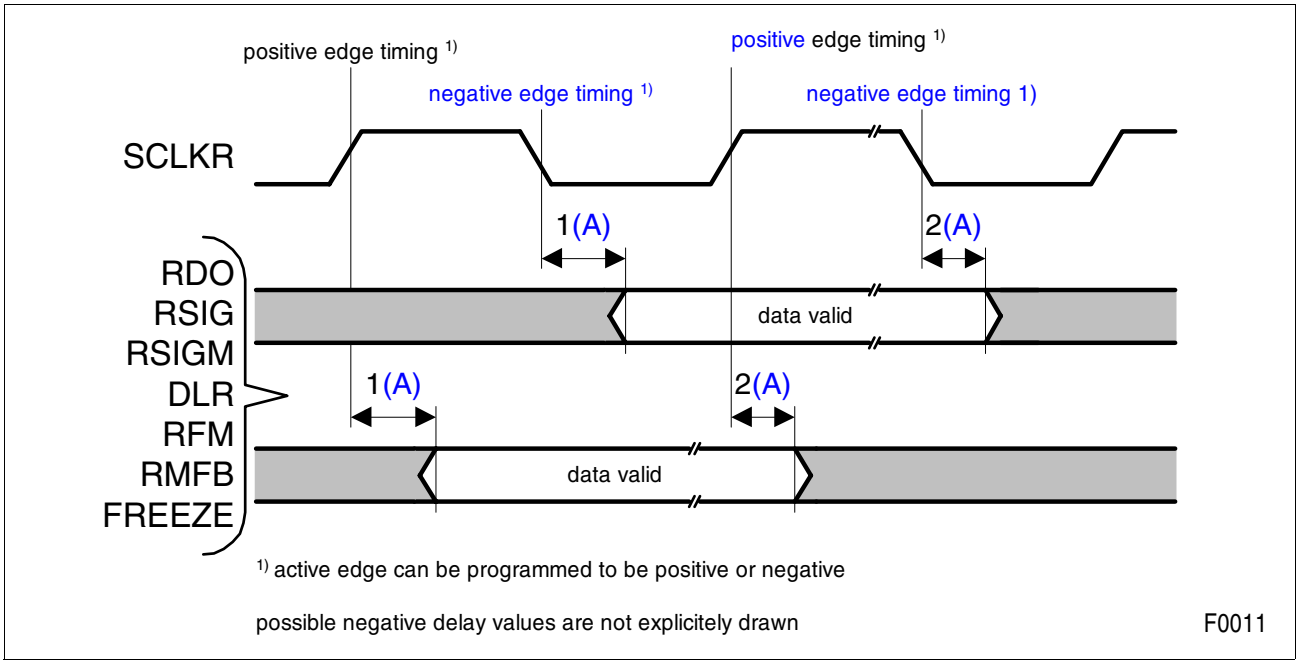

Figure 99 System Interface Marker Timing (Receive)

Table 79 System Interface Marker Timing Parameter Values

No.	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
SCLKR Input Mode					
1	RDO delay	0		35	ns
2	RSIGM, RMFB, DLR, RFM[1)], FREEZE, RSIG marker delay	0		45	ns
SCLKR Output Mode					
1A	RDO delay	~~-55~~ 0	9	~~-20~~ 20	ns
2A	RSIGM, RMFB, DLR, RFM[1)], FREEZE, RSIG marker delay	~~-55~~ 0	9	~~-20~~ 20	ns

SCLKR can be input or output.

1) Timing for RMF is valid only for active high polarity selection.

18 $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Timing

Page 438/439, Chapter 11.4.6, AC Characteristics, System Interface

The output timing has been corrected as shown in the table below.

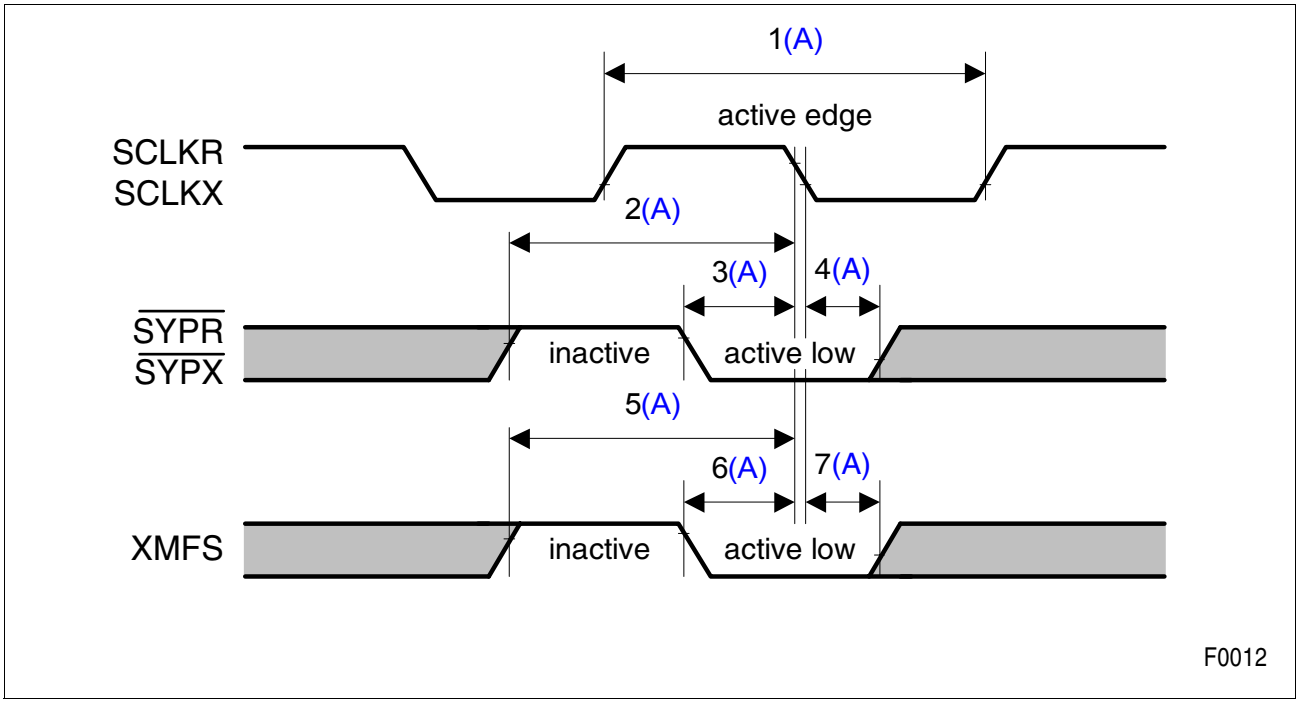

Figure 100 $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Marker Timing

Table 80 $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Timing Parameter Values

No.	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
SCLKR Input Mode					
1	SCLKR period (t_1)	61		648	ns
2	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ inactive setup time	1 x t_1			ns
3	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ setup time	5			ns
4	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ hold time	15			ns
5	XMFS inactive setup time	1 x t_1			ns
6	XMFS setup time	5			ns
7	XMFS hold time	15			ns
SCLKR Output Mode					
1A	SCLKR period (t_1)	61		648	ns
2A	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ inactive setup time	1 x t_1			ns

Table 80 $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Timing Parameter Values (cont'd)

No.	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
SCLKR Output Mode					
3A	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ setup time	~~10~~ 0			ns
4A	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ hold time	~~0~~ 10			ns
5A	XMFS inactive setup time	1 x t_1			ns
6A	XMFS setup time	~~10~~ 0			ns
7A	XMFS hold time	~~0~~ 10			ns

19 Marker Output Timing Parameters

Page 440, Chapter 11.4.6, AC Characteristics, System Interface

The output timing has been corrected as shown in the table below.

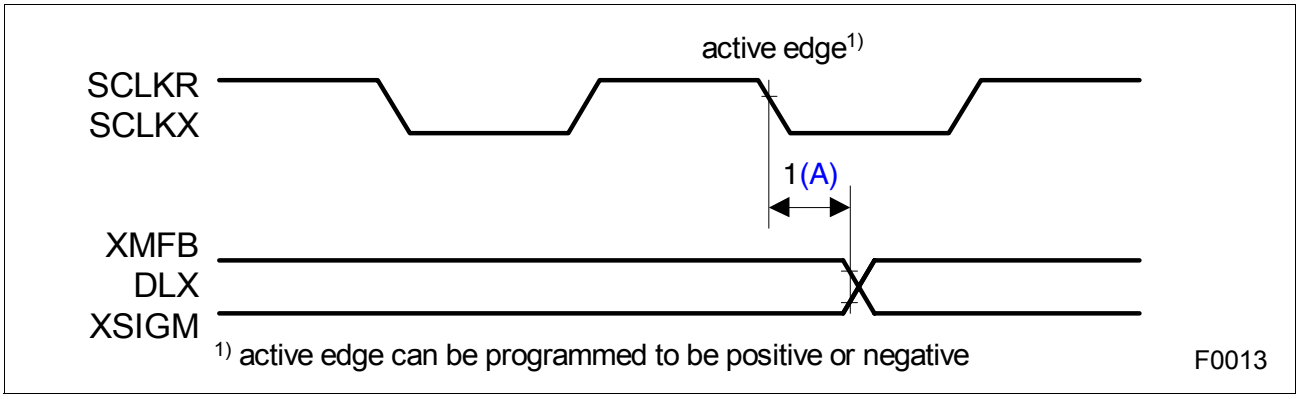

Figure 101 System Interface Marker Timing

Table 81 System Interface Marker Timing Parameter Values

No.	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
SCLKR Input Mode					
1	XMFB, DLX, XSIGM delay			100	ns
SCLKR Output Mode					
1A	XMFB, DLX, XSIGM delay	0	9	~~-20~~ 20	ns

20 XDI/XSIG Timing Parameters

Page 441, Chapter 11.4.6, AC Characteristics, System Interface

The timing has been corrected as shown in the table below.

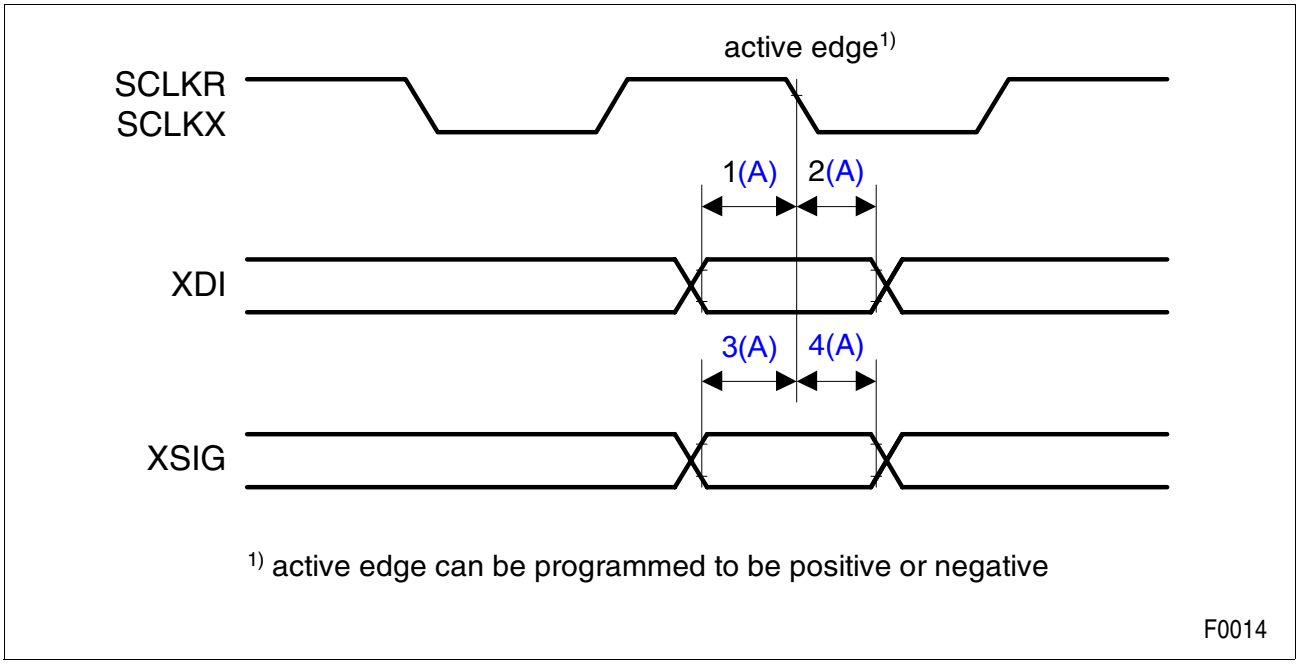

Figure 101 XDI/XSIG Marker Timing

Table 81 XDI/XSIG Timing Parameter Values

No.	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
SCLKR Input Mode					
1	XDI setup time	5			ns
2	XDI hold time	15			ns
3	XSIG setup time	5			ns
4	XSIG hold time	15			ns
SCLKR Output Mode					
1A	XDI setup time	~~10~~ 0			ns
2A	XDI hold time	~~20~~ 10			ns

Table 81 XDI/XSIG Timing Parameter Values (cont'd)

No.	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
3A	XSIG setup time	~~10~~ 0			ns
4A	XSIG hold time	~~20~~ 10			ns

21 SYNC Input Timing Parameters

Page 446, Chapter 11.4.6, AC Characteristics, System Interface

The input timing has been relaxed as shown in the table below.

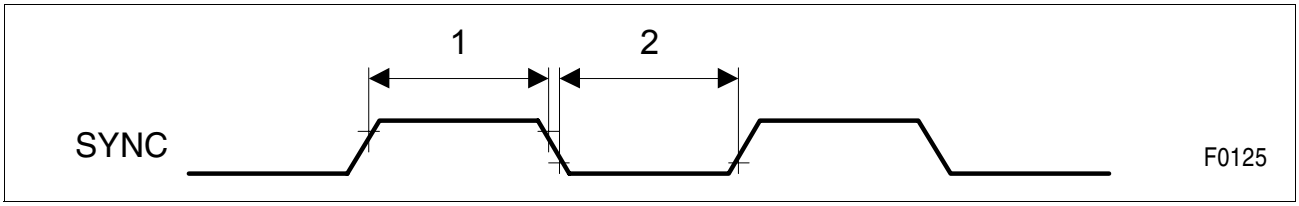

Figure 107 SYNC Timing

Table 87 SYNC Timing Parameter Values

No.	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
1	SYNC high time	~~30~~ 122			~~%~~ ns
2	SYNC low time	~~30~~ 122			~~%~~ ns

22 Typographical Errata

Page 57, Table 7: "BHE" should read "*$\overline{BHE}$*"

Page 57, Table 8: "BLE" should read "*$\overline{BLE}$*"

Page 256/361, FLLB = 1:

The line loopback code is transmitted in ~~un~~framed mode. LLB code does not overwrite the FS/DL-bits.