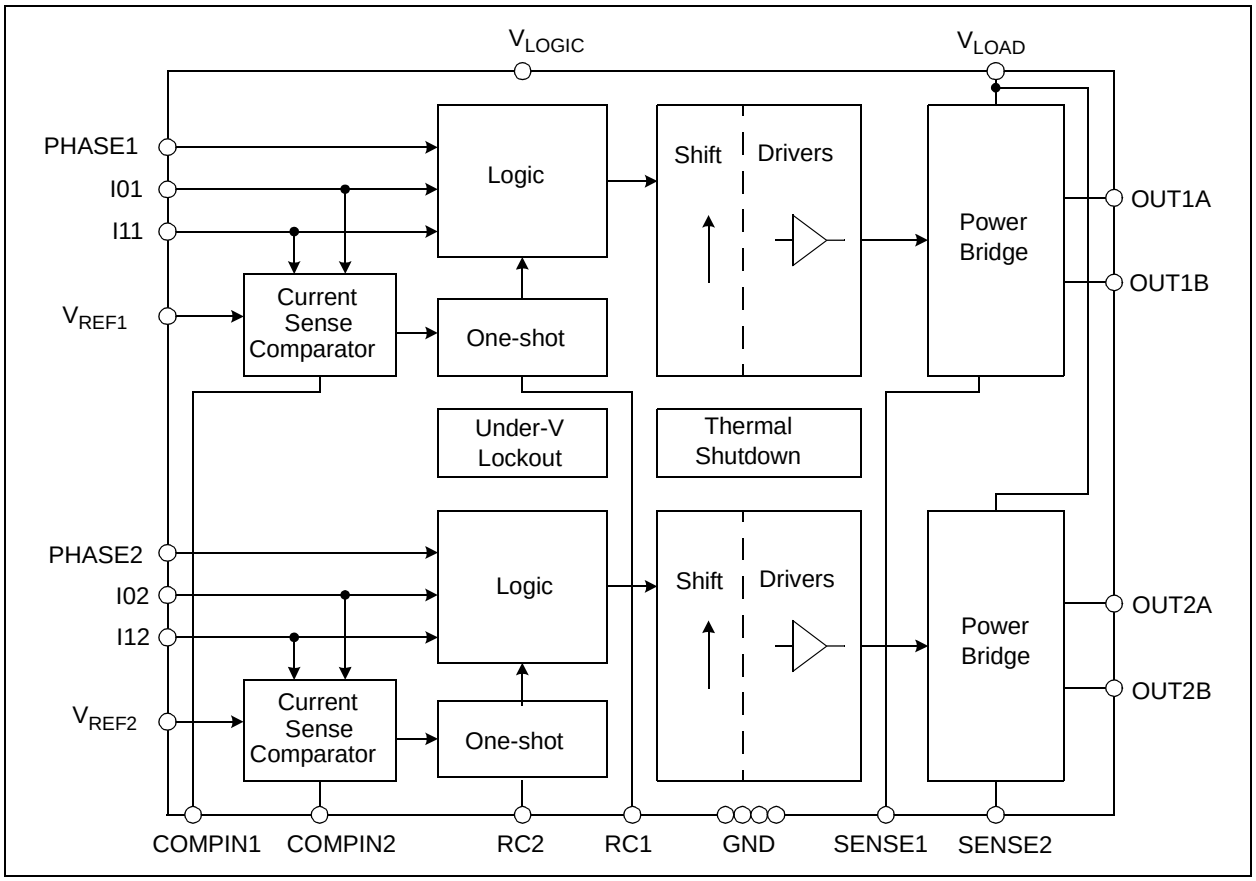
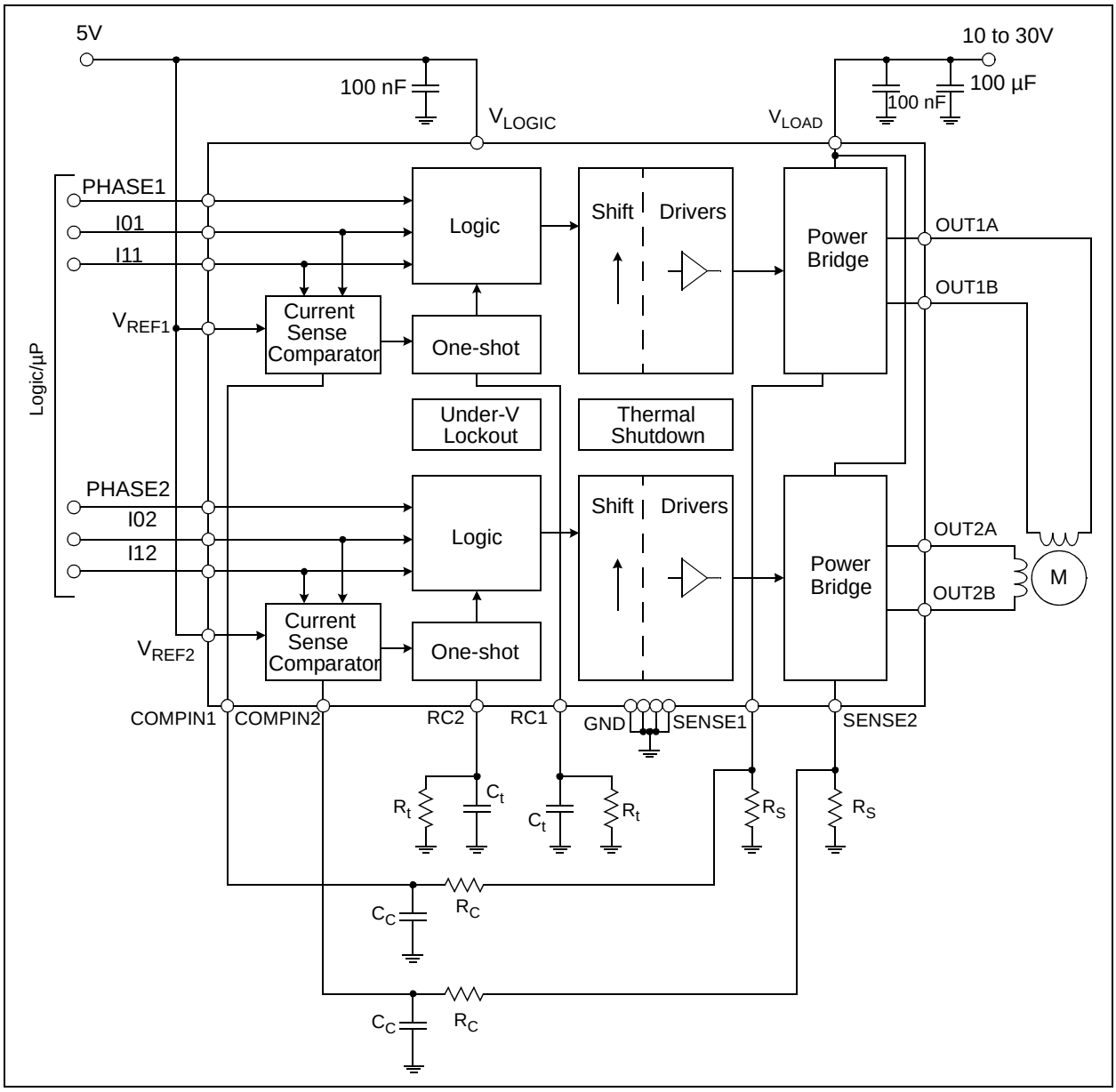
Functional Block Diagram



Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Logic Supply Voltage (V_{LOGIC}) ..... -0.3 to +5.5V
Load Supply Voltage (V_{LOAD}) ..... -0.3 to +40.0V
Logic Input Voltage Range (V_{IN}) ..... -0.3 to VLOGIC + 0.3V
V_{REF} Voltage Range (V_{REF})..... -0.3 to +10.0V
Output Current (Peak) ..... ±1A
Output Current (Continuous) ..... ±0.75A
Sense Output Voltage ..... -0.3V to 1.5V
Junction Temperature (T_J).....-40°C to +150°C
Operating Temperature Range (T_{OPR}).....-40°C to +105°C
Storage Temperature Range (T_{STG}) .....-55°C to +150°C

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits are established for V_{LOGIC} = 4.5V to 5.5V, V_{LOAD} = 30V,V_{REF} = 5V, T_A = +25°C

Parameters	Sym	Min	Typ	Max	Units	Conditions
DC Characteristics						
Logic Supply Voltage	V_{LOGIC}	4.5	5.0	5.5	V	
Load Supply Voltage	V_{LOAD}	10	30	40	V	
Logic Supply Current	I_{VLOGIC}	—	0.8	1.0	mA	
V_{REF} Voltage Range	V_{REF}	1.5	5.0	7.0	V	
Driver Supply Current	I_{VLOAD_ON}	—	0.55	1.0	mA	Both Bridges ON, No Load
	I_{VLOAD_OFF}	—	0.55	1.0	mA	Both Bridges Off
Control Logic Input Current (V_{IN} = 0V)	I_{IN}	—	—	-70	µA	I01, I11, I02, I12, PHASE1, PHASE2, **(Note 1)**
Logic-Low Input Voltage	V_{IL}	—	—	0.8	V	I01, I11, I02, I12, PHASE1, PHASE2
Logic-High Input Voltage	V_{IH}	2.4	—	—	V	I01, I11, I02, I12, PHASE1, PHASE2
Current Limit Threshold Ratio ($V_{REF} \div V_{SENSE}$)	V_{REF_VSENSE}	9.5	10	10.5	—	I0 = L, I1 = L
		13.5	15	16.5	—	I0 = H, I1 = L
		25.5	30	34.5	—	I0 = L, I1 = H
Driver Output Saturation Voltage $V_{CE(SAT)}$	V_{ONN} (Low Side)	—	0.55	0.65	V	(Sink) I_{OUT} = +500 mA
		—	0.90	1.00	V	(Sink) I_{OUT} = +750 mA
	V_{ONP} (High Side)	—	1.05	1.40	V	(Source) I_{OUT} = -500 mA
		—	1.85	2.10	V	(Source) I_{OUT} = -750 mA
Clamp Diode Forward Voltage **(Note 2)**	V_{F_NDIODE}	—	0.95	1.30	V	I_F = 750 mA
	V_{F_PDIODE}	—	1.00	1.30	V	I_F = 750 mA
Driver Output Leakage Current	I_{LEAK}	—	—	-50	µA	V_{OUT} = 0V
		—	—	50	µA	V_{OUT} = V_{LOAD}
Thermal Shutdown Temperature	T_{J_SHDN}	—	170	—	°C	
AC Characteristics						
Cut-off Time (one-shot pulse)	T_{OFF}	—	50	58	µs	R_s = 1Ω, R_C = 1 kΩ, C_C = 820 pF, R_t = 56 kΩ, C_t = 820 pF
Turn-off Delay	T_D	—	1.5	10	µs	

Note 1: V_{IN} = 5.0V input current given by internal pull-up to Logic Supply.
2: Clamp/Freewheel diode is the intrinsic body-drain diode of the NMOS and PMOS transistors.

TEMPERATURE SPECIFICATIONS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Recommended Temperature Ranges						
Junction Temperature Range	T_J	-40		+125	°C	
Operating Temperature Range	T_A	-40		+105	°C	
Thermal Package Resistance						
Thermal Resistance, SOP-24	θ_{JA}	—	76	—	°C/W	EIA/JEDEC JESD51-10
Thermal Resistance, SOP-24	θ_{JC}	—	16	—	°C/W	EIA/JEDEC JESD51-10

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: MTS62C19A PIN FUNCTION TABLE

Pin No. SOP-24	Type	Name	Function
1	Output	OUT1A	Output 1 ‘A’ Side of Motor Winding
2	Output	OUT2A	Output 2 ‘A’ Side of Motor Winding
3	Input	SENSE2	Current Sense for Output 2
4	Input	COMPIN2	Current Sense Comparator Input for Output 2
5	Output	OUT2B	Output 2 ‘B’ Side of Motor Winding
6	Power	GND	Negative Logic Supply (Ground)
7	Power	GND	Negative Logic Supply (Ground)
8	Input	I02	Output 2 Current Selection Bit 0
9	Input	I12	Output 2 Current Selection Bit 1
10	Input	PHASE2	Output 2 Phase
11	Input	V_{REF2}	Output 2 Current Reference
12	Input	RC2	Output 2 RC Time Constant
13	Power	V_{LOGIC}	Positive Logic Supply Voltage
14	Input	RC1	Output 1 RC Time Constant
15	Input	V_{REF1}	Output 1 Current Reference
16	Input	PHASE1	Output 1 Phase
17	Input	I11	Output 1 Current Selection Bit 1
18	Power	GND	Negative Logic Supply (Ground)
19	Power	GND	Negative Logic Supply (Ground)
20	Input	I01	Output 1 Current Selection Bit 0
21	Output	OUT1B	Output 1 ‘B’ Side of Motor Winding
22	Input	COMPIN1	Current Sense Comparator Input for Output 1
23	Input	SENSE1	Current Sense for Output 1
24	Power	V_{LOAD}	Positive Load Supply Voltage

2.1 Output Stage (OUT1A, OUT2A, OUT1B, OUT2B)

Output connection to “A” side and “B” side of motor windings.

2.2 Current Sense Input (SENSE1, SENSE2)

Connection to lower sources of output stage for insertion of current sense resistor.

2.3 Current Sense Comparator Input (COMPIN1, COMPIN2)

Current sense comparator input.

2.4 Ground Terminal (GND)

Logic supply ground. Only the driver current flows out of this pin; there is no high current. Minimize voltage drops between this pin and the logic inputs.

2.5 Current Detection Selection (I01, I02, I11, I12)

Comparator input for current threshold detection. The voltage across the sense resistor is fed back to this input through the low-pass filter R_cC_c. The power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs, the current decays for a time set by R_tC_t (T_{OFF} = 1.1 R_tC_t).

2.6 Current Flow Direction Selection (PHASE1, PHASE2)

Logic input to select the direction of the current flow through the load. A “HIGH” logic signal level causes load current to flow from OUTxA to OUTxB. A “LOW” logic level causes load current to flow from OUTxB to OUTxA.

2.7 Current Sense Reference (V_{REF1}, V_{REF2})

Reference voltage for current sense comparator. Determines the level of output current detection together with sensing resistor and inputs I0x, I1x.

2.8 Output Stage OFF Time (RC1, RC2)

A parallel R_tC_t network connected to this pin sets the OFF time of the power transistors. The monostable pulse generator is triggered by the output of the current sense comparator.

2.9 Logic Supply Voltage (V_{LOGIC})

Connect V_{LOGIC} to the logic source voltage. Decouple the supply with a 0.1 µF ceramic capacitor mounted close to the V_{LOGIC} and GND terminals.

2.10 Load Supply Voltage (V_{LOAD})

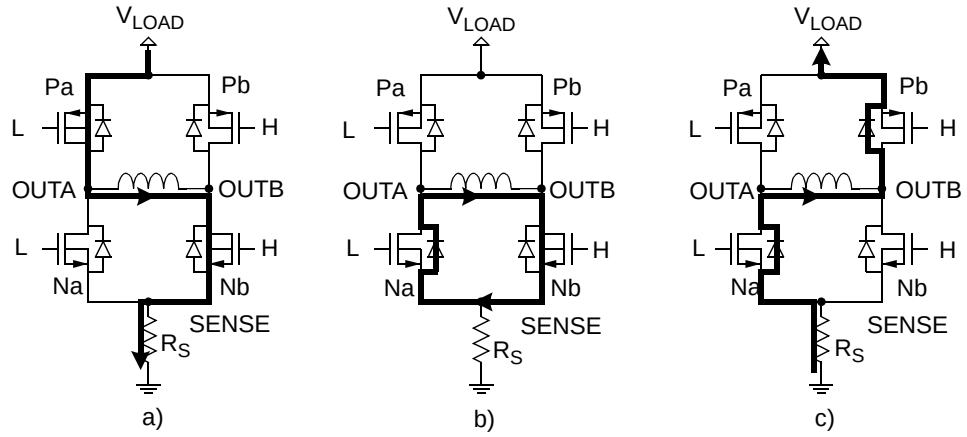
Connect V_{LOAD} to the motor positive voltage supply. The motor current is supplied through this pin and the selected output transistors.

3.0 FUNCTIONAL DESCRIPTION

The circuit is designed to drive the two windings of a bipolar stepper motor, and can be divided in two identical channels (channel 1 and channel 2) and protection circuitry for overtemperature and undervoltage. The functionality of a channel and protection circuitry is presented in the following sections.

3.1 Power Bridge Operation

Each motor winding is driven by an H-type bridge consisting of two N and two P transistors that allow the current to flow in both winding directions depending on the value of the PHASE signal (Table 3-1). The H-bridge can be set in five configurations that are related to the digital inputs PHASE, I0 and I1 and to the current sensed. These configurations are shown in Table 3-2.



Legend: a) Bridge ON, b) Source OFF, c) All OFF/Coasting

Note: For PHASE = L/Reverse, invert A and B in drawings.

FIGURE 3-1: *Power Bridge Control (PHASE = H/forward).*

TABLE 3-1: CURRENT DIRECTION CONTROL

Phase	Output Current
L	Current flows from OUTxB to OUTxA
H	Current flows from OUTxA to OUTxB

TABLE 3-2: POWER BRIDGE GATE CONTROL TRUTH TABLE

I0I1	PHASE	Overi	T_{OFF}	Case/Mode	gna	gpa	gnb	gpb
00/01/10	1	0	0	Forward ON	L	**L**	**H**	H
00/01/10	1	x	1	Forward OFF	L	H	**H**	H
00/01/10	0	0	0	Reverse ON	**H**	H	L	**L**
00/01/10	0	x	1	Reverse OFF	**H**	H	L	H
11	x	x	x	No Current/ Coasting	L	H	L	H

Legend: Bold = Active MOS Transistors, Overi = Overcurrent flag, T_{OFF} = Channel T_{OFF} State Flag

3.2 PWM Current Control

The current level in each motor winding is controlled by a PWM circuit with a fixed T_{OFF} time. The load current flowing in the winding is sensed through an external sensing resistor R_S, connected between the power bridge's source pin SENSE (sources of transistors Na and Nb) and GND.

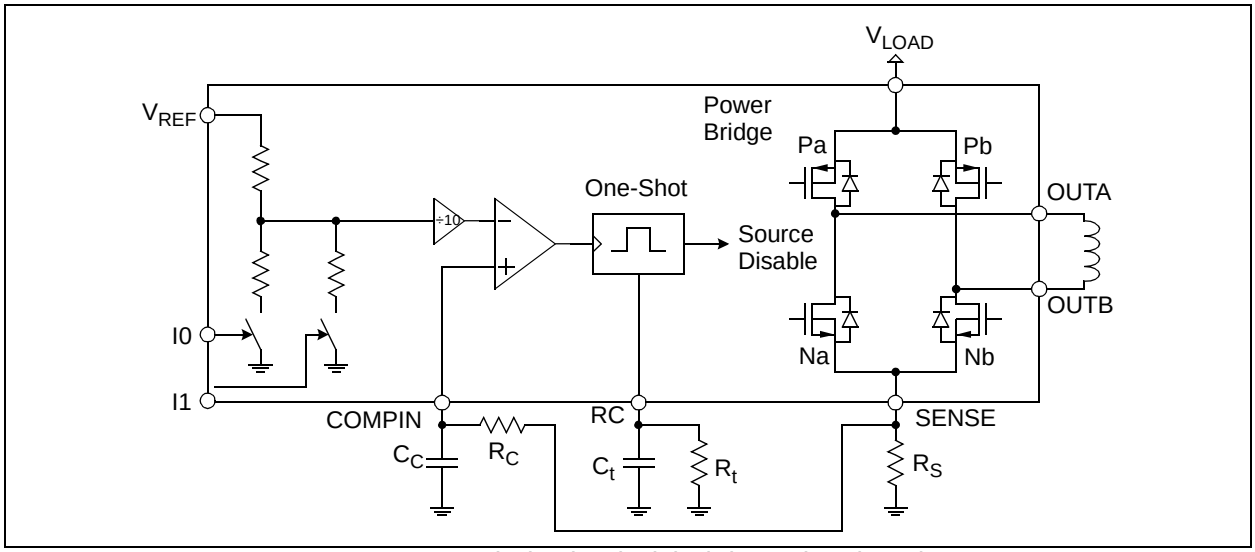


FIGURE 3-2: *PWM Current Control Circuit Principle (Channel 1 Shown).*

The voltage across R_S is compared to a fraction of the reference voltage V_{REF}, chosen with the logic input bits I0 and I1 (Table 3-3). The power bridge, and thus the load current, can also be switched off completely when both logic inputs are high. Note that any logic input left unconnected will be treated as a high level (pull-up resistor).

The maximum trip current for regulation, given for I0 I1 = 00 is calculated in Equation 3-1.

EQUATION 3-1:

$$I_{MAX} = \frac{V_{REF}}{10 \times R_S}$$

TABLE 3-3: CURRENT LEVEL CONTROL TRUTH TABLE

I0	I1	Comp. Trip Voltage	Output Current
0	0	V_{TRIP} = 1/10 x V_{REF}	$I_{MAX} = V_{REF}/10R_S$
1	0	V_{TRIP} = 1/15 x V_{REF}	2/3 x $I_{MAX} = V_{REF}/15R_S$
0	1	V_{TRIP} = 1/30 x V_{REF}	1/3 x $I_{MAX} = V_{REF}/30R_S$
1	1	x	0 (no current)

When the maximum allowed current is reached, the bridge source is turned off during a fixed period T_{OFF} (typically 50 µs) given by a non-retriggerable pulse generator and the external timing components R_t (20k – 100 kΩ range) and C_t (100 pF – 1000 pF range):

EQUATION 3-2:

$$T_{OFF} = 1.1 \times (R_t \times C_t)$$

During T_{OFF} the winding current decreases. When the driver is re-enabled, the winding current increases again until it reaches the threshold, and the cycle repeats itself, maintaining the load current at the desired level.

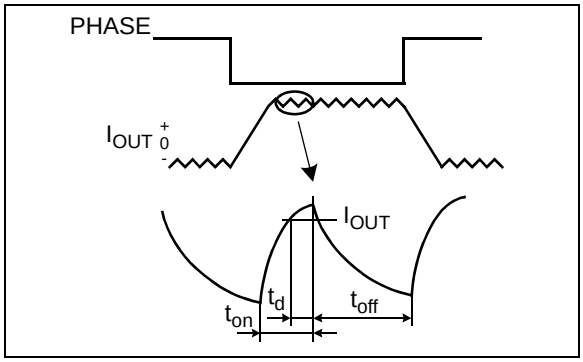


FIGURE 3-3: *PWM Output Current Waveform.*

3.3 Circuit Protection

A thermal protection circuitry turns off all drivers when the junction temperature exceeds a safe operating limit of +170°C (typical). This protects the devices from failure due to excessive heating. Despite this thermal protection, output short circuits are not permitted. The output drivers are re-enabled once junction temperature has dropped below +145°C (typical).

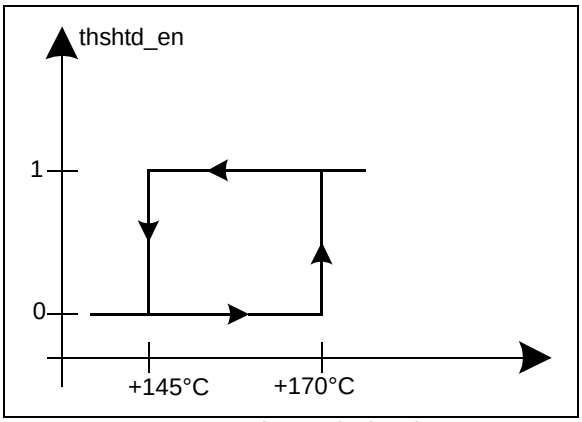


FIGURE 3-4: *Thermal Shutdown Output vs. Temperature Showing Hysteresis.*

An undervoltage lockout circuit protects the MTS62C19A from potential shoot-through currents when the load supply voltage is applied prior to the logic supply voltage. The power bridge and all outputs are disabled if V_{LOGIC} is smaller than 4V.

With this protection feature, the circuit will withstand any order of turn-on or turn-off of the supply voltages V_{LOGIC} and $V_{LOAD.}$ Normal dV/dt values are assumed.

4.0 APPLICATION CIRCUITS AND ISSUES

4.1 Typical Application

The MTS62C19A circuit, with external components for a typical application, is shown in Figure 4-1. Typical passive component values are: R_S = 1Ω, R_C = 1 kΩ, C_C = 820 pF, R_t = 56 kΩ and C_t = 820 pF.

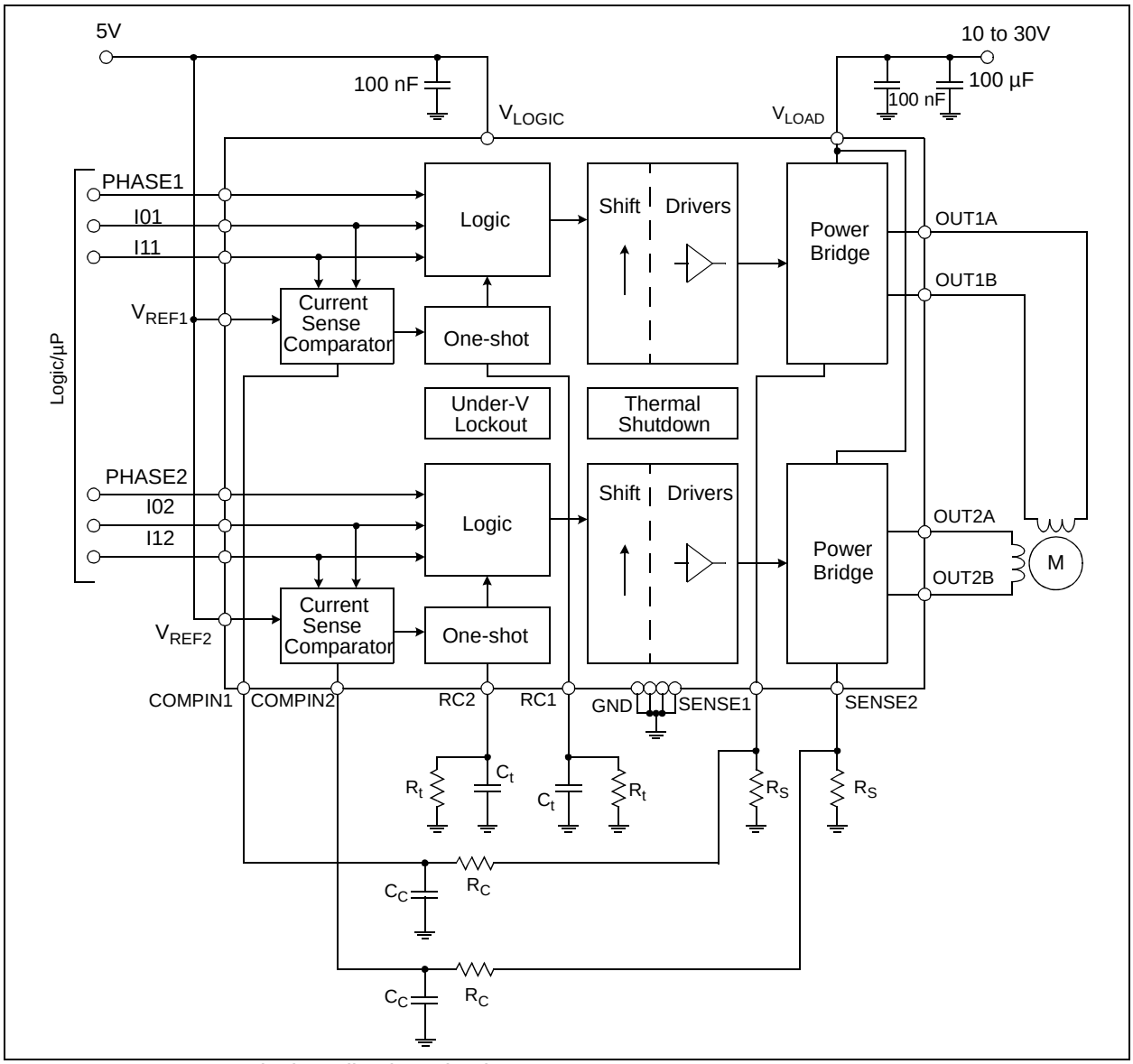


FIGURE 4-1: *Typical Application Circuit.*

During PWM operation, when the output stage is turned-on, large voltage peaks might appear across R_S, which can wrongly trigger the input comparator. To avoid an unstable current control, an external R_CC_C filter should be used that delays the comparator action. Depending on load type, many applications will not require this filter (SENSE connected to COMPIN).

4.2 Stepping Examples

The MTS62C19A control modes are full-step, half-step, modified half-step and microstepping control of the motor, as shown in Figure 4-2.

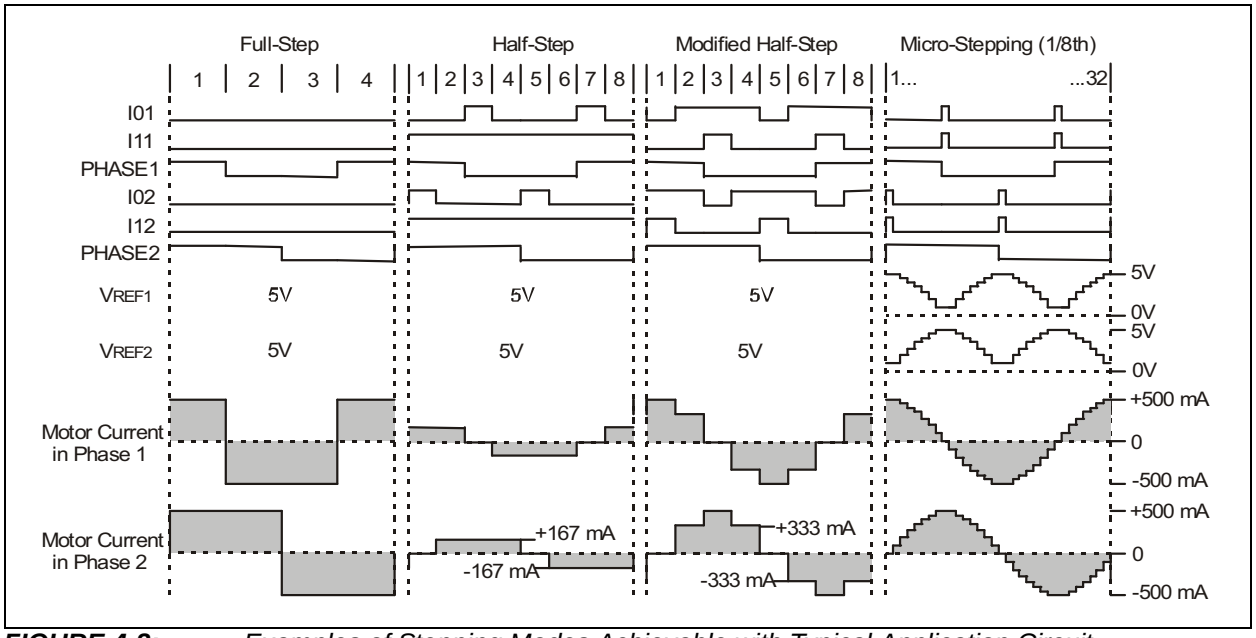


FIGURE 4-2: *Examples of Stepping Modes Achievable with Typical Application Circuit.*

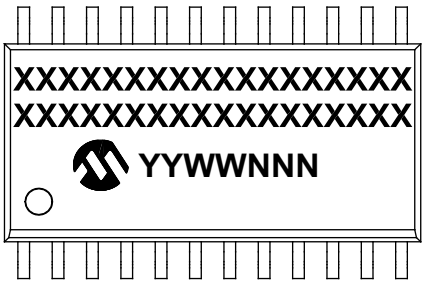
4.3 PCB Design Guidelines

Unused inputs should be connected to fixed voltage levels in order to get the highest noise immunity. Typical PCB layout guidelines for power applications should be followed. These include separate power ground planes, supply decoupling capacitors close to the IC, short connections and use of maximized copper areas to improve thermal dissipation.

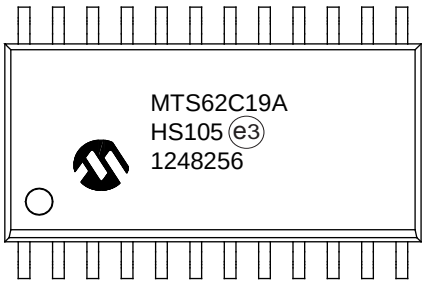
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

24-Lead SOP



Example

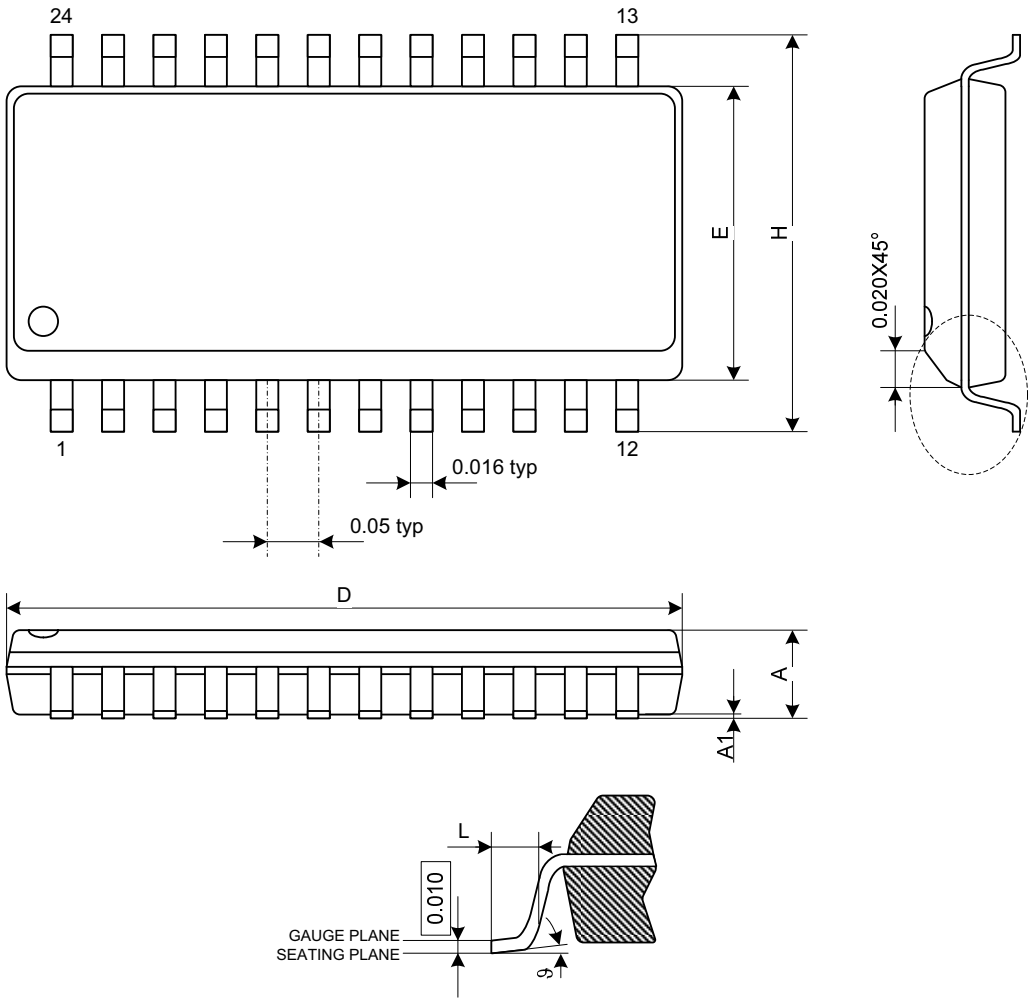


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

SOP 24L Package Outline

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Note: The package drawing dimensions are expressed in inches.

Symbol	Minimum	Typical	Maximum	Unit
A	—	—	2.642 (0.104)	mm (inch)
A1	0.102 (0.004)	—	—	mm (inch)
D	15.545 (0.612)	15.697 (0.618)	15.850 (0.624)	mm (inch)
E	7.417 (0.292)	7.518 (0.296)	7.595 (0.299)	mm (inch)
H	10.287 (0.405)	10.464 (0.412)	10.643 (0.419)	mm (inch)
L	0.533 (0.021)	0.787 (0.031)	1.041 (0.041)	mm (inch)
J	0	4	8	°

Note 1: JEDEC outline: M0-119 AA

2: Dimensions “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs should not exceed 0.25mm (0.010inch) per side.

3: Dimensions “E” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

APPENDIX A: REVISION HISTORY

Revision C (March 2013)

The following is the list of modifications:

1. Corrected one dimension in the package drawing. Added a note mentioning the unit type used in the drawing.
2. Minor editorial changes.

Revision B (December 2012)

The following is the list of modifications:

1. Updated Operating Temperature Range throughout the document.
2. Corrected Typical Application diagram.
3. Added **Section 5.1, Package Marking Information**.
4. Added Product Identification System section.

Revision A (September 2010)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	X	XXX
Device	Tube/Tape and Reel	Package	Fixed Characters

Device:	MTS62C19A: Dual Full-Bridge Motor Driver		
Packing Type:	H	=	Tube
	L	=	Tape and Reel
Package:	S*	=	24-Lead Plastic Small Outline (SOP)

* These devices are formerly products of Advanced Silicon

Examples:

a) MTS62C19A-HS105 Tube, 24LD SOP Package

b) MTS62C19A-LS105 Tape and Reel, 24LD SOP Package

NOTES:

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