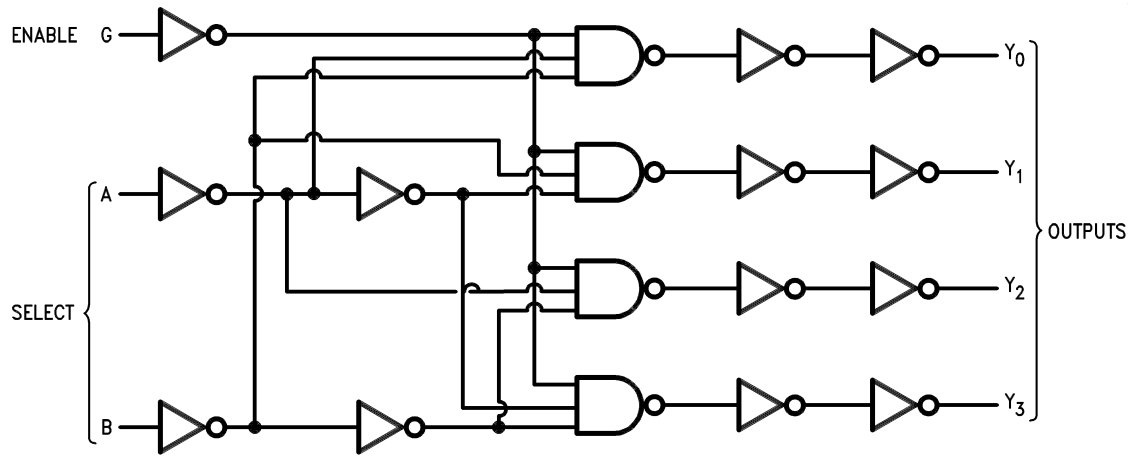## Logic Diagram

(1 of 2)

Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC} +1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC} +0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Note:

1. Unless otherwise specified all voltages are referenced to ground.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times			ns
	$V_{CC} = 2.0V$		1000	
	$V_{CC} = 4.5V$		500	
	$V_{CC} = 6.0V$		400	

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DC Electrical Characteristics[(2)]

Symbol	Parameter	Conditions	V$_{CC}$	T$_A$ = 25°C				Units
				Typ.	Guaranteed Limits			
						T$_A$ = −40 to 85°C	T$_A$ = −55 to 125°C	
V$_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	
			6.0V		4.2	4.2	4.2	
V$_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	
			6.0V		1.8	1.8	1.8	
V$_{OH}$	Minimum HIGH Level Output Voltage	V$_{IN}$ = V$_{IH}$ or V$_{IL}$: |I$_{OUT}$| ≤ 20µA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	
			6.0V	6.0	5.9	5.9	5.9	
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$: |I$_{OUT}$| ≤ 4.0mA	4.5V	4.2	3.98	3.84	3.7	
		|I$_{OUT}$| ≤ 5.2mA	6.0V	5.7	5.48	5.34	5.2	
V$_{OL}$	Maximum LOW Level Output Voltage	V$_{IN}$ = V$_{IH}$ or V$_{IL}$: |I$_{OUT}$| ≤ 20µA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	
			6.0V	0	0.1	0.1	0.1	
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$: |I$_{OUT}$| ≤ 4.0mA	4.5V	0.2	0.26	0.33	0.4	
		|I$_{OUT}$| ≤ 5.2mA	6.0V	0.2	0.26	0.33	0.4	
I$_{IN}$	Maximum Input Current	V$_{IN}$ = V$_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	µA
I$_{CC}$	Maximum Quiescent Supply Current	V$_{IN}$ = V$_{CC}$ or GND, I$_{OUT}$ = 0µA	6.0V		8.0	80	160	µA

Note:

2. For a power supply of 5V ±10% the worst case output voltages (V$_{OH}$, and V$_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V$_{IH}$ and V$_{IL}$ occur at V$_{CC}$ = 5.5V and 4.5V respectively. (The V$_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current (I$_{IN}$, I$_{CC}$, and I$_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ns.

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 4 levels of delay		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 5 levels of delay		28	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to any Output		19	30	ns

AC Electrical Characteristics

$C_L = 50$ pF, $t_r = t_f = 6$ns (unless otherwise specified).

| Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ.	$T_A = 25°C$	$T_A = -40$ to 85°C	$T_A = -55$ to 125°C	Units
					Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 4 levels of delay	(3)	2.0V	110	175	219	254	ns
			4.5V	22	35	44	51	
			6.0V	18	30	38	44	
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 5 levels of delay	(4)	2.0V	165	220	275	320	ns
			4.5V	33	44	55	64	
			6.0V	28	38	47	54	
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to any Output		2.0V	115	175	219	254	ns
			4.5V	23	35	44	51	
			6.0V	19	30	38	44	
t_{TLH}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	
			6.0V	7	13	16	19	
C_{IN}	Maximum Input Capacitance			3	10	10	10	pF
C_{PD}	Power Dissipation Capacitance(5)	(5)		75				pF

Notes:

3. 4 levels of delay are A to Y1, Y3 and B to Y2, Y3.

4. 5 levels of delay are A to Y0, Y2 and B to Y0, Y1.

5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

LAND PATTERN RECOMMENDATION
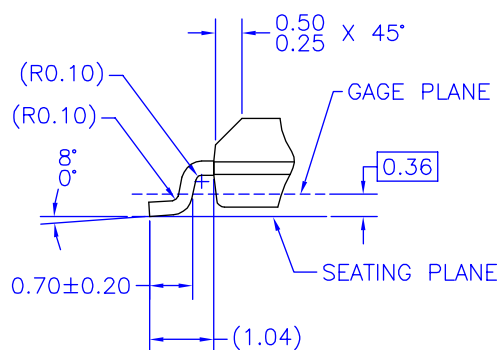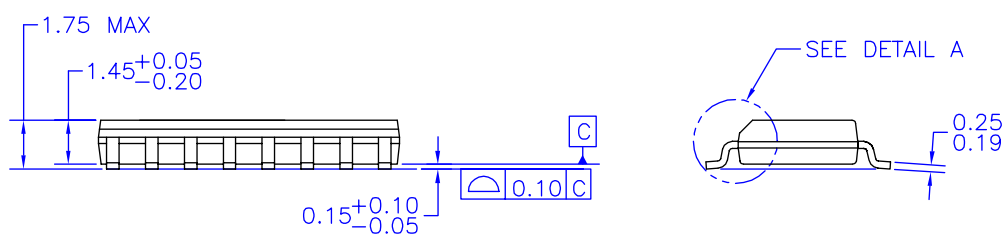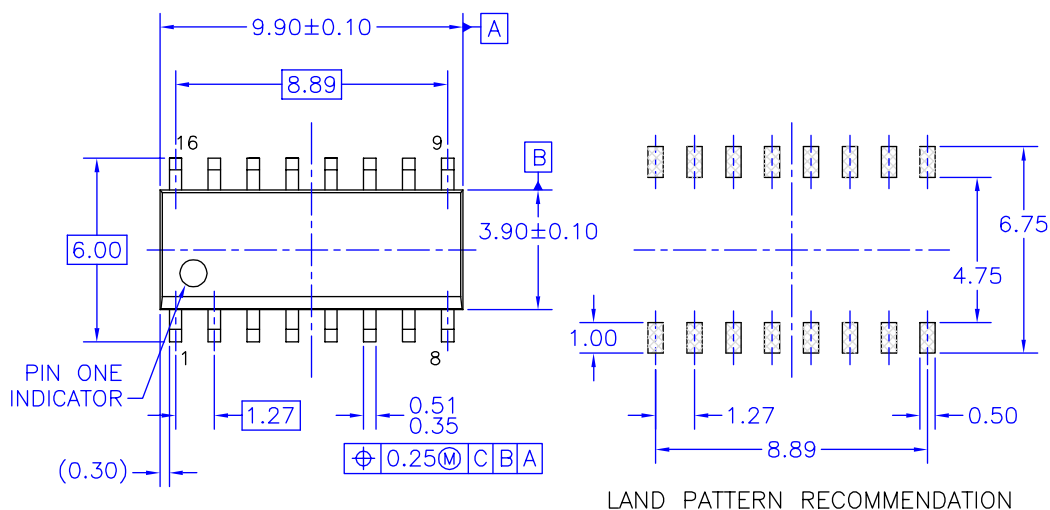
NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC
    MS-012, VARIATION AC, ISSUE C,
    DATED MAY 1990.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
    FLASH OR BURRS.
D) STANDARD LEAD FINISH:
    200 MICROINCHES / 5.08 MICRONS MIN.
    LEAD/TIN (SOLDER) ON COPPER.

DETAIL A
SCALE: 2:1

M16AREVK

**Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

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