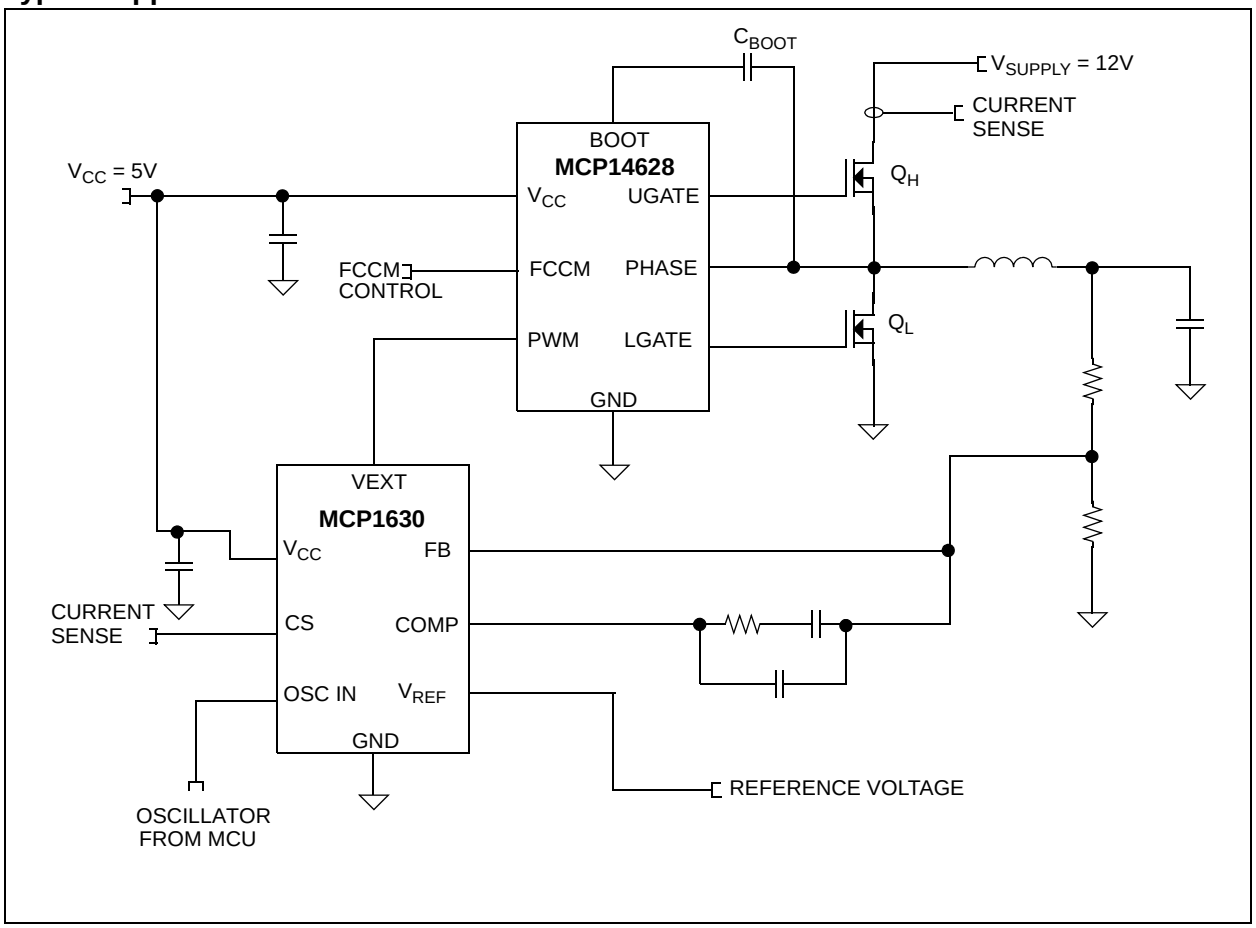
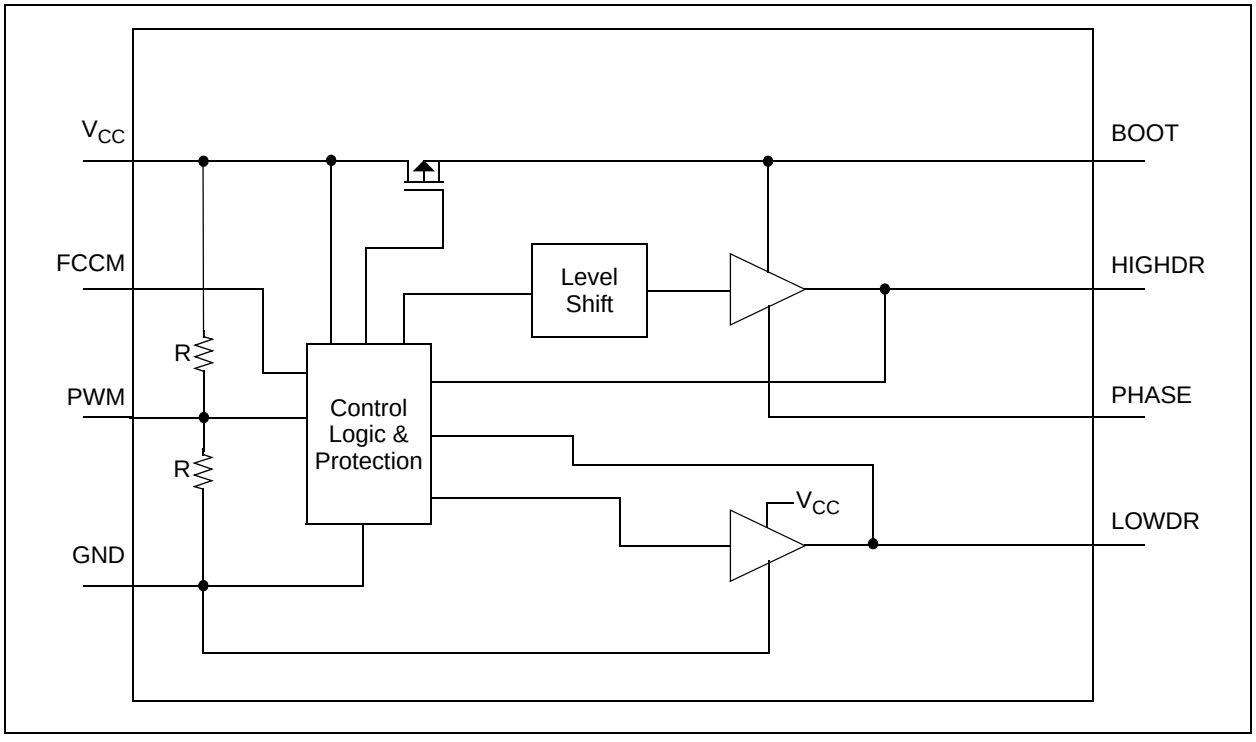
Typical Application Schematic



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{CC}, Device Supply Voltage.....-0.3V to +7.0V
V_{BOOT}, BOOT Voltage.....-0.3V to +36.0V
V_{PHASE}, Phase Voltage.....V_{BOOT} - 7.0V to V_{BOOT} + 0.3V
V_{FCCM}, FCCM Voltage..... -0.3V to V_{CC} + .0.3V
V_{PWM}, PWM Voltage..... -0.3V to V_{CC} + 0.3V
V_{UGATE}, UGATE Voltage..... V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{LGATE}, LGATE Voltage..... -0.3V to V_{CC} + 0.3V
ESD Protection on all Pins.....2 kV (HBM)

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, V_{CC} = 5V, T_J = -40°C to +125°C

Parameters	Sym	Min	Typ	Max	Units	Conditions
V_{CC} Supply Requirements						
Recommended Operating Range	V_{CC}	4.5	5.0	5.5	V	
Bias Supply Voltage	I_{VCC}	—	80	—	µA	PWM pin floating, V_{FCCM} = 5V
UVLO (Rising V_{CC})		—	3.40	3.90	V	
UVLO (Falling V_{CC})		2.40	2.90	—	V	
Hysteresis		—	500	—	mV	
PWM Input Requirements						
PWM Input Current	I_{PWM}	—	250	—	µA	V_{PWM} = 5V
		—	-250	—	µA	V_{PWM} = 0V
PWM Rising Threshold		0.70	1.00	1.30	V	
PWM Falling Threshold		3.50	3.80	4.10	V	
Tri-State Shutdown Hold-off Time	t_{TSSHD}	100	175	250	ns	T_A = +25°C, **Note 2**
FCCM input Requirements						
FCCM Low Threshold		0.50	—	—	V	
FCCM High Threshold		—	—	2.0	V	
Output Requirements						
High Drive Source Resistance		—	1.0	2.5	Ω	500 mA source current, **Note 1**
High Drive Sink Resistance		—	1.0	2.5	Ω	500 mA sink current, **Note 1**
High Drive Source Current		—	2.0	—	A	**Note 1**
High Drive Sink Current		—	2.0	—	A	**Note 1**
Low Drive Source Resistance		—	1	2.5	Ω	500 mA source current, **Note 1**
Low Drive Sink Resistance		—	0.5	1.0	Ω	500 mA sink current, **Note 1**
Low Drive Source Current		—	2.0	—	A	**Note 1**
Low Drive Sink Current		—	3.5	—	A	**Note 1**

Note 1: Parameter ensured by design, not production tested.
2: See Figure 4-1 for parameter definition.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, V_{CC} = 5V, T_J = -40°C to +125°C						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Switching Times						
HIGHDR Rise Time	t_{RH}	—	10	—	ns	C_L = 3.3nF, **Note 1**, **Note 2**
LOWDR Rise Time	t_{RL}	—	10	—	ns	C_L = 3.3nF, **Note 1, Note 2**
HIGHDR Fall Time	t_{FH}	—	10	—	ns	C_L = 3.3nF, **Note 1, Note 2**
LOWDR Fall Time	t_{FL}	—	6.0	—	ns	C_L = 3.3nF, **Note 1, Note 2**
HIGHDR Turn-off Propagation Delay	t_{PDLH}	—	15	—	ns	No Load, **Note 2**
LOWDR Turn-off Propagation Delay	t_{PDLL}	—	16	—	ns	No Load, **Note 2**
HIGHDR Turn-on Propagation Delay	t_{PDHH}	10	18	30	ns	No Load, **Note 2**
LOWDR Turn-on Propagation Delay	t_{PDHL}	10	22	30	ns	No Load, **Note 2**
Tri-State Propagation Delay	t_{PTS}	—	35	—	ns	No Load, **Note 2**
Minimum LOWDR On Time in DCM	t_{LGMIN}	—	400	—	ns	FCCM pin low **Note 1**

Note 1: Parameter ensured by design, not production tested.

2: See Figure 4-1 for parameter definition.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with V_{CC} = 5V.						
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-DFN (3x3)	θ_{JA}	—	60.0	—	°C/W	Typical Four-layer board with vias to ground plane

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with V_{CC} = 5.0V.

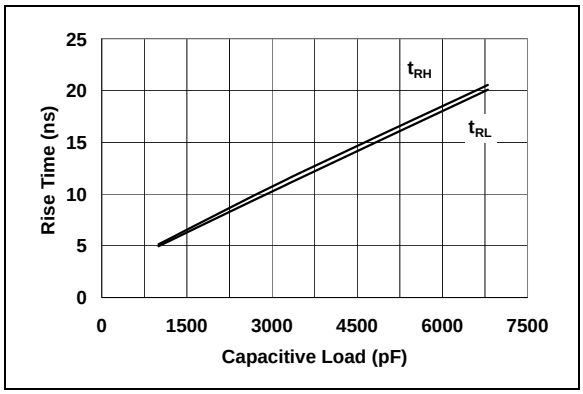


FIGURE 2-1: *Rise Times vs. Capacitive Load.*

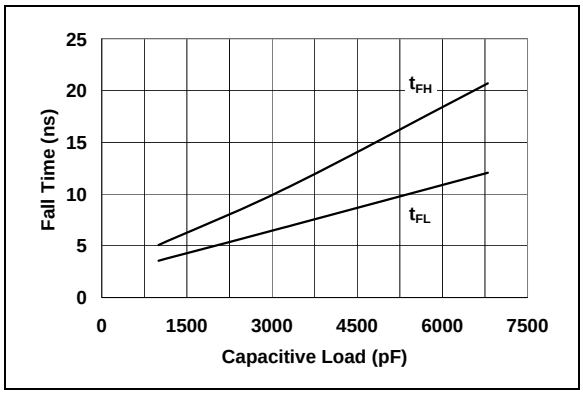


FIGURE 2-4: *Fall Times vs. Capacitive Load.*

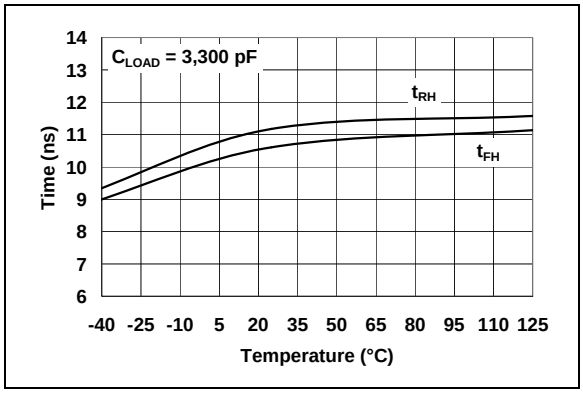


FIGURE 2-2: *HIGHDR Rise and Fall Time vs. Temperature.*

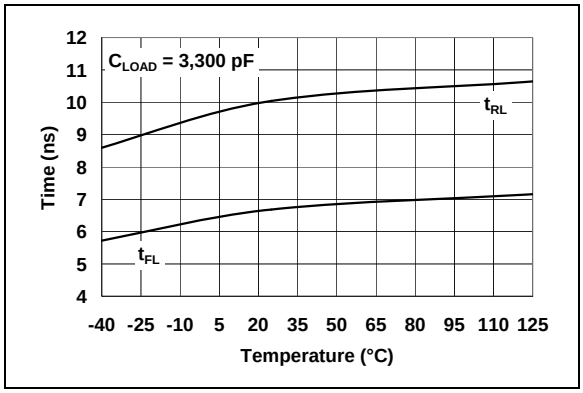


FIGURE 2-5: *LOWDR Rise and Fall Time vs. Temperature.*

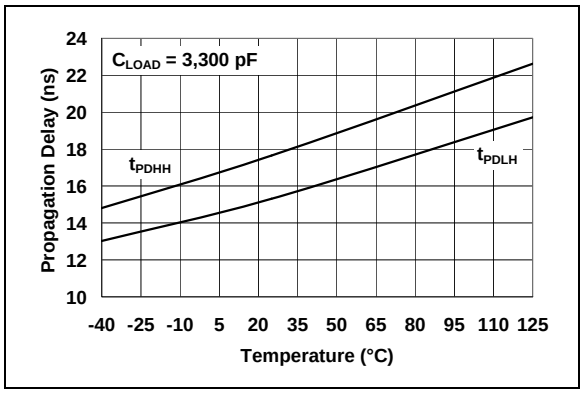


FIGURE 2-3: *HIGHDR Propagation Delay vs. Temperature.*

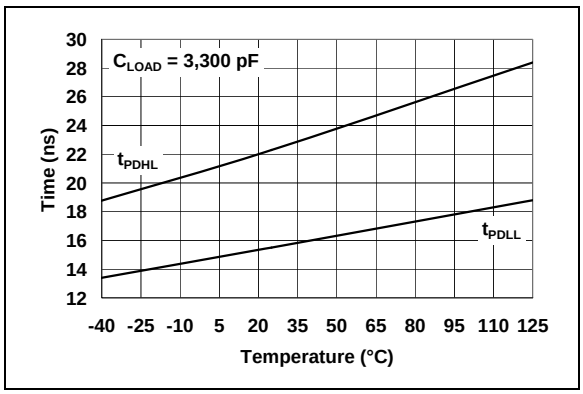


FIGURE 2-6: *LOWDR Propagation Delay vs. Temperature.*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25°C with V_{CC} = 5.0V.

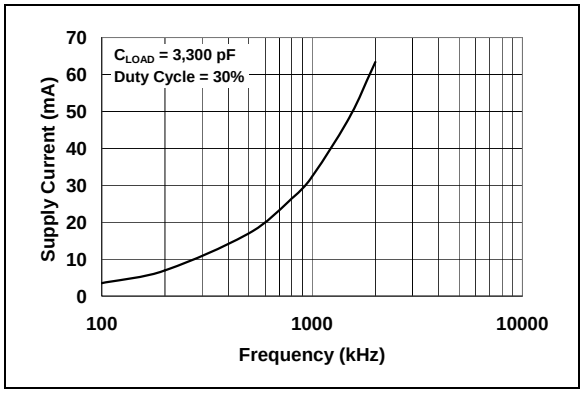


FIGURE 2-7: *Supply Current vs. Frequency.*

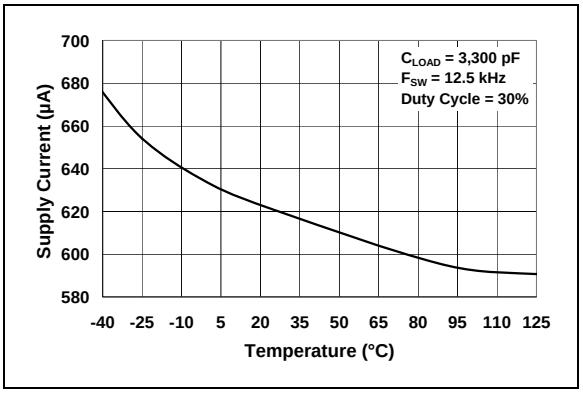


FIGURE 2-10: *Supply Current vs. Temperature.*

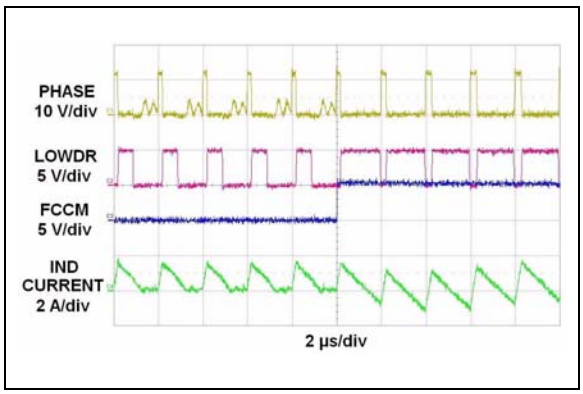


FIGURE 2-8: *DCM to CCM Transition Operation.*

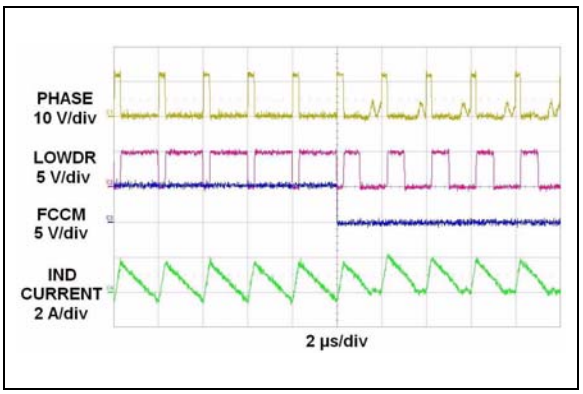


FIGURE 2-11: *CCM to DCM Transition Operation.*

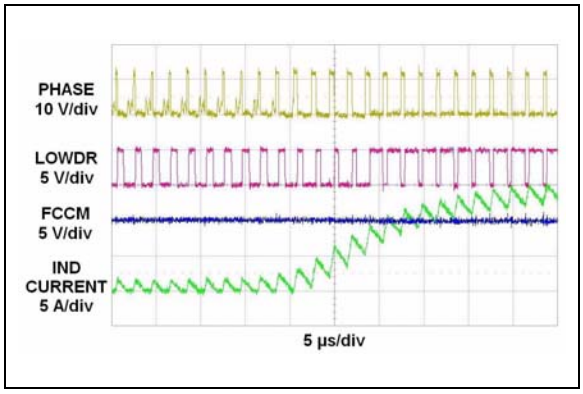


FIGURE 2-9: *Load Transition (0.5A - 15A).*

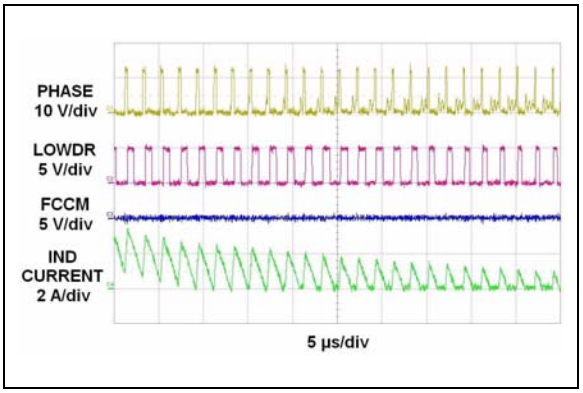


FIGURE 2-12: *Load Transition (15A - 0.5A).*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25°C with V_{CC} = 5.0V.

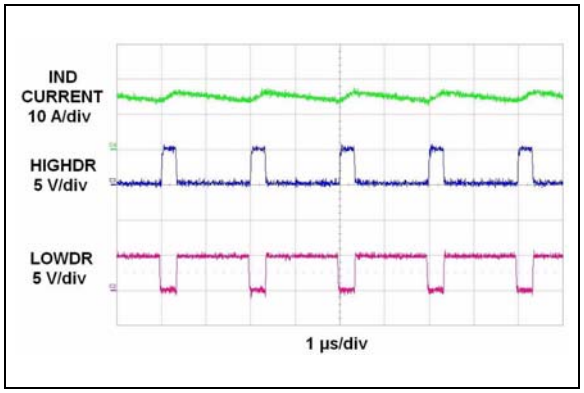


FIGURE 2-13: *HIGHDR and LOWDR Operation.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE .

SOIC	3x3 DFN	Symbol	Description
1	1	HIGHDR	High-side Gate Driver Pin
2	2	BOOT	Floating Bootstrap Supply Pin
3	3	PWM	PWM Input Control Pin
4	4	GND	Ground
5	5	LOWDR	Low-side Gate Driver Pin
6	6	V_{CC}	Supply Input Voltage
7	7	FCCM	Forced Continuous Conduction Mode Pin
8	8	PHASE	Switch Node Pin
—	PAD	NC	Exposed Metal Pad

3.1 High-side Gate Driver Pin (HIGHDR)

The HIGHDR pin provides the gate drive signal to control the high-side power MOSFET. The gate of the high-side power MOSFET is connected to this pin.

3.2 Floating Bootstrap Supply Pin (BOOT)

The BOOT pin is the floating bootstrap supply pin for the high-side gate drive. A capacitor is connected between this pin and the PHASE pin to provide the necessary charge to turn on the high-side power MOSFET.

3.3 PWM Input Control Pin (PWM)

The control input signal is supplied to the PWM pin. This tri-state pin controls the state of the HIGHDR and LOWDR pins. Placing a voltage equal to $V_{CC}/2$ on this pin causes both the HIGHDR and LOWDR to a low state.

3.4 Ground Pin (GND)

The GND pin provides ground for the MCP14628 circuitry. It should have a low impedance connection to the bias supply source return. High peak currents will flow out the GND pin when the low-side power MOSFET is being turned off.

3.5 Low-side Gate Driver Pin (LOWDR)

The LOWDR pin provides the gate drive signal to control the low-side power MOSFET. The gate of the low-side power MOSFET is connected to this pin.

3.6 Supply Input Voltage Pin (V_{CC})

The V_{CC} pin provides bias to the MCP14628. A bypass capacitor is to be placed between this pin and the GND pin. This capacitor should be placed as close to the MCP14628 as possible.

3.7 Forced Continuous Conduction Mode Pin (FCCM)

The FCCM pin enables or disables the forced continuous conduction mode. With the FCCM pin connected to ground the MCP14628 enters a diode emulation mode to improve system efficiency at light loads. Continuous conduction is forced if the FCCM pin is connected to V_{CC}.

3.8 Switch Node Pin (PHASE)

The PHASE pin provides the return path for the high-side gate driver. The source of the high-side power MOSFET is connected to this pin.

3.9 DFN Exposed Pad

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP14628 is a dual MOSFET gate driver designed to optimally drive both high-side and low-side N-channel MOSFETs arranged in a non-isolated synchronous buck converter topology.

The MCP14628 is capable of suppling 2A (typical) peak current to the floating high-side power MOSFET that is connected to the HIGHDR pin. With the exception of a capacitor, all of the circuitry needed to drive this high-side N-channel MOSFET is internal to the MCP14628. A blocking device is placed between the V_{CC} and BOOT pins that allows the bootstrap capacitor to be charged to V_{CC} when the low-side power MOSFET is conducting. Refer to **Section 5.1**, for information on determining the proper size of the bootstrap capacitor. The HIGHDR is also capable of sinking 2A (typical) peak current.

The LOWDR is capable of sourcing 2A (typical) peak current and sinking 3.5A (typical) peak current. This helps ensure that the low-side power MOSFET stays turned off during the high dv/dt of the PHASE node.

4.2 Adaptive Cross-Conduction Protection

The MCP14628 prevents cross-conduction power loss by adaptively ensuring that the high-side and low-side power MOSFETs are not conducting simultaneously. When the PWM signal goes low, the HIGHDR is pulled low and the LOWDR signal is held low until the HIGHDR reach 1V (typically). At that time, the LOWDR is allowed to turn on.

4.3 FCCM Mode

The MCP14628 features a diode emulation mode to enhance the light load system efficiency. The FCCM pin enables or disables the diode emulating mode. With the FCCM pin grounded, diode emulation mode is entered. The forced continuous conduction mode is entered when the FCCM pin is connected to V_{CC}.

In diode emulation mode, the MCP14628 turns off the low-side power MOSFET when the inductor current reaches approximately zero even if the PWM input signal is still low. The LOWDR and HIGHDR both stay low until the next switching cycle begins. To prevent false termination of the LOWDR signal, there is a 400 ns minimum on time, t_{LGMIN}, of the LOWDR. This also ensures that the bootstrap capacitor is fully charged.

In forced continuous conduction mode, the LOWDR of the MCP14628 does not terminate until the PWM input signal transitions from a low to a high.

4.4 Tri-State PWM

The PWM input pin of the MCP14628 controls the high current LOWDR and HIGHDR drive signals. These signals have three distinct operating modes depending upon the state of the PWM input signal.

A logic low on the PWM pin cause the LOWDR drive signal to be high and the HIGHDR drive signal to be low. When the PWM signal transitions to a logic high, the LOWDR signal goes low and the HIGHDR signal go high. To ensure proper operation the PWM input signal should be capable of a logic low of 0V and a logic high of 5V.

The third operating mode of the drive signals occurs when the PWM signal is set to a value equal to $V_{CC}/2$ (typically). When the PWM signal dwells at this voltage for 175 ns (typically) the MCP14628 disables both LOWDR and HIGHDR drive signals. Both drive signals are pulled and held low. Once the PWM signal moves beyond $V_{CC}/2$, the MCP14628 removes the shutdown state of the drive signals.

4.5 Timing Diagram

The PWM signal applied to the MCP14628 is suppled by a controller IC that regulates the power supply output. The timing diagram in Figure 4-1 graphically depicts the PWM signal and the output signals of the MCP14628.

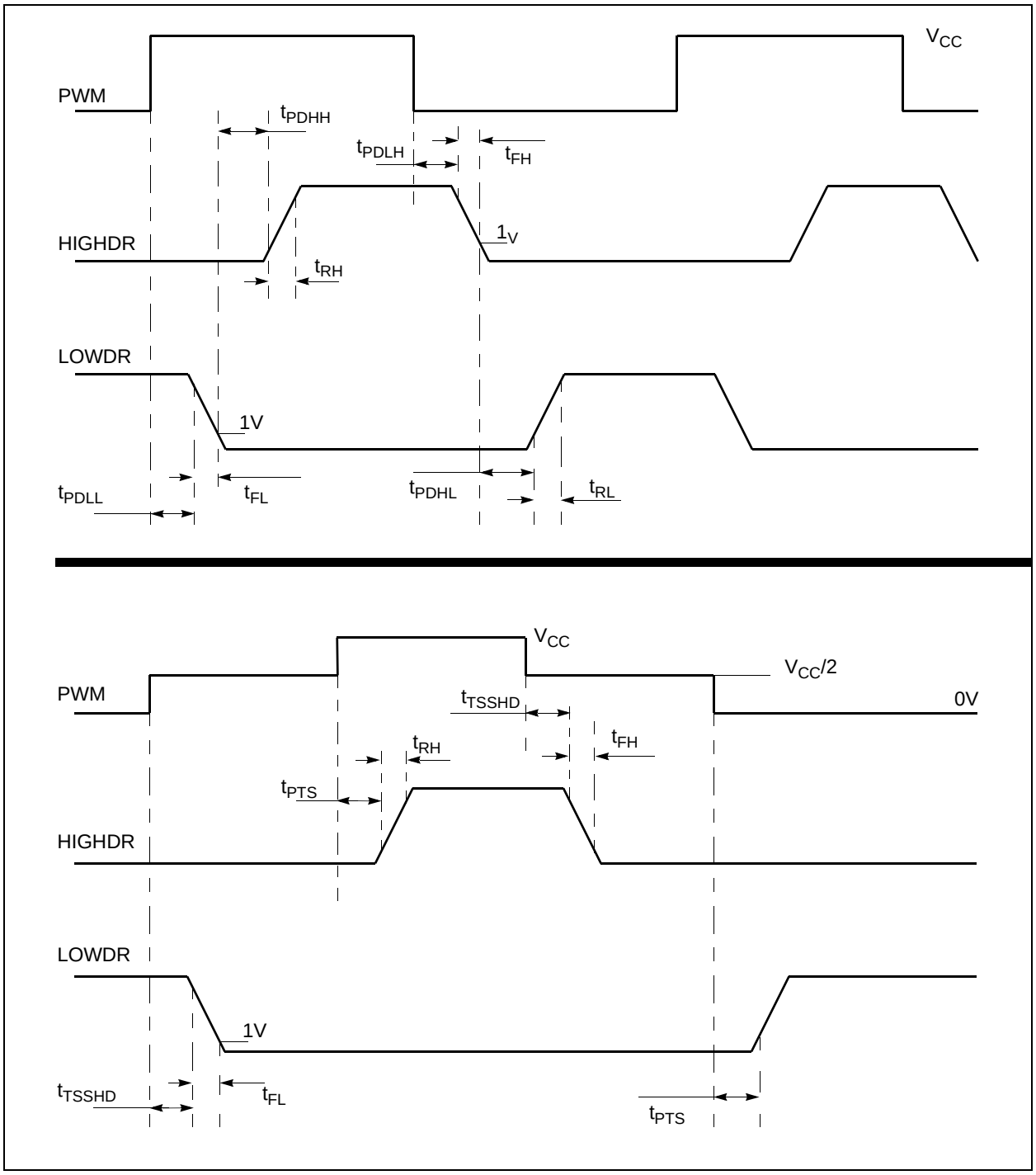


FIGURE 4-1: *MCP14628 Timing Diagram.*

5.0 APPLICATION INFORMATION

5.1 Bootstrap Capacitor Select

The selection of the bootstrap capacitor is based upon the total gate charge of the high-side power MOSFET and the allowable droop in gate drive voltage while the high-side power MOSFET is conducting.

EQUATION 5-1:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{DROOP}}$$

Where:

C_{BOOT}	=	bootstrap capacitor value
Q_{GATE}	=	total gate charge of the high-side MOSFET
ΔV_{DROOP}	=	allowable gate drive voltage droop

For example:

$$Q_{GATE} = 30\ nC$$

$$\Delta V_{DROOP} = 200\ mV$$

$$C_{BOOT} \geq 0.15\ uF$$

A low ESR ceramic capacitor is recommend with a maximum voltage rating that exceeds the maximum input voltage, V_{CC}, plus the maximum supply voltage, V_{SUPPLY}. It is also recommended that the capacitance of C_{BOOT} not exceed 1.2 uF.

5.2 Decoupling Capacitor

Proper decoupling of the MCP14628 is highly recommended to help ensure reliable operation. This decoupling capacitor should be placed as close to the MCP14628 as possible. The large currents required to quickly charge the capacitive loads are provided by this capacitor. A low ESR ceramic capacitor is recommended.

5.3 Power Dissipation

The power dissipated in the MCP14628 consists of the power loss associated with the quiescent power and the gate charge power.

The quiescent power loss can be calculated by the following equation and is typically negligible compared to the gate drive power loss.

EQUATION 5-2:

$$P_Q = I_{VCC} \times V_{CC}$$

Where:

P_Q	=	Quiescent Power Loss
I_{VCC}	=	No Load Bias Current
V_{CC}	=	Bias Voltage

The main power loss occurs from the gate charge power loss. This power loss can be defined in terms of both the high-side and low-side power MOSFETs.

EQUATION 5-3:

$$P_{GATE} = P_{HIGHDR} + P_{LOWDR}$$

$$P_{HIGHDR} = V_{CC} \times Q_{HIGH} \times F_{SW}$$

$$P_{LOWDR} = V_{CC} \times Q_{LOW} \times F_{SW}$$

Where:

P_{GATE}	=	Total Gate Charge Power Loss
P_{HIGHDR}	=	High-Side Gate Charge Power Loss
P_{LOWDR}	=	Low-Side Gate Charge Power Loss
V_{CC}	=	Bias Supply Voltage
Q_{HIGH}	=	High-Side MOSFET Total Gate Charge
Q_{LOW}	=	Low-Side MOSFET Total GAte Charge
F_{SW}	=	Switching Frequency

5.4 PCB Layout

Proper PCB layout is important in a high current, fast switching circuit to provide proper device operation. Improper component placement may cause errant switching, excessive voltage ringing, or circuit latch-up.

There are two important states of the MCP14628 outputs, high and low. Figure 5-1 depicts the current flow paths when the outputs of the MCP14628 are high and the power MOSFETs are turned on. Charge needed to turn on the low-side power MOSFET comes from the decoupling capacitor C_{VCC}. Current flows from this capacitor through the internal LOWDR circuitry, into the gate of the low-side power MOSFET, out the source, into the ground plane, and back to C_{VCC}. To reduce any excess voltage ringing or spiking, the inductance and area of this current loop must be minimized.

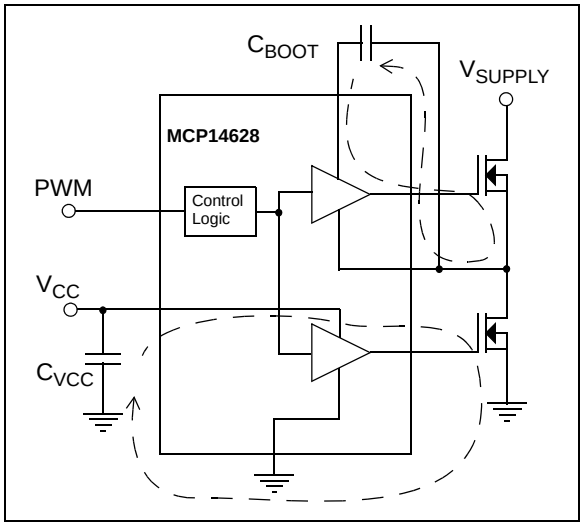


FIGURE 5-1: *Turn On Current Paths.*

The charge needed for the turning on of the high-side power MOSFET comes from the bootstrap capacitor C_{BOOT}. Current flows from C_{BOOT} through the internal HIGHDR circuitry, into the gate of the high-side power MOSFET, out the source, and back to C_{BOOT}. The printed circuit board traces that construct this current loop need to have a small area and low inductance. To control the inductance, short and wide traces must be used.

Figure 5-2 depicts the current flow paths when the outputs of the MCP14628 are low and the power MOSFETs are turned off. These current paths should also have low inductance and a small loop area to minimize voltage ringing and spiking.

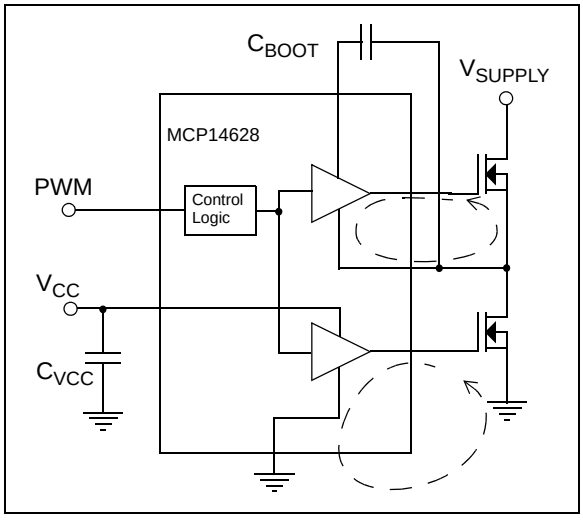


FIGURE 5-2: *Turn Off Current Paths.*

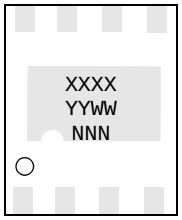
The following recommendations should be followed to allow for optimal circuit performance.

- The components that construct the high current paths previously mentioned should be placed close the MCP14628. The traces used to construct these current loops should be wide and short to keep the inductance and impedance low.
- A ground plane should be used to keep both the parasitic inductance and impedance minimized. The MCP14628 is capable of sourcing and sinking high peaks current and any extra parasitic inductance or impedance will result in non-optimal performance.

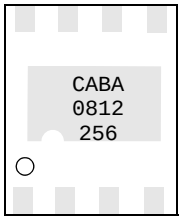
6.0 PACKAGING INFORMATION

6.1 Package Marking Information (Not to Scale)

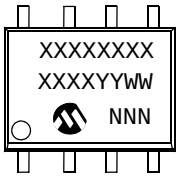
8-Lead DFN



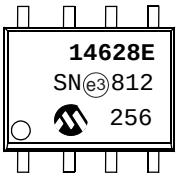
Example:



8-Lead SOIC (150 mil)



Example:

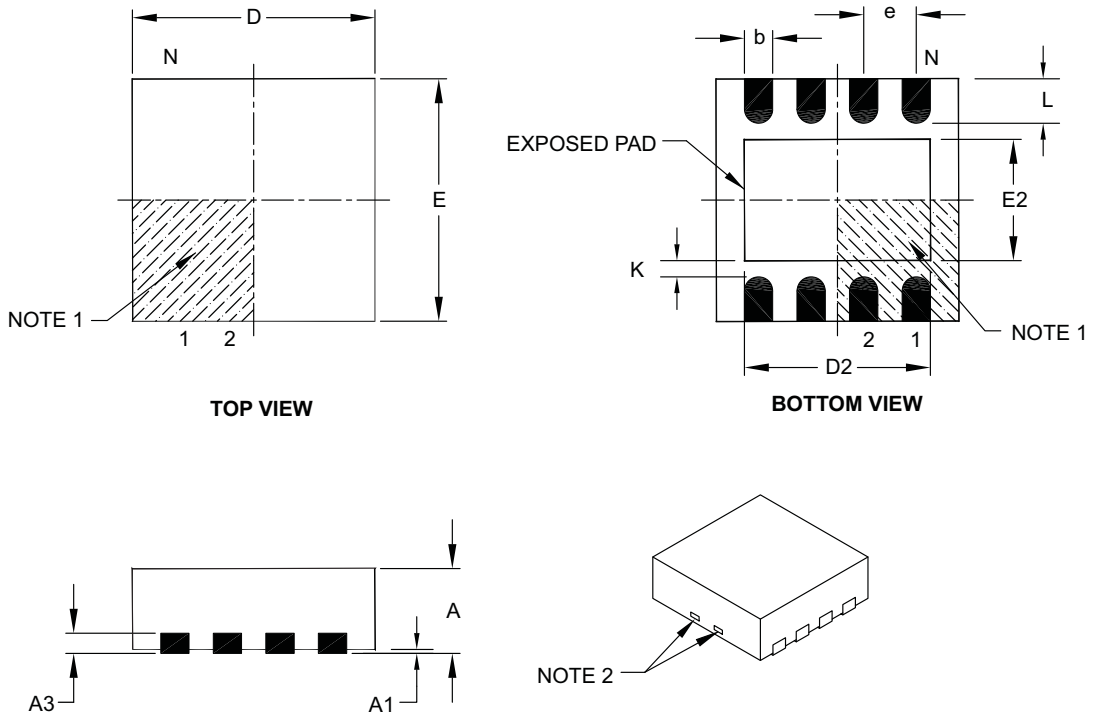


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	0.00	–	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	0.00	–	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

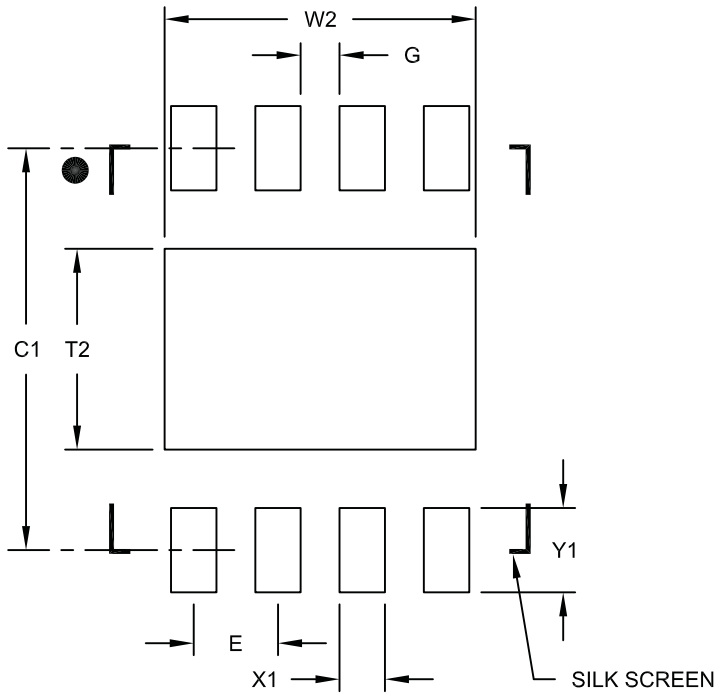
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B

8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

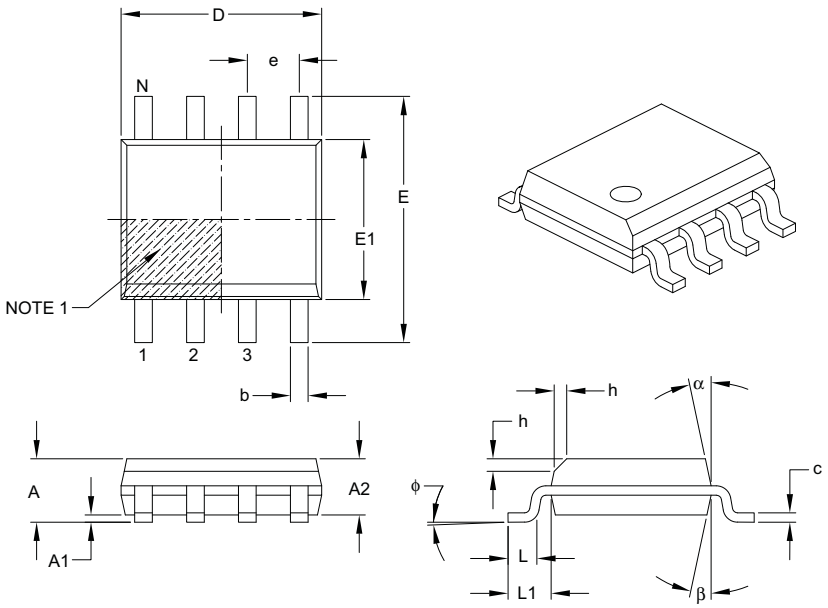
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062A

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

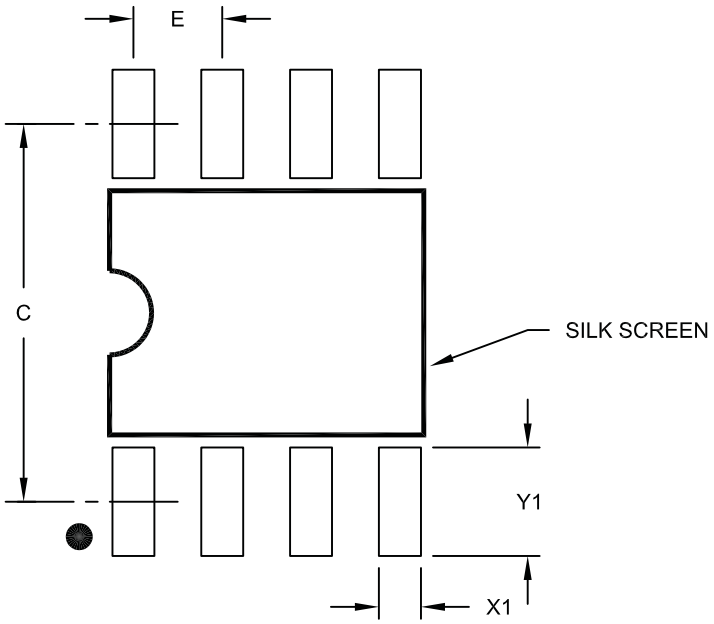
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2008)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device	MCP14628	2A Synchronous Buck Power MOSFET Driver
	MCP14628T	2A Synchronous Buck Power MOSFET Driver Tape and Reel
Temperature Range	E =	-40°C to +85°C
Package	MF =	Dual Flat, No Lead (3x3mm Body), 8-Lead
	SN =	Plastic SOIC (150 mil Body), 8-Lead

Examples:

a)	MCP14628-E/MF:	2A Synchronous Driver 8LD DFN Package
b)	MCP14628T-E/MF:	Tape and Reel, 2A Synchronous Driver 8LD DFN Package
c)	MCP14628-E/SN:	2A Synchronous Driver 8LD SOIC Package
d)	MCP14628T-E/SN:	Tape and Reel, 2A Synchronous Driver 8LD SOIC Package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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