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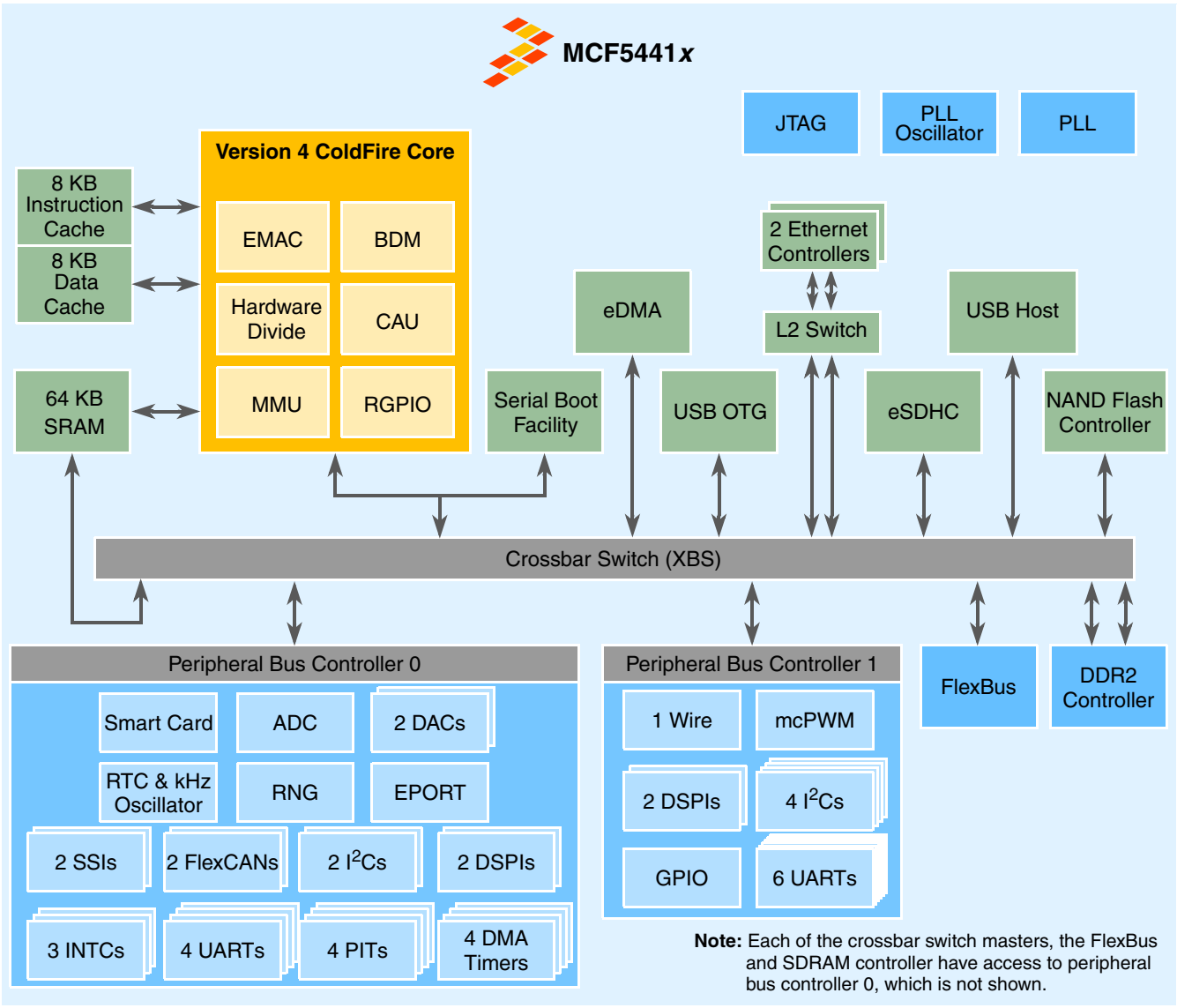


ADC – Analog-to-digital converter
BDM – Background debug module
CAU – Cryptography acceleration unit
DAC – Digital-to-analog
DSPI – DMA serial peripheral interface
eDMA – Enhanced direct memory access module
eSDHC – Enhanced Secure Digital host controller
EMAC – Enhanced multiply-accumulate unit
EPORT – Edge port module
GPIO – General purpose input/output module
I²C – Inter-Integrated Circuit
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
mcPWM – Motor control pulse width modulator
PIT – Programmable interrupt timers
PLL – Phase locked loop module
RGPIO – Rapid GPIO
RNG – Random number generator
RTC – Real time clock
SSI – Synchronous serial interface
USB OTG – Universal Serial Bus On-the-Go controller

1 MCF5441*x* family comparison

Table 1. MCF5441*x* family configurations

Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
Version 4 ColdFire core with EMAC (enhanced multiply-accumulate unit) and MMU (memory management unit)	•	•	•	•	•
Cryptography acceleration unit (CAU)	—	—	•	—	•
Core (system) and SDRAM clock	up to 250 MHz				
Peripheral clock (Core clock ÷ 2)	up to 125 MHz				
External bus (FlexBus) clock	up to 100 MHz				
Performance (Dhrystone 2.1 MIPS)	up to 385				
Static RAM (SRAM)	64 KB				
Independent data/instruction cache	8 KB each				
USB 2.0 Host controller	—	•	•	•	•
USB 2.0 Host/Device/On-the-Go controller	•	•	•	•	•
UTMI+ Low Pin Interface (ULPI) for external high-speed USB PHY	—	•	•	•	•
10/100 Mbps Ethernet controller with IEEE 1588 support	1	2	2	2	2
Level 2 IEEE 1588-compliant 3-port Ethernet switch	—	—	—	•	•
Enhanced Secure Digital host controller (eSDHC)	•	•	•	•	•
Smart card/Subscriber Identity Module (SIM)	—	2 ports	2 ports	2 ports	2 ports
UARTs	6	10	10	10	10
DSPI	3	4	4	4	4
CAN 2.0B controllers	1	2	2	2	2
I^2C	4	6	6	6	6
Synchronous serial interface (SSI)	1	2	2	2	2
12-bit ADC	—	•	•	•	•
12-bit DAC	—	2	2	2	2
32-bit DMA timers	4	4	4	4	4
Periodic interrupt timers (PIT)	4	4	4	4	4
Motor control PWM timer (mcPWM)	—	8 channel	8 channel	8 channel	8 channel
64-channel DMA controller	•	•	•	•	•
Real-time clock with 2 KB standby RAM and battery back-up input	•	•	•	•	•
DDR2 SDRAM controller	•	•	•	•	•
FlexBus external memory controller	•	•	•	•	•

Table 1. MCF5441*x* family configurations (continued)

Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
NAND flash controller	•	•	•	•	•
1-Wire® interface	•	•	•	•	•
Serial boot facility	•	•	•	•	•
Watchdog timer	•	•	•	•	•
Interrupt controllers (INTC)	3	3	3	3	3
Edge port module (EPORT)	3 IRQs	5 IRQs	5 IRQs	5 IRQs	5 IRQs
Rapid GPIO pins	9	16	16	16	16
General-purpose I/O (GPIO) pins	48	87	87	87	87
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	196 MAPBGA	256 MAPBGA			

1.1 Ordering information

Table 2. Orderable part numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF54410CMF250	MCF54410 Microprocessor	196 MAPBGA	250 MHz	–40 to +85°C
MCF54415CMJ250	MCF54415 Microprocessor	256 MAPBGA		
MCF54416CMJ250	MCF54416 Microprocessor			
MCF54417CMJ250	MCF54417 Microprocessor			
MCF54418CMJ250	MCF54418 Microprocessor			

2 Hardware design considerations

2.1 Power filtering

To further enhance noise isolation, an external filter is strongly recommended for the analog V_{DD} pins (VDDA_PLL and VDDA_DAC_ADC). The filter shown in Figure 1 should be connected between the board 3.3 V (nominal) supply and the analog pins. The resistor and capacitors should be placed as close to the dedicated analog V_{DD} pin as possible. The 10 Ω resistor in the given filter is required.

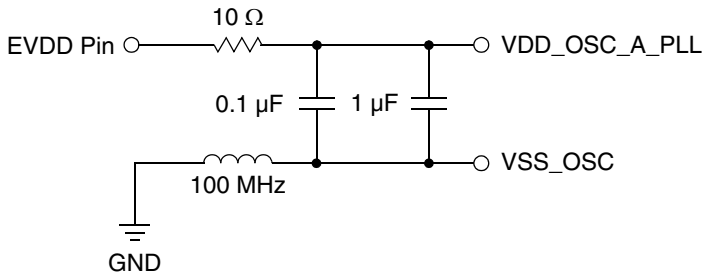


Figure 1. Oscillator/PLL/DAC power filter

Figure 2 shows an example for isolating the ADC power supply from the I/O supply (EVDD) and ground. Note that in this power supply the 10 Ω resistor is replaced by a 0 Ω resistor. This will reduce the IR drop into the ADC, limiting additional gain error.

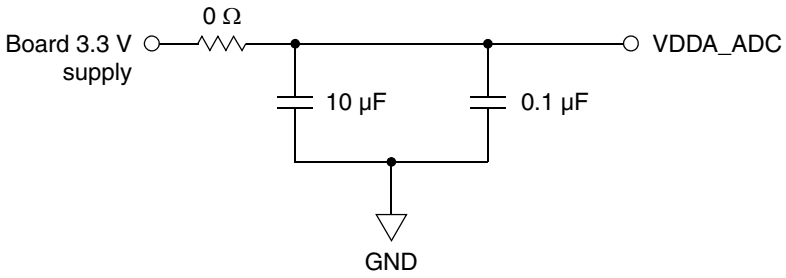


Figure 2. ADC power filter

Figure 3 shows an example for bypassing the internal core digital power supply for the MPU. This bypass should be applied to as many IVDD signals as routing allows. Each one should be placed as close to the ball as possible.

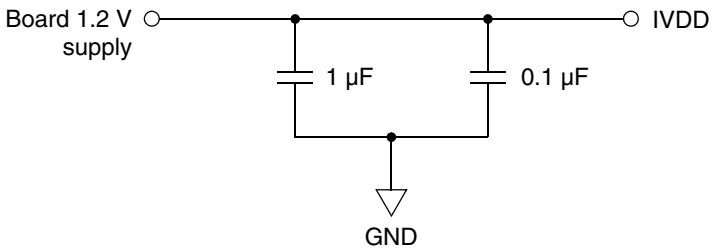


Figure 3. IVDD power filter

Figure 4 shows an example for bypassing the external pad ring digital power supply for the MPU. This bypass should be applied to as many EVDD signals as routing allows. Each one should be placed as close to the ball as possible.

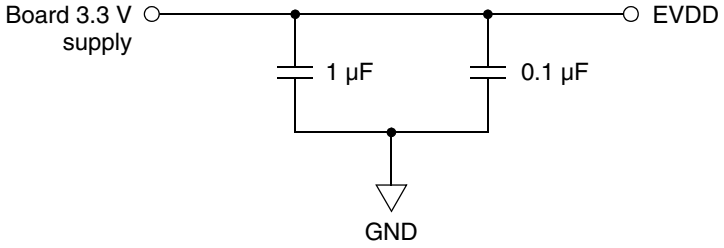


Figure 4. EVDD power filter

Figure 5 shows an example for bypassing the FlexBus power supply for the MPU. This bypass should be applied to as many FB_VDD signals as routing allows. Each one should be placed as close to the ball as possible.

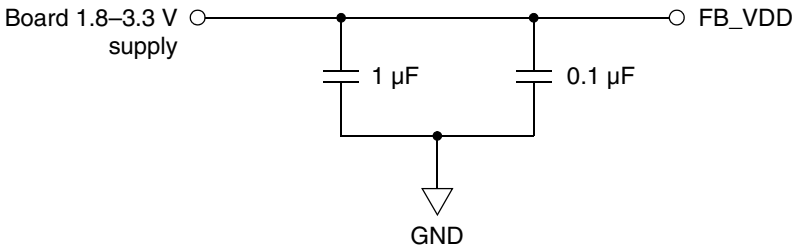
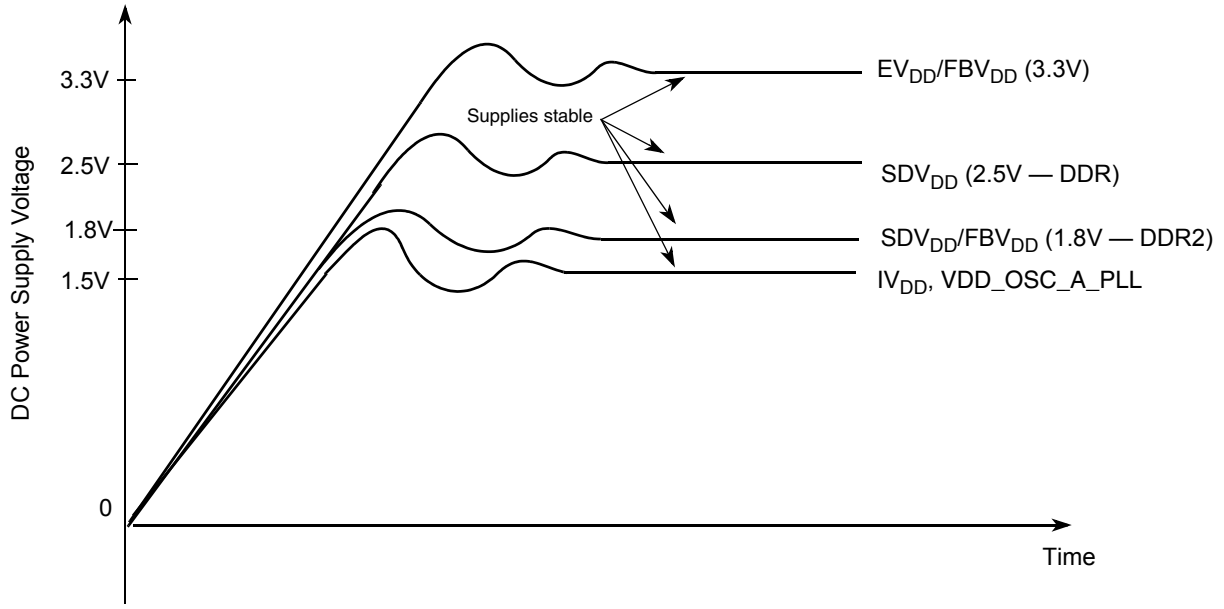


Figure 5. FB_VDD power filter

2.2 Supply voltage sequencing

Figure 6 shows requirements in the sequencing of the I/O V_{DD} (EV_{DD}), FlexBus V_{DD} (FBV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (VDD_OSC_A_PLL), and internal logic/core V_{DD} (IV_{DD}).



Notes:
1. Input voltage must not be greater than the supply voltage (EV_{DD}, FBV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
2. Use 25 V/millisecond or slower rise time for all supplies.

Figure 6. Supply voltage sequencing and separation cautions

The relationships between FBV_{DD}, SDV_{DD} and EV_{DD} are non-critical during power-up and power-down sequences. FBV_{DD} (1.8 – 3.3V), SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

NOTE

All I/O VDD pins must be powered on when the device is functioning, except when in standby mode.

In standby mode, all I/O VDD pins, except VSTBY_RTC (battery), can be switched off.

2.2.1 Power-up sequence

If EV_{DD}/FBV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/FBV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/FBV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, FBV_{DD}, or SDV_{DD} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 25 V/millisecond to avoid turning on the internal ESD protection clamp diodes.

2.2.2 Power-down sequence

If IV_{DD}/PV_{DD} are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD}, FBV_{DD}, or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, FBV_{DD}, or SDV_{DD} going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PV_{DD} to 0 V.
2. Drop EV_{DD}/FBV_{DD}/SDV_{DD} supplies.

2.3 Power consumption specifications

Table 3. Estimated power consumption specifications

Characteristic	Symbol	Typical	Unit
Core operating supply current (nominal 1.2 V)[1]	IVDD		
Run mode		127	mA
Wait mode		33	
Doze mode		32	
Stop00 mode		9.3	
Stop01 mode		9.2	
Stop02 mode		3.6	
Stop03 mode		3.4	
FlexBus operating supply current	FBVDD		
Run mode (application dependent)		80	mA
Wait mode		49	
Doze mode		42	
Stop00 mode		40	
Stop01, Stop02, Stop03 mode		28	
SDRAM operating supply current (DDR2 at 1.8 V)	SDVDD		
Isys(DQ) [×8, 2×DQS]		3	mA
Isys(WR) [×8, 2×DQS]		15	
Isys(RD) [×8, 2×DQS]		15	
SDRAM input reference current	SDVREF		
Isys(REF)		1.3	
SDRAM termination current	SDVTT		
Isys(termRD)		41	
Total SDIDD MPU side[2]		75	
Oscillator/PLL operating supply current (nominal 3.3 V)	VDD_OSC_A_PLL		
Run, Wait, Doze, Stop00, Stop01 mode		10	mA
Stop02 mode		6	
Stop03 mode		1	

Table 3. Estimated power consumption specifications (continued)

Characteristic	Symbol	Typical	Unit
External I/O pad operating supply current (nominal 3.3 V)	EVDD	—[3]	mA
USB operating supply current (nominal 3.3 V)	VDD_USBO, VDD_USBH	30	mA
ADC operating supply current (nominal 3.3 V) Speed mode 00 Speed mode 01	VDDA_ADC	 14 22	mA
DAC operating supply current (nominal 3.3 V)	VDDA_DAC_ADC	11	mA
RTC standby supply current ISTBY	VSTBY_RTC	17	µA

1 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

2 DDR2 interface power is estimated from the Micron DDR2 data sheet. The numbers given in this table do not include the actual power consumption of the memory itself. The current drawn by the memory needs to be added to the values in this table and may be several hundred mA.

3 EVDD values depend on the application, with the restrictions that any single pin cannot exceed 25 mA and that the total power does not exceed the thermal characteristics.

3 Pin assignments and reset states

3.1 Signal multiplexing

The following table lists all the MCF5441*x* pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to the following sections for package diagrams. For a more detailed discussion of the MCF5441*x* signals, consult the *MCF5441x Reference Manual* (MCF54418RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_AD23), while designations for multiple signals within a group use brackets (i.e., FB_AD[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO default to their GPIO functionality. See the following table for a list of the exceptions.

Table 4. Special-case default signal functionality

Pin	Default signal
FB_CLK, FB_OE, FB_R/W, FB_BE/BWE[1:0], FB_CS[5:4]	FB_CLK, FB_OE, FB_R/W, FB_BE/BWE[1:0], FB_CS[5:4]
FB_ALE	FB_ALE or FB_TS (depending on RCON[3])
FB_BE/BWE3	Boot from NFC, NF_ALE. Otherwise, FB_BE/BWE3.
FB_BE/BWE2	Boot from NFC, NF_CLE. Otherwise, FB_BE/BWE2.
FB_CS1	Boot from NFC, NFC_CE. Otherwise, GPIO.
FB_CS0	Boot from FlexBus, FB_CS0. Otherwise, GPIO.
FB_TA	Boot from NFC, NFC_R/B. Otherwise, FB_TA.
ALLPST, PST[3:0], DDATA[3:0]	ALLPST, PST[3:0], DDATA[3:0]

NOTE

While most modules and functionalities between the 196 and 256 MAPBGA package are the same, the following modules have been removed from 196 MAPBGA for pin space:

UART2, UART6, UART9, PWM, SSI1, SIM1, USB HOST, IRQ6, IRQ3, IRQ2, FLEXCAN1, I2C1, ADC, DAC.

Other modifications to the 196 MAPBGA package are:

- SDRAMC — One address line, SD_A14, is removed.
- SDHC — Number of data lines for eSDHC have been reduced to 4 instead of 8.
- MAC — Only MAC0_RMII mode is implemented.

Table 5. MCF5441*x* Signal information and muxing

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
Reset									
RESET	—	—	—	U	I	EVDD	ssr	K14	K15
RSTOUT	—	—	—	—	O	EVDD	msr	P12	L16
Clock									
EXTAL/ RMII_REF_CLK	—	—	—	—	I[4]	EVDD	ae	G14	G16

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
XTAL	—	—	—	—	O	EVDD	ae	H14	H16
Mode selection									
BOOTMOD[1:0]	—	—	—	—	I	EVDD	msr	G5,H5	K5, L5
FlexBus									
FB_AD[31:24]/ NFC_IO[15:8][5]	—	—	—	—	I/O	FBVDD	fsr	A10, A9, B9, C9, A8, B8, C8, A7	B9, C8, A9, B8, D8, A8, D7, B7
FB_AD[23:16]/ NFC_IO[7:0][5]	—	—	—	—	I/O	FBVDD	fsr	B7, C7, C6, B6, A6, A5, B5, A4	C7, A7, D6, A6, B6, D5, C6, A5
FB_AD[15:10]	—	—	—	—[6]	I/O	FBVDD	fsr	C5, A3, B4, C4, B3, A2	B5, A4, A3, D4, B4, C5
FB_AD[9:8]	—	—	—	U[7]	I/O	FBVDD	fsr	B2, C3	C4, B3
FB_AD[7:0]	—	—	—	—	I/O	FBVDD	fsr	D4, B1, C2, D3, C1, D2, E3, D1	C3, E4, D3, E3, A2, B2, C2, F3
FB_ALE	PA7	$\overline{\text{FB\_TS}}$	—	—	O	FBVDD	fsr	E2	D2
$\overline{\text{FB\_OE}}$/ $\overline{\text{NFC\_RE}}$	PA6	$\overline{\text{FB\_TBST}}$/ $\overline{\text{NFC\_RE}}$	—	—	O	FBVDD	fsr	H1	F1
FB_R/$\overline{\text{W}}$/ $\overline{\text{NFC\_WE}}$	PA5	—	—	—	O	FBVDD	fsr	H2	G2
$\overline{\text{FB\_TA}}$	PA4	—	NFC_R/$\overline{\text{B}}$	U[8]	O	FBVDD	fsr	H3	H3
$\overline{\text{FB\_BE/BWE3}}$	PA3	$\overline{\text{FB\_CS3}}$	FB_A1/ NFC_ALE[9]	—	O	FBVDD	fsr	F3	C1
$\overline{\text{FB\_BE/BWE2}}$	PA2	$\overline{\text{FB\_CS2}}$	FB_A0/ NFC_CLE[10]	—	O	FBVDD	fsr	E1	E2
$\overline{\text{FB\_BE/BWE}}$[1:0]	PA[1:0]	FB_TSIZ[1:0]	—	—	O	FBVDD	fsr	F2, F1	D1, F4
FB_CLK	PB7	—	—	—	O	FBVDD	fsr	G1	G1
$\overline{\text{FB\_CS5}}$	PB6	$\overline{\text{DACK1}}$	—	—	O	FBVDD	fsr	—	F2
$\overline{\text{FB\_CS4}}$	PB5	$\overline{\text{DREQ1}}$	—	—	O	FBVDD	fsr	—	B1
$\overline{\text{FB\_CS1}}$	PB4	—	$\overline{\text{NFC\_CE}}$	—	O	FBVDD	fsr	G3	E1
$\overline{\text{FB\_CS0}}$	PB3	—	—	—	O	FBVDD	fsr	G2	G3
I²C 0									
I2C0_SCL	PB2	UART8_TXD	CAN0_TX	—	I/O	EVDD	ssr	H12	G15
I2C0_SDA	PB1	UART8_RXD	CAN0_RX	—	I/O	EVDD	ssr	G12	G14

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
FlexCAN 1									
CAN1_TX	PB0	UART9_TXD	I2C1_SCL	—	I/O	EVDD	ssr	—	D14
CAN1_RX	PC7	UART9_RXD	I2C1_SDA	—	I/O	EVDD	ssr	—	D15
SDRAM controller									
SD_A14	—	—	—	—	O	SDVDD	st_dec ap	—	P6
SD_A[13:0]	—	—	—	—	O	SDVDD	st_dec ap	P3, M1, M3, L2, L1, N4, M2, P2, L3, L4, N1, N2, K1, N3	R4, R1, R3, N4, P3, T4, R2, T2, N3, P5, P4, N5, P2, T3
SD_BA[2:0]	—	—	—	—	O	SDVDD	st_dec ap	M6, J4, P4	P7, N6, R5
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	st_dec ap	K4	N8
SD_CKE	—	—	—	—	O	SDVDD	st_dec ap	N6	R7
SD_CLK	—	—	—	—	O	SDVDD	st_ck	P6	T5
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	st_ck	P7	T6
$\overline{\text{SD\_CS}}$	—	—	—	—	O	SDVDD	st_dec ap	M5	N7
SD_D[7:0]	—	—	—	—	I/O	SDVDD	st_odt	P11, M10, N10, M9, P10, M8, N8, M7	T12, R11, T11, R10, N9, T10, P9, R9
SD_DM	—	—	—	—	O	SDVDD	st_odt	N7	T7
SD_DQS	—	—	—	—	I/O	SDVDD	st_dqs	P8	T8
$\overline{\text{SD\_DQS}}$	—	—	—	—	I/O	SDVDD	st_dqs	P9	T9
SD_ODT	—	—	—	—	O	SDVDD	st_dec ap	P5	P8
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	st_dec ap	M4	R6
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	st_dec ap	N5	R8
SD_VREF	—	—	—	—	—	SDVDD	st_vref	N9	P10
SD_VTT	—	—	—	—	—	SDVDD	st_vtt	L8	N10

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
External interrupts port									
$\overline{\text{IRQ7}}$	PC6	—	—	—	I	EVDD	ssr	G10	F12
$\overline{\text{IRQ6}}$	PC5	—	USB_CLKIN[11]	—	I	EVDD	ssr	—	N1
$\overline{\text{IRQ4}}$	PC4	$\overline{\text{DREQ0}}$	—	—	I	EVDD	ssr	E11	F14
$\overline{\text{IRQ3}}$	PC3	DSPI0_PCS3	USBH_VBUS_EN	—	I	EVDD	ssr	—	M1
$\overline{\text{IRQ2}}$	PC2	DSPI0_PCS2	USBH_VBUS_OC	—[12]	I	EVDD	ssr	—	M2
$\overline{\text{IRQ1}}$	PC1	—	—	—	I	EVDD	ssr	E13	F13
USB On-the-Go									
USBO_DM	—	—	—	—	I/O	VDD_USB0	ae	B13	A14
USBO_DP	—	—	—	—	I/O	VDD_USB0	ae	A13	B14
USB host									
USBH_DM	—	—	—	—	I/O	VDD_USBH	ae	—	A15
USBH_DP	—	—	—	—	I/O	VDD_USBH	ae	—	B15
ADC									
ADC_IN7/ DAC1_OUT	—	—	—	—	I	VDDA_DAC_ADC	ae	—	K3
ADC_IN[6:4]	—	—	—	—	I	VDDA_ADC	ae	—	H2, J3, G4
ADC_IN3/ DAC0_OUT	—	—	—	—	I	VDDA_DAC_ADC	ae	—	K4
ADC_IN[2:0]	—	—	—	—	I	VDDA_ADC	ae	—	J2, J1, H1
Real time clock									
RTC_EXTAL	—	—	—	—	I[4]	VSTBY	ae	B14	B16
RTC_XTAL	—	—	—	—	O	VSTBY	ae	C14	C16
DSPI0/SBF[13]									
DSPI0_PCS1/ $\overline{\text{SBF\_CS}}$	PC0	—	—	—	I/O	EVDD	msr	K3	L1

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
DSPI0_PCS0/$\overline{SS}$	PD7	I2C3_SDA	SDHC_DAT3	—	I/O	EVDD	msr	J1	K2
DSPI0_SCK/ SBF_CK	PD6	I2C3_SCL	SDHC_CLK	—	I/O	EVDD	msr	J3	L2
DSPI0_SIN/ SBF_DI	PD5	UART3_RXD	SDHC_CMD	U[14]	I	EVDD	msr	K2	L3
DSPI0_SOUT/ SBF_DO	PD4	UART3_TXD	SDHC_DAT0	—	O	EVDD	msr	J2	K1
One wire									
OW_DAT	RGPIO0/PD3	$\overline{DACK0}$	—	—	I/O	EVDD	ssr	M11	N11
DMA timers									
T3IN/PWM_EXTA3	RGPIO1/PD2	T3OUT	USBO_VBUS_EN/ ULPI_DIR[15]	—	I	EVDD	msr	G13	G13
T2IN/PWM_EXTA2	RGPIO2/PD1	T2OUT	SDHC_DAT2	—	I	EVDD	msr	J12	H14
T1IN/PWM_EXTA1	RGPIO3/PD0	T1OUT	SDHC_DAT1	—	I	EVDD	msr	H13	H13
T0IN/PWM_EXTA0	RGPIO4/PE7	T0OUT	USBO_VBUS_OC/ ULPI_NXT[16]	—[17]	I	EVDD	msr	J13	H15
UART 2									
$\overline{UART2\_CTS}$	RGPIO14/PE6	UART6_TXD	SSI1_BCLK	—	I	EVDD	msr	—	M4
$\overline{UART2\_RTS}$	RGPIO15/PE5	UART6_RXD	SSI1_FS	—	O	EVDD	msr	—	M3
UART2_RXD	PE4	PWM_A3	SSI1_RXD	—	I	EVDD	msr	—	P1
UART2_TXD	PE3	PWM_B3	SSI1_TXD	—	I/O[18]	EVDD	msr	—	N2
UART 1									
$\overline{UART1\_CTS}$	RGPIO7/PE2	UART5_TXD	DSPI3_SCK	—	I	EVDD	msr	D12	C10
$\overline{UART1\_RTS}$	RGPIO8/PE1	UART5_RXD	DSPI3_PCS0	—	O	EVDD	msr	D11	D10
UART1_RXD	PE0	I2C5_SDA	DSPI3_SIN	—	I	EVDD	msr	B10	C9
UART1_TXD	PF7	I2C5_SCL	DSPI3_SOUT	—	I/O[18]	EVDD	msr	C10	D9
UART 0									
$\overline{UART0\_CTS}$	RGPIO5/PF6	UART4_TXD	DSPI2_SCK	—	I	EVDD	msr	E12	E13
$\overline{UART0\_RTS}$	RGPIO6/PF5	UART4_RXD	DSPI2_PCS0	—	O	EVDD	msr	C12	B11
UART0_RXD	PF4	I2C4_SDA	DSPI2_SIN	—	I	EVDD	msr	C11	B10
UART0_TXD	PF3	I2C4_SCL	DSPI2_SOUT	—	I/O[18]	EVDD	msr	B11	D11

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
Enhanced secure digital host controller									
SDHC_DAT3	PF2	PWM_A1	DSPI1_PCS0	—	I/O	EVDD	msr	—	B13
SDHC_DAT2	PF1	PWM_B1	DSPI1_PCS2	—	I/O	EVDD	msr	—	E14
SDHC_DAT1	PF0	PWM_A2	DSPI1_PCS1	—	I/O	EVDD	msr	—	D12
SDHC_DAT0	PG7	PWM_B2	DSPI1_SOUT	—	I/O	EVDD	msr	—	B12
SDHC_CMD	PG6	PWM_B0	DSPI1_SIN	—	I/O	EVDD	msr	—	C11
SDHC_CLK	PG5	PWM_A0	DSPI1_SCK	—	O	EVDD	msr	—	A10
Smart card interface 0									
SIM0_DATA	RGPIO13/PG4	PWM_FAULT2	SDHC_DAT7	—	I/O	EVDD	msr	—	E12
SIM0_VEN	RGPIO12/PG3	PWM_FAULT0	—	—	O	EVDD	msr	—	D13
SIM0_RST	RGPIO11/PG2	PWM_FORCE	SDHC_DAT6	—	O	EVDD	msr	—	C15
SIM0_PD	RGPIO10/PG1	PWM_SYNC	SDHC_DAT5	—	I	EVDD	msr	—	C14
SIM0_CLK	RGPIO9/PG0	PWM_FAULT1	SDHC_DAT4	—	O	EVDD	msr	—	A11
Synchronous serial interface 0[19]									
SSI0_RXD	PH7	I2C2_SDA	SIM1_VEN	—	I	EVDD	msr	B12	C12
SSI0_TXD	PH6	I2C2_SCL	SIM1_DATA	—	O	EVDD	msr	A11	C13
SSI0_FS	PH5	UART7_TXD	SIM1_RST	—	I/O	EVDD	msr	C13	E15
SSI0_MCLK	PH4	SSI_CLKIN	SIM1_CLK	—	O	EVDD	msr	A12	A12
SSI0_BCLK	PH3	UART7_RXD	SIM1_PD	—	I/O	EVDD	msr	D13	A13
Ethernet subsystem									
MII0_MDC	PI1	RMII0_MDC[20]	—	—	O	EVDD	fsr	N14	P16
MII0_MDIO	PI0	RMII0_MDIO[20]	—	—	I/O	EVDD	fsr	M14	N16
MII0_RXDV	PJ7	RMII0_CRS_DV[20]	—	—	I	EVDD	fsr	M13	P14
MII0_RXD[1:0]	PJ[6:5]	RMII0_RXD[1:0][20]	—	—	I	EVDD	fsr	P13, N13	R15, T15
MII0_RXER	PJ4	RMII0_RXER[20]	—	—	I	EVDD	fsr	M12	N14
MII0_TXD[1:0]	PJ[3:2]	RMII0_TXD[1:0][20]	—	—	O	EVDD	fsr	L12, L11	R13, P13
MII0_TXEN	PJ1	RMII0_TXEN[20]	—	D[21]	O	EVDD	fsr	N12	P12
MII0_COL	PJ0	RMII1_MDC	ULPI_STP	—	I	EVDD	fsr	—	R12
MII0_TXER	PK7	RMII1_MDIO	ULPI_DATA4	—	O	EVDD	fsr	—	R14
MII0_CRS	PK6	RMII1_CRS_DV	ULPI_DATA5	—	I	EVDD	fsr	—	P11
MII0_RXD[3:2]	PK[5:4]	RMII1_RXD[1:0]	ULPI_DATA[1:0]	—	I	EVDD	fsr	—	P15, N13

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
MII0_RXCLK	PK3	RMII1_RXER	ULPI_DATA6	—	I	EVDD	fsr	—	M14
MII0_TXD[3:2]	PK[2:1]	RMII1_TXD[1:0]	ULPI_DATA[3:2]	—	O	EVDD	fsr	—	T13, N12
MII0_TXCLK	PK0	RMII1_TXEN	ULPI_DATA7	D[21]	I	EVDD	fsr	—	T14
BDM/JTAG									
ALLPST[22]	PH2	—	—	—	O	EVDD	fsr	K12	—
DDATA[3:2]	PH[1:0]	—	—	—	O	EVDD	fsr	—	L15, M13
DDATA[1:0]	PI[7:6]	—	—	—	O	EVDD	fsr	—	M15, L14
PST[3:0]	PI[5:2]	—	—	—	O	EVDD	fsr	—	J13, J16, J15, J14
JTAG_EN	—	—	—	D	I	EVDD	msr	N11	N15
PSTCLK	—	TCLK[23]	—	—	I	EVDD	fsr	L14	M16
DSI	—	TDI[23]	—	U	I	EVDD	msr	L10	L13
DSO	—	TDO[23]	—	—	O	EVDD	msr	L13	K14
$\overline{\text{BKPT}}$	—	TMS[23]	—	U	I	EVDD	msr	K13	K16
DSCLK	—	$\overline{\text{TRST}}$[23]	—	U	I	EVDD	msr	L9	K13
Test (this signal must be grounded)									
TEST	—	—	—	D	I	EVDD	ssr	K10	R16
Power supplies									
IVDD	—	—	—	—	—	—	—	D9, D10, E9, E10, F9, F10, F12	E9–E11, F9–F11
EVDD	—	—	—	—	—	—	—	F4–F7, G6, G7, H6, H7, J5, J6	H8, J7–J10, K6–K11, L6
FB_VDD	—	—	—	—	—	—	—	D5–D7, E4–E7	E5–E7, F5, F6, G5
SD_VDD	—	—	—	—	—	—	—	K7–K9, L5–L7	M7–M12
VDD_OSC_A_PLL	—	—	—	—	—	—	vddint	F14	F15
VSS_OSC_A_PLL	—	—	—	—	—	—	vddint	F13	F16
VDD_USBO	—	—	—	—	—	—	vdde	F11	G12
VDD_USBH	—	—	—	—	—	—	vdde	—	H12
VDDA_ADC	—	—	—	—	—	—	—	—	H4

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
VSSA_ADC	—	—	—	—	—	—	vssint	—	H5
VDDA_DAC_ADC	—	—	—	—	—	—	vddint	—	J4
VSSA_DAC_ADC	—	—	—	—	—	—	vssint	—	J5
VSTBY[24]	—	—	—	—	—	—	vddint	E14	E16
VSS	—	—	—	—	—	—	—	A1, A14, D8, D14, E8, F8, G4, G8, G9, G11, H4, H8–11, J7–11, J14, K5, K6, K11, P1, P14	A1, A16, D16, E8, F7, F8, G6–G11, H6, H7, H9–H11, J6, J11, J12, K12, L4, L7–L12, M5, M6, T1, T16

1 All pins available with GPIO contain a configurable pull-up/down. This column indicates the pull devices that are enabled automatically at reset. Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 For details on the available slew rates of the various pad types see section "Output Pad Loading and Slew Rate" of the *MCF5441x Data Sheet* or section "Slew Rate Control Registers (SRCR_x)" in chapter "Pin-Multiplexing and Control" of the *MCF5441x Reference Manual*.

4 Enabled as input only in oscillator bypass mode (internal crystal oscillator is disabled).

5 These pins are time-division multiplexed between the FlexBus and NFC. An arbitration mechanism determines which module drives these pins at any point in time.

6 An internal pulldown circuit is enabled during system reset for FB_AD[10].

7 An internal pullup circuit is enabled when the system is in reset state.

8 Configurable pull that is enabled and pulled up after reset.

9 When configured for FB_A1, this pin is time-division multiplexed between the FlexBus and NFC. An arbitration mechanism determines which module drives the pin at any point in time. When not configured as FB_A1, NFC_ALE cannot be used.

10 When configured for FB_A0, this pin is time-division multiplexed between the FlexBus and NFC. An arbitration mechanism determines which module drives the pin at any point in time. When not configured as FB_A0, NFC_CLE cannot be used.

11 Since USB_CLKIN is a clock signal, it must be dedicated to the USB system. Do not implement this pin as dual-use.

12 When Alternate 2 is selected, then internal pullup/pulldown control will come from the MISCCR[3] register of CIM.

13 When booting from serial boot flash, the SBF function is enabled automatically. After the SBF function completes its reset sequence, the signals are returned to GPIO functionality.

14 Automatic pull-up when SBF controls the pin during reset only. Configurable pull when UART, DSPI, or SDHC control the pin.

15 If ULPI is enabled, ULPI_DIR is available as the Alternate 2 function. If ULPI is disabled, USBO_VBUS_EN is available.

16 If ULPI is enabled, ULPI_NXT is available as the Alternate 2 function. If ULPI is disabled, USBO_VBUS_OC is available.

17 When Alternate 2 is selected, then internal pullup/pulldown control will come from the MISCCR[2] register of CIM.

18 UART*x*_TXD pad can act as RXD(input) pad when UART One Wire mode is enabled.

19 The SIM1 signals are available with 256 MAPBGA but are not available with 196 MAPBGA.

20 These RMII functions are selected by the mode chosen by the MAC-NET, not by the pin-multiplexing and control (GPIO) module.

[21] Configurable pull that is enabled and pulled down after reset.

[22] The ALLPST signal is available only on the 196 MAPBGA package and allows limited debug trace functionality compared to the 256 MAPBGA package.

[23] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

[24] VSTBY is for optional standby lithium battery. If not used, connect to EVDD.

3.2 Pinout—196 MAPBGA

The pinout for the MCF54410 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	GND	FB_AD10	FB_AD14	FB_AD16	FB_AD18	FB_AD19	FB_AD24	FB_AD27	FB_AD30	FB_AD31	SSI0_TXD	SSI0_MCLK	USB_DPLS	GND	A
B	FB_AD6	FB_AD9	FB_AD11	FB_AD13	FB_AD17	FB_AD20	FB_AD23	FB_AD26	FB_AD29	U1_RXD	U0_TXD	SSI0_RXD	USB_DMNS	RTC_EXTAL	B
C	FB_AD3	FB_AD5	FB_AD8	FB_AD12	FB_AD15	FB_AD21	FB_AD22	FB_AD25	FB_AD28	U1_TXD	U0_RXD	U0RTS_B	SSI0_FS	RTC_XTAL	C
D	FB_AD0	FB_AD2	FB_AD4	FB_AD7	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	U1RTS_B	U1CTS_B	SSI0_BCLK	GND	D
E	FB_BE2_B	FB_ALE	FB_AD1	FBVDD	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	IRQ4_B	U0CTS_B	IRQ1_B	VSTBY	E
F	FB_BE0_B	FB_BE1_B	FB_BE3_B	EVDD	EVDD	EVDD	EVDD	GND	CVDD	CVDD	VDD_USBO	CVDD	VSS_OSC_A_PLL	VDD_OSC_A_PLL	F
G	FB_CLK	FB_CS0_B	FB_CS1_B	GND	BOOTMOD1	EVDD	EVDD	GND	GND	IRQ7_B	GND	I2C0_SDA	T3IN	EXTAL	G
H	FB_OE_B	FB_RW_B	FB_TA_B	GND	BOOTMOD0	EVDD	EVDD	GND	GND	GND	GND	I2C0_SCL	T1IN	XTAL	H
J	DSPI0_PCS0	DSPI0_SOUT	DSPI0_SCK	SD_BA1	EVDD	EVDD	GND	GND	GND	GND	GND	T2IN	T0IN	GND	J
K	SD_A1	DSPI0_SIN	DSPI0_PCS1	SD_CAS_B	GND	GND	SDVDD	SDVDD	SDVDD	TEST	GND	ALLPST	TMS	RSTIN_B	K
L	SD_A9	SD_A10	SD_A5	SD_A4	SDVDD	SDVDD	SDVDD	SD_VTT	TRST_B	TDI	RM110_TXD0	RM110_TXD1	TDO	TCLK	L
M	SD_A12	SD_A7	SD_A11	SD_RAS_B	SD_CS_B	SD_BA2	SD_D0	SD_D2	SD_D4	SD_D6	OWIO	RMII0_RXER	RMII0_CRS_DV	RMII0_MDIO	M
N	SD_A3	SD_A2	SD_A0	SD_A8	SD_WE_B	SD_CKE	SD_DQM	SD_D1	SD_VREF	SD_D5	JTAG_EN	RMII0_TXEN	RMII0_RXD0	RMII0_MDC	N
P	GND	SD_A6	SD_A13	SD_BA0	SD_ODT	SD_CLK	SD_CLK_B	SD_DQS	SD_DQS_B	SD_D3	SD_D7	RSTOUT_B	RMII0_RXD1	GND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 7. MCF54410 Pinout (196 MAPBGA)

3.3 Pinout—256 MAPBGA

The pinout for the MCF54415, MCF54416, MCF54417, and MCF54418 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FB_AD3	FB_AD13	FB_AD14	FB_AD16	FB_AD20	FB_AD22	FB_AD26	FB_AD29	SDHC_CLK	SIM0_CLK	SSI0_MCLK	SSI0_BCLK	USBO_DM	USBH_DM	VSS	A
B	FB_CS4	FB_AD2	FB_AD8	FB_AD11	FB_AD15	FB_AD19	FB_AD24	FB_AD28	FB_AD31	UART0_RXD	UART0_RTS	SDHC_DAT0	SDHC_DAT3	USBO_DP	USBH_DP	RTC_EXTAL	B
C	FB_BE/BWE3	FB_AD1	FB_AD7	FB_AD9	FB_AD10	FB_AD17	FB_AD23	FB_AD30	UART1_RXD	UART1_CTS	SDHC_CMD	SSI0_RXD	SSI0_TXD	SIM0_PD	SIM0_RST	RTC_XTAL	C
D	FB_BE/BWE1	FB_ALE	FB_AD5	FB_AD12	FB_AD18	FB_AD21	FB_AD25	FB_AD27	UART1_TXD	UART1_RTS	UART0_TXD	SDHC_DAT1	SIM0_VEN	CAN1_TX	CAN1_RX	VSS	D
E	FB_CS1	FB_BE/BWE2	FB_AD4	FB_AD6	FB_VDD	FB_VDD	FB_VDD	VSS	IVDD	IVDD	IVDD	SIM0_XMT	UART0_CTS	SDHC_DAT2	SSI0_FS	VSTBY_RTC	E
F	FB_OE	FB_CS5	FB_AD0	FB_BE/BWE0	FB_VDD	FB_VDD	VSS	VSS	IVDD	IVDD	IVDD	IRQ7	IRQ1	IRQ4	VDD_OSC_A_PLL	VSS_OSC_A_PLL	F
G	FB_CLK	FB_R/W	FB_CS0	ADC_IN4	FB_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD_USBO	T3IN	I2C0_SDA	I2C0_SCL	EXTAL	G
H	ADC_IN0	ADC_IN6	FB_TA	AVDD_ADC	AVSS_ADC	VSS	VSS	EVDD	VSS	VSS	VSS	VDD_USBH	T1IN	T2IN	T0IN	XTAL	H
J	ADC_IN1	ADC_IN2	ADC_IN5	VDDA_DAC_ADC	VSSA_DAC_ADC	VSS	EVDD	EVDD	EVDD	EVDD	VSS	VSS	PST3	PST0	PST1	PST2	J
K	DSPI0_SOUT	DSPI0_PCS0	ADC_IN7	ADC_IN3	BOOT MOD1	EVDD	EVDD	EVDD	EVDD	EVDD	EVDD	VSS	TRST	TDO	RESET	TMS	K
L	DSPI0_PCS1	DSPI0_SCK	DSPI0_SIN	VSS	BOOT MOD0	EVDD	VSS	VSS	VSS	VSS	VSS	VSS	TDI	DDATA0	DDATA3	RST_OUT	L
M	IRQ3	IRQ2	UART2_RTS	UART2_CTS	VSS	VSS	SD_VDD	SD_VDD	SD_VDD	SD_VDD	SD_VDD	SD_VDD	DDATA2	MII0_RXCLK	DDATA1	TCLK	M
N	IRQ6	UART2_TXD	SD_A5	SD_A10	SD_A2	SD_BA1	SD_CS	SD_CAS	SD_D3	SD_VTT	OW_IO	MII0_TXD2	MII0_RXD2	MII0_RXER	JTAG_EN	MII0_MDIO	N
P	UART2_RXD	SD_A1	SD_A9	SD_A3	SD_A4	SD_A14	SD_BA2	SD_ODT	SD_D1	SD_VREF	MII0_CRS	MII0_TXEN	MII0_TXD0	MII0_RXDV	MII0_RXD3	MII0_MDC	P
R	SD_A12	SD_A7	SD_A11	SD_A13	SD_BA0	SD_RAS	SD_CKE	SD_WE	SD_D0	SD_D4	SD_D6	MII0_COL	MII0_TXD1	MII0_TXER	MII0_RXD1	TEST	R
T	VSS	SD_A6	SD_A0	SD_A8	SD_CLK	SD_CLK	SD_DM	SD_DQS	SD_DQS	SD_D2	SD_D5	SD_D7	MII0_TXD3	MII0_TXCLK	MII0_RXD0	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 8. MCF54415, MCF54416, MCF54417, and MCF54418 Pinout (256 MAPBGA)

4 Electrical characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5441*x* microprocessor. This section contains detailed information on AC/DC electrical characteristics and AC timing specifications.

NOTE

The specifications for this device in any other document are superseded by the specifications in this document.

4.1 Absolute maximum ratings

Table 6. Absolute maximum ratings[1, 2]

Rating	Symbol	Pin name	Value	Units
External I/O pad supply voltage	EV_{DD}	EVDD	–0.3 to +4.0	V
Internal logic supply voltage	IV_{DD}	IVDD	–0.5 to +2.0	V
FlexBus I/O pad supply voltage	FBV_{DD}	FB_VDD	–0.3 to +4.0	V
SDRAM I/O pad supply voltage	SDV_{DD}	SD_VDD	–0.3 to +4.0	V
PLL supply voltage	PV_{DD}	VDD_OSC_A_PLL	–0.3 to +4.0	V
USB OTG supply voltage	$USBV_{DD}$	VDD_USBO	–0.3 to +4.0	V
USB host supply voltage	$USBV_{DD}$	VDD_USBH	–0.3 to +4.0	V
ADC supply voltage	AV_{DD}	VDDA_ADC	–0.3 to +4.0	V
DAC and ADC supply voltage	—	VDDA_DAC_ADC	–0.3 to +4.0	V
RTC standby supply voltage	$RTCV_{STBY}$	VSTBY_RTC	–0.3 to +4.0	V
Digital input voltage[3]	V_{IN}	—	–0.3 to +3.6	V
Instantaneous maximum current Single pin limit (applies to all pins) [3, 4, 5]	I_{DD}	—	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	—	–40 to +85	°C
Storage temperature range	T_{stg}	—	–55 to +150	°C

1 Functional operating conditions are given in Table 11. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Immunity to static and electrical fields is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD} .

5 Power supply must maintain regulation within operating EV_{DD}, FBV_{DD}, and SDV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$, FBV_{DD}, or SDV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD}, FBV_{DD}, or SDV_{DD} and could result in external power supply going out of regulation. Ensure the external EV_{DD}, FBV_{DD}, or SDV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MPU is not consuming power (for example, no clock).

4.2 Thermal characteristics

Table 7. Thermal characteristics

Characteristic		Symbol	196 MAPBGA	256 MAPBGA	Unit
Junction to ambient, natural convection[1]	Single layer board (1s)[2]	θ_{JA}	58	—	
	Four layer board (2s2p)[2,3]	θ_{JA}	35	32	°C/W
Junction to ambient (@200 ft/min)[1, 3]	Single layer board (1s)	θ_{JMA}	48	—	
	Four layer board (2s2p)	θ_{JMA}	32	29	°C/W
Junction to board[4]		θ_{JB}	22	22	°C/W
Junction to case[5]		θ_{JC}	14	12	°C/W
Junction to top of package, natural convection[1, 6]		Ψ_{jt}	3	2	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = I_{DD} × IV_{DD}, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

4.3 ESD protection

Table 8. ESD protection characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with JESD22 Stress Test Qualification.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable specification at room temperature followed by hot temperature, unless specified otherwise in the device specifications provided in this document.

4.4 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output, and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 9. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.5 DC electrical specifications

Table 10. Power supply specifications

Characteristic	Symbol	Pin Name	Min	Max	Units
Internal logic supply voltage, nominal 1.2 V	IV_{DD}	IVDD	1.14	1.32	V
FlexBus supply voltage Nominal 1.8–3.3 V	FBV_{DD}	FB_VDD	1.71	3.63	V
SDRAM supply voltage DDR2 @ 1.8 V	SDV_{DD}	SD_VDD	1.71	1.98	V
SDRAM input reference voltage	SDV_{REF}	SD_VREF	0.49 x SDV_{DD}	0.51 x SDV_{DD}	V
SDRAM termination supply voltage	SDV_{TT}	SD_VTT	SDV_{REF} – 0.04	SDV_{REF} + 0.04	V
PLL analog operation voltage range, nominal 3.3 V	PV_{DD}	VDD_OSC_A_PLL	3.135	3.63	V

Table 10. Power supply specifications (continued)

Characteristic	Symbol	Pin Name	Min	Max	Units
External I/O pad supply voltage, nominal 3.3 V	EV_{DD}	EVDD	3.135	3.63	V
USB supply voltage, nominal 3.3 V	$USBV_{DD}$	VDD_USBO VDD_USBH	3.135	3.63	V
ADC supply voltage	AV_{DD}	VDDA_ADC	3.135	3.63	V
DAC supply voltage	—	VDDA_DAC_ ADC	3.135	3.63	V
RTC standby supply voltage	$RTCV_{STBY}$	VSTBY_RTC	1.6	EV_{DD} – 0.2V	V

Table 11. I/O electrical specifications

Characteristic	Symbol	Min	Max	Units
CMOS input high voltage	EV_{IH}	0.65 × EV_{DD}	EV_{DD} + 0.3	V
CMOS input low voltage	EV_{IL}	V_{SS} – 0.3	0.35 × EV_{DD}	V
CMOS output high voltage I_{OH} = –2.0 mA	EV_{OH}	0.8 × EV_{DD}	—	V
CMOS output low voltage I_{OL} = 2.0 mA	EV_{OL}	—	0.2 × EV_{DD}	V
SDRAM input high voltage DDR2 @ 1.8V	SDV_{IH}	SDV_{REF} + 0.125	SDV_{DD} + 0.3	V
SDRAM input low voltage DDR2 @ 1.8V	SDV_{IL}	–0.3	SDV_{REF} – 0.125	V
SDRAM output high voltage DDR2@ 1.8V I_{OH} = –13.4 mA	SDV_{OH}	SDV_{DD} × 0.9	—	V
SDRAM output low voltage DDR2@ 1.8V I_{OH} = 13.4 mA	SDV_{OL}	—	SDV_{DD} × 0.1	V
FlexBus input high voltage @ 1.8V–3.3V	FBV_{IH}	0.51 × FBV_{DD}	FBV_{DD} + 0.3	V
FlexBus input low voltage @ 1.8V–3.3V	FBV_{IL}	V_{SS} – 0.3	0.42 × FBV_{DD}	V
FlexBus output high voltage @ 1.8V–3.3V I_{OH} = –5.0 mA for all modes	FBV_{OH}	0.8 × FBV_{DD}	—	V
FlexBus output low voltage @ 1.8V–3.3V I_{OL} = 5.0 mA for all modes	FBV_{OL}	—	0.2 × FBV_{DD}	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA

Table 11. I/O electrical specifications (continued)

Characteristic	Symbol	Min	Max	Units
Weak internal pull-up/pull-down device current[1]	I_{APU}	10	315	µA
Selectable weak internal pull-up/pull-down device current[1]	I_{APU}	25	150	µA
Input capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Output loading for CMOS pads (EV_{DD} and FBV_{DD} domains) Low drive High drive	C_L		 50 200	pF
Output loading for SDRAMC pads (SDV_{DD} domain) Low drive High drive	C_L		 5 50	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

4.6 Output pad loading and slew rate

The output pins on the MCF5441x devices have programmable slew rates. Table 12 lists the rise/fall time for pins based on the type of pad used for the signal, the value programmed into the appropriate field of the slew rate control registers, and capacitive loading. Refer to Table 5 for a list of the external signals to pad connections.

NOTE

To allow the I/O interfaces to run at their maximum frequency, set their respective slew rate select values to 11.

Table 12. Output pad slew rates

Pad type[1]	Slew rate select field value	Drive load (pF)	Rise/fall time (ns)
ssr	11	50	2.2
		200	6
	10	50	22
		200	28
	01	50	42
		200	50
	00	50	210
		200	220

Table 12. Output pad slew rates (continued)

Pad type[1]	Slew rate select field value	Drive load (pF)	Rise/fall time (ns)
msr	11	50	1.2
		200	6
	10	50	9
		200	14
	01	50	17
		200	23
	00	50	110
		200	120
fsr	11	50	1.1
		200	2.6
	10	50	2.4
		200	5
	01	50	5
		200	8
	00	50	16
		200	21

1 The ae pads are used for USB communication and are governed by usb.org specifications. They are not included in this table.

4.7 DDR pad drive strengths

The DDR pins on the MCF5441x devices have programmable drive strengths. Table 13 lists the drive strengths for pins based on the value programmed into the appropriate field of the drive strength control register. Refer to Table 5 for a list of the external signals to pad connections.

NOTE

For a single device drive, this setting should be 00 to enable Half Strength mode. High strength is intended for multiple device drives (DIMM).

Table 13. DDR pad drive strengths

Pad type	Drive strength select field value	Drive strength
st	00	Half strength 1.8V DDR2
	01	Full strength 1.8V DDR2
	10	Reserved
	11	Reserved

4.8 Oscillator and PLL electrical characteristics

Reference Figure 9 for crystal circuits.

Table 14. PLL electrical characteristics

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[1] Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 14[1] 14[1]	 50[1] 50[1]	 MHz MHz
2	Core frequency FB_CLK frequency[2] (MISCCR2[FBHALF] = 0)	f_{sys} $f_{sys/2}$	120 60	250 100	MHz MHz
3	VCO frequency	f_{vco}	240	500	MHz
4	DCC frequency[3]	f_{DCC}	300	500	MHz
5	Crystal start-up time[4, 5]	t_{cst}	—	10	ms
6	EXTAL input high voltage External and limp modes	V_{IHEXT}	EV_{IH}	EVDD	V
7	EXTAL input low voltage External and limp modes	V_{ILEXT}	0	EV_{IL}	V
8	PLL lock time [4, 6]	t_{lpll}	—	50	ms
9	Duty cycle of reference [4]	t_{dc}	–45%	+45%	%
10	Crystal capacitive load	C_L	—	From crystal spec	pF
11	Feedback resistor	R_F	10	—	MΩ
12	Series resistor	R_S	0	200	Ω
13	Discrete load capacitance for XTAL	C_{L_XTAL}	—	$2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}	—	$2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[7]	pF
15	FB_CLK period jitter, [4, 5, 7, 8,] Measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter	C_{jitter}	 — —	 10 0.1	 % $f_{sys/3}$ % $f_{sys/3}$

1 These reference value ranges are for after a PLL predivider (PREDIV), which can be programmed to 1, 2, 4, 8, or 16. The PREDIV value can be set while booting from serial flash. In parallel reset configuration, the PREDIV value is set to one. In this mode, if the input frequency results in an out of range reference frequency, boot the processor in limp mode, set the proper PREDIV and multiplier settings, and switch to PLL mode.

2 All internal registers retain data at 0 Hz.

3 Required only for DDR2 memory.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

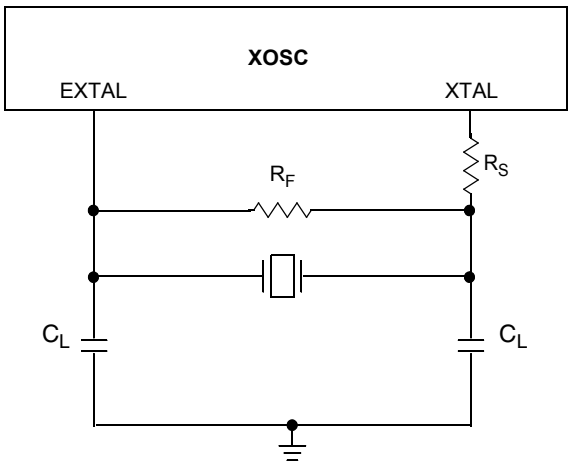


Figure 9. Typical crystal circuit

4.9 Reset timing specifications

Table 15 lists specifications for the reset timing parameters shown in Figure 10.

Table 15. Reset and configuration override timing

Num	Characteristic	Min	Max	Unit
R1[1]	$\overline{\text{RESET}}$ valid to FB_CLK (setup)	9	—	ns
R2	FB_CLK to $\overline{\text{RESET}}$ invalid (hold)	1.5	—	ns
R3	$\overline{\text{RESET}}$ valid time[2]	5	—	FB_CLK cycles
R4	FB_CLK to $\overline{\text{RSTOUT}}$ valid	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Configuration Override inputs valid	0	—	ns
R6	Configuration Override inputs valid to $\overline{\text{RSTOUT}}$ invalid (setup)	20	—	FB_CLK cycles
R7	Configuration Override inputs invalid after $\overline{\text{RSTOUT}}$ invalid (hold)	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override inputs High Impedance	—	1	FB_CLK cycles
R9	Minimum RSTOUT pulse width	512	—	FB_CLK cycles

1 $\overline{\text{RESET}}$ and configuration override data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

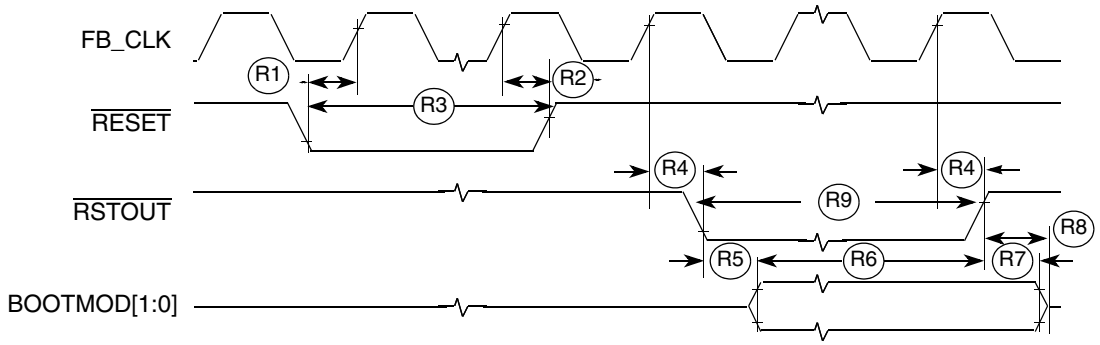


Figure 10. RESET and configuration override timing

4.10 FlexBus timing specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the FlexBus output clock (FB_CLK). All other timing relationships can be derived from these values.

All FlexBus signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

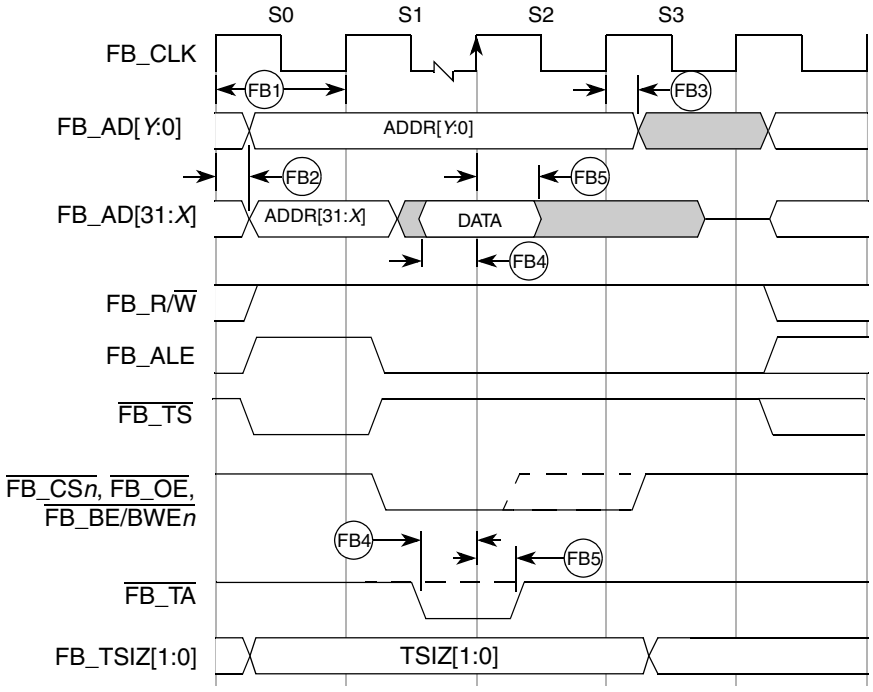
Table 16. FlexBus timing specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of operation	—	62.5	MHz	
FB1	Clock period	16	—	ns	
FB2	Output valid	—	6.0	ns	1
FB3	Output hold	0.5	—	ns	1
FB4	Input setup	5.5	—	ns	2
FB5	Input hold	0	—	ns	2

1 Specification is valid for all FB_AD[31:0], FB_R/W, FB_ALE, FB_TS, FB_CS*n*, FB_OE, FB_BE/BWE*n*, and FB_TSIZ[1:0].

2 Specification is valid for all FB_AD[31:0] and FB_TA.

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

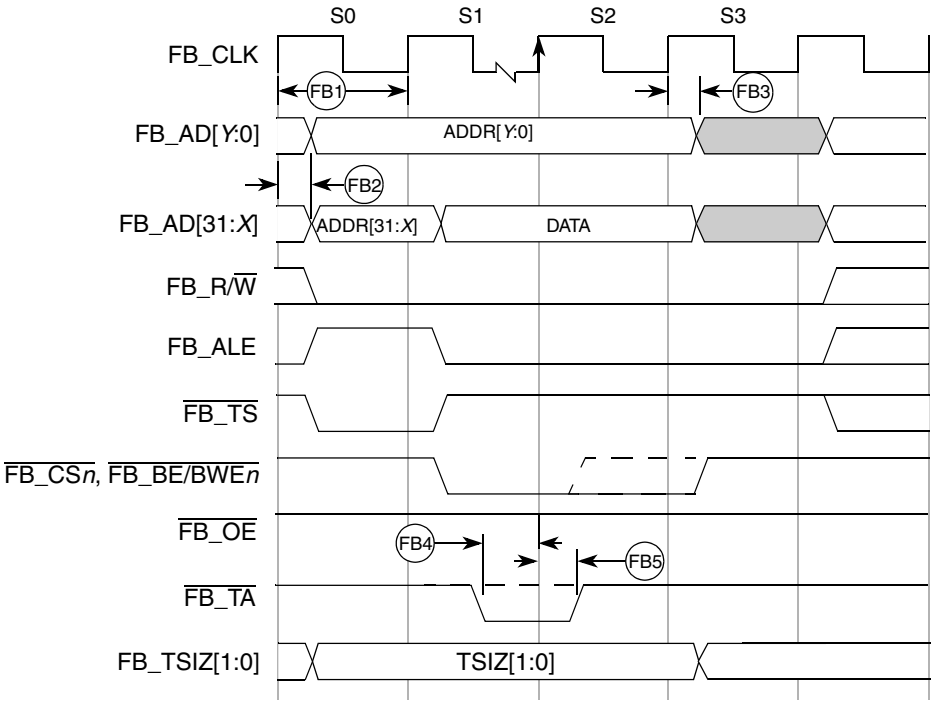


Note:

1 FB2 and FB3 output specifications are valid for all FB_AD[31:0], FB_R/W, FB_ALE, FB_TS, FB_CS*n*, FB_OE, FB_BE/BWE*n*, and FB_TSIZ[1:0].

2 FB4 and FB5 input specifications are valid for all FB_AD[31:0] and FB_TA.

Figure 11. FlexBus read timing



Note:

1 FB2 and FB3 output specifications are valid for all FB_AD[31:0], FB_R/W, FB_ALE, FB_TS, FB_CS*n*, FB_OE, FB_BE/BWE*n*, and FB_TSIZ[1:0].

2 FB4 and FB5 input specifications are valid for all FB_AD[31:0] and FB_TA.

Figure 12. FlexBus write timing

4.11 NAND flash controller (NFC) timing specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

All NFC signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 17. NFC timing specifications

Num	Characteristic	Symbol	Min	Max	Unit
	Frequency of operation		—	40[1]	MHz
NF1	Clock period	t_{NFC}	25	—	ns
NF2	NFC_CLE setup time	t_{CLS}	$1.5 \times t_{NFC}$	—	ns
NF3	NFC_CLE hold time	t_{CLH}	t_{NFC}	—	ns
NF4	NFC_CE setup time	t_{CS}	$1.5 \times t_{NFC}$	—	ns
NF5	NFC_CE hold time	t_{CH}	t_{NFC}	—	ns
NF6	NFC_WE pulse width	t_{WP}	$0.5 \times t_{NFC} - 0.5$	—	ns

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 17. NFC timing specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
NF7	NFC_ALE setup time	t_{ALS}	$1.5 \times t_{NFC}$	—	ns
NF8	NFC_ALE hold time	t_{ALH}	t_{NFC}	—	ns
NF9	Data setup time	t_{DS}	$0.5 \times t_{NFC} - 4$	—	ns
NF10	Data hold time	t_{DH}	$0.5 \times t_{NFC} - 10$	—	ns
NF11	Write cycle time	t_{WC}	t_{NFC}	—	ns
NF12	$\overline{\text{NFC\_WE}}$ high hold time	t_{WH}	$0.5 \times t_{NFC} - 1$	—	ns
NF13	Ready to $\overline{\text{NFC\_RE}}$ low	t_{RR}	$4.5 \times t_{NFC}$	—	ns
NF14	$\overline{\text{NFC\_RE}}$ pulse width	t_{RP}	$0.5 \times t_{NFC} - 0.5$	—	ns
NF15	Read cycle time	t_{RC}	t_{NFC}	—	ns
NF16	$\overline{\text{NFC\_RE}}$ high hold time	t_{REH}	$0.5 \times t_{NFC} - 1$	—	ns
NF17	Data in setup time	t_{DSU}	6	—	ns

1 50 MHz maximum frequency can only be used if the part is in EDO (enhanced data out) mode.

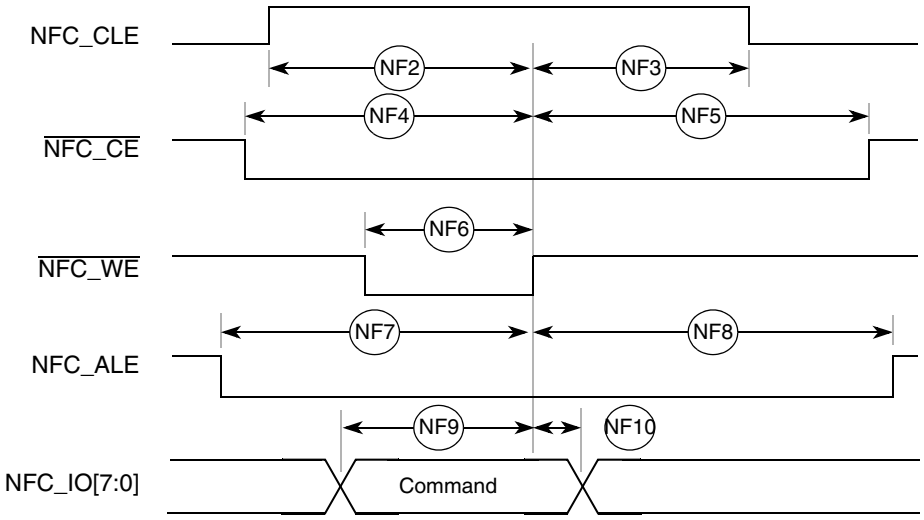


Figure 13. Command latch cycle timing

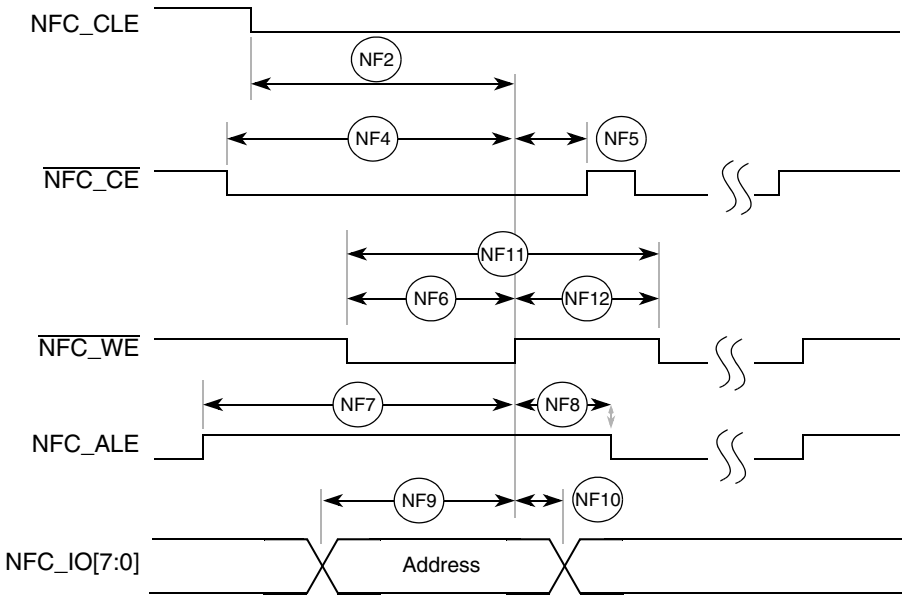


Figure 14. Address latch cycle timing

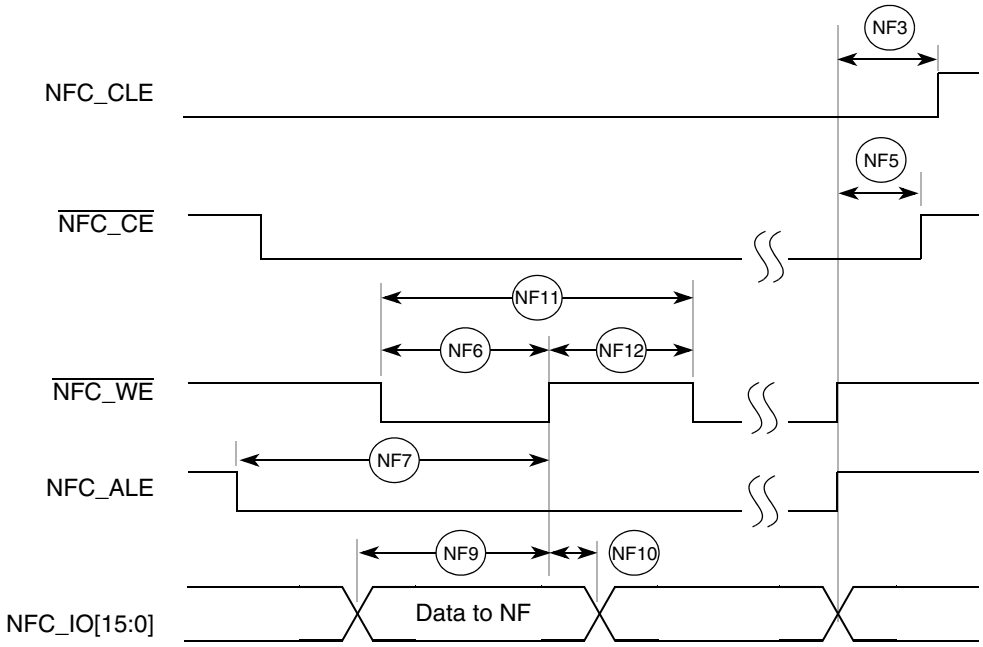


Figure 15. Write data latch timing

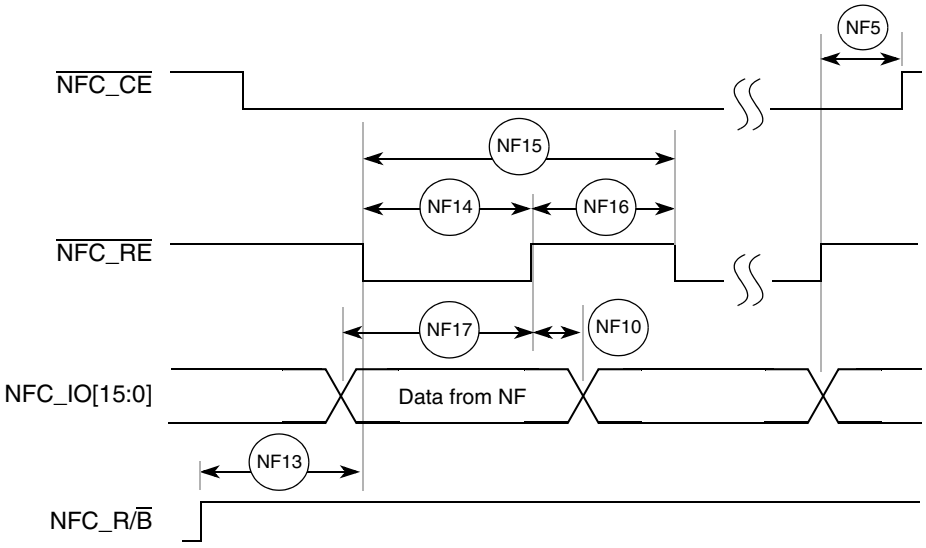


Figure 16. Read data latch timing

4.12 DDR SDRAM controller timing specifications

The following timing numbers must be followed to properly latch or drive data onto the SDRAM memory bus. All timing numbers are relative to the DQS byte lanes.

Table 18. SDRAM timing specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of operation		100	250	MHz	
DD1	Clock period	t_{SDCK}	4.0	10.0	ns	
DD2	Pulse width high	t_{SDCKH}	0.45	0.55	t_{SDCK}	1
DD3	Pulse width low	t_{SDCKL}	0.45	0.55	t_{SDCK}	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] — output valid	t_{CMV}	—	$0.5 \times t_{SDCK} + 1$	ns	2
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] — output hold	t_{CMH}	$0.5 \times t_{SDCK} - 1$	—	ns	
DD6	Write command to first DQS latching transition	t_{DQSS}	—	$WL + 0.2 \times t_{SDCK}$	ns	
DD7	Data and data mask output setup (DQ→DQS) relative to DQS (DDR write mode)	t_{QS}	0.4	—	ns	3 4
DD8	Data and data mask output hold (DQS→DQ) relative to DQS (DDR write mode)	t_{QH}	0.4	—	ns	5
DD9	Input data skew relative to DQS (input setup)	t_{IS}	—	0.5	ns	6
DD10	Input data hold relative to DQS.	t_{IH}	$0.375 \times t_{SDCK}$	—	ns	7

1 Pulse width high plus pulse width low cannot exceed min and max clock period.

2 Command output valid should be 1/2 the memory bus clock (t_{SDCK}) plus some minor adjustments for process, temperature, and voltage variations.

3 This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

4 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

5 This specification relates to the required hold time of DDR memories. SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

6 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

7 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

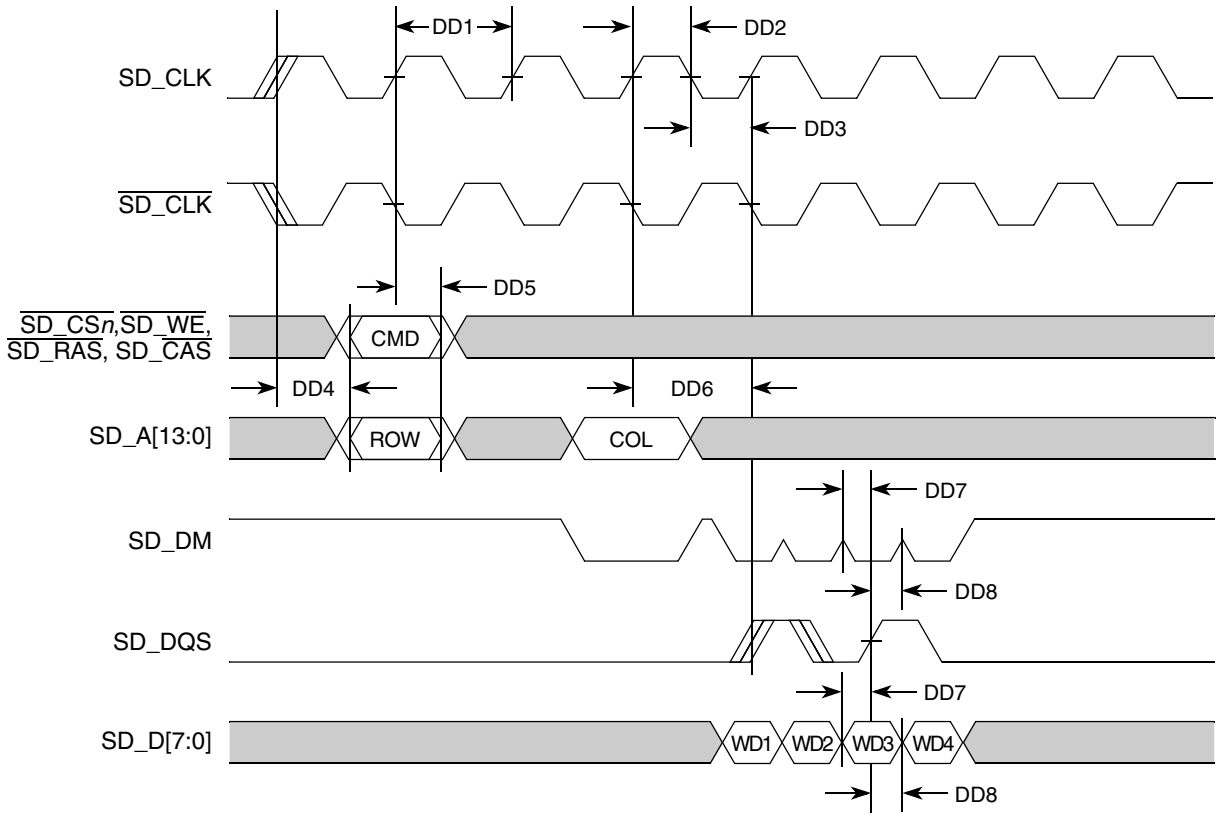


Figure 17. DDR write timing

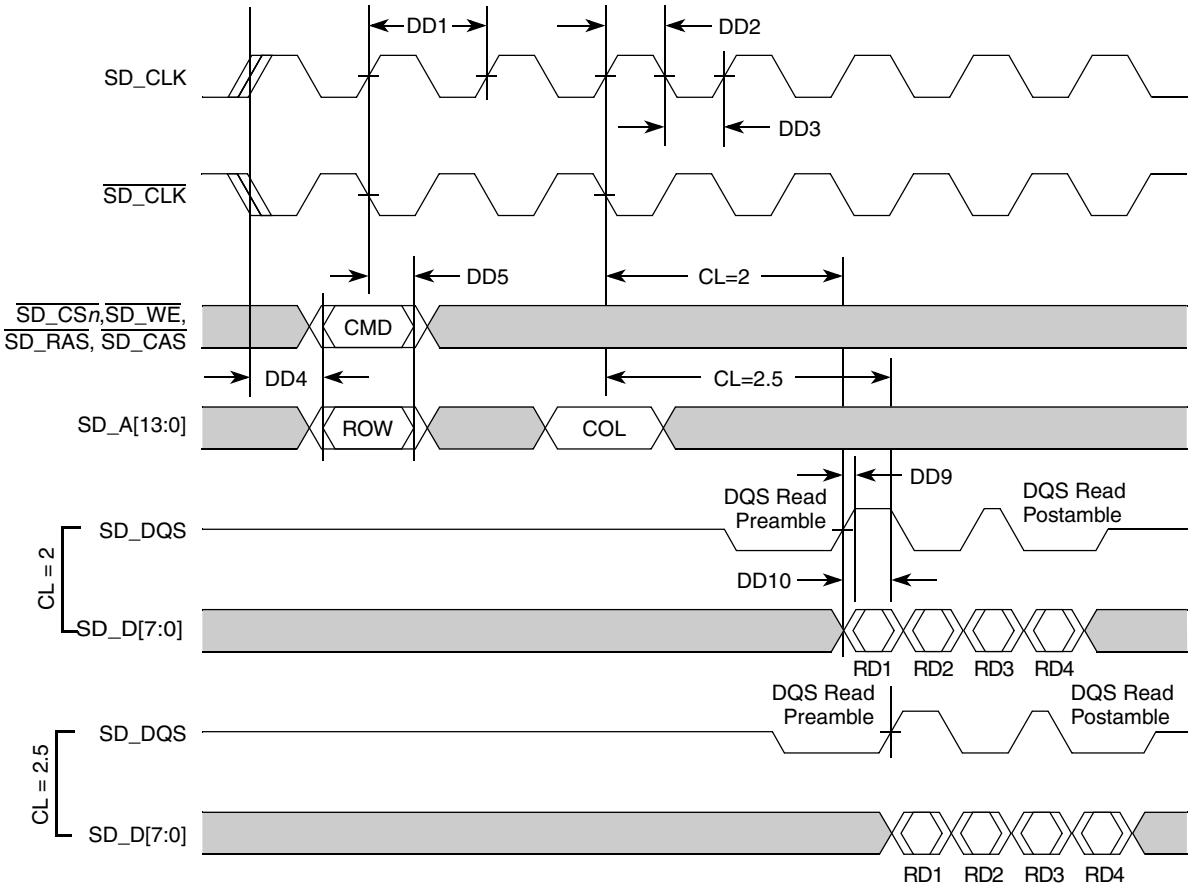


Figure 18. DDR read timing

4.13 USB transceiver timing specifications

The MCF5441*x* device is compliant with industry standard USB 2.0 specification.

4.14 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in Table 19. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin on the MCF5441*x*. The ULPI PHY is the source of the 60MHz clock.

NOTE

The USB controller requires a 60-MHz clock, even if using the on-chip FS/LS transceiver instead of the ULPI interface. In this case, the 60-MHz clock can be generated by the PLL or input on the USB_CLKIN pin.

All ULPI signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 19. ULPI interface timing

Num	Characteristic	Min	Nominal	Max	Units
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input setup (control and data)	5.0	—	—	ns
U3	Input hold (control and data)	1.0	—	—	ns
U4	Output valid (control and data)	—	—	9.5	ns
U5	Output hold (control and data)	1.0	—	—	ns

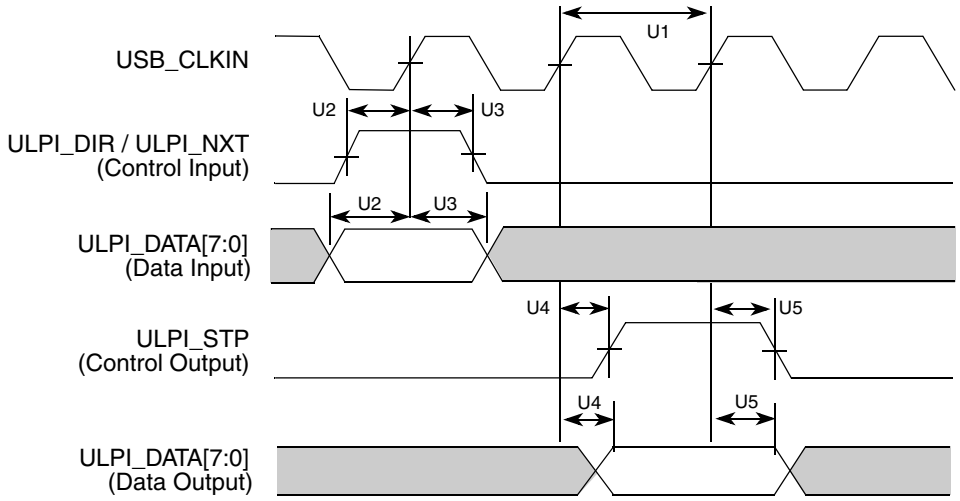


Figure 19. ULPI timing diagram

4.15 eSDHC timing specifications

This section describes the electrical information of the eSDHC.

All eSDHC signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[2]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

2.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

4.15.1 eSDHC timing specifications

Figure 20 depicts the timing of eSDHC, and Table 20 lists the eSDHC timing characteristics.

Table 20. eSDHC interface timing specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency (low speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO full speed)	f_{PP}[2]	0	40	MHz
	Clock frequency (MMC full speed)	f_{PP}[3]	0	20	MHz
	Clock frequency (identification mode)	f_{OD}[4]	100	400	kHz
SD2	Clock low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	eSDHC output delay (output valid)	t_{OD}	–5	5	ns
eSDHC Input / card outputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}	0	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value from 0 to 25 MHz.
3 In normal data transfer mode for MMC card, clock frequency can be any value from 0 to 20 MHz.
4 In card identification mode, card clock must be 100 kHz– 400 kHz, voltage ranges from 2.7 to 3.6 V.

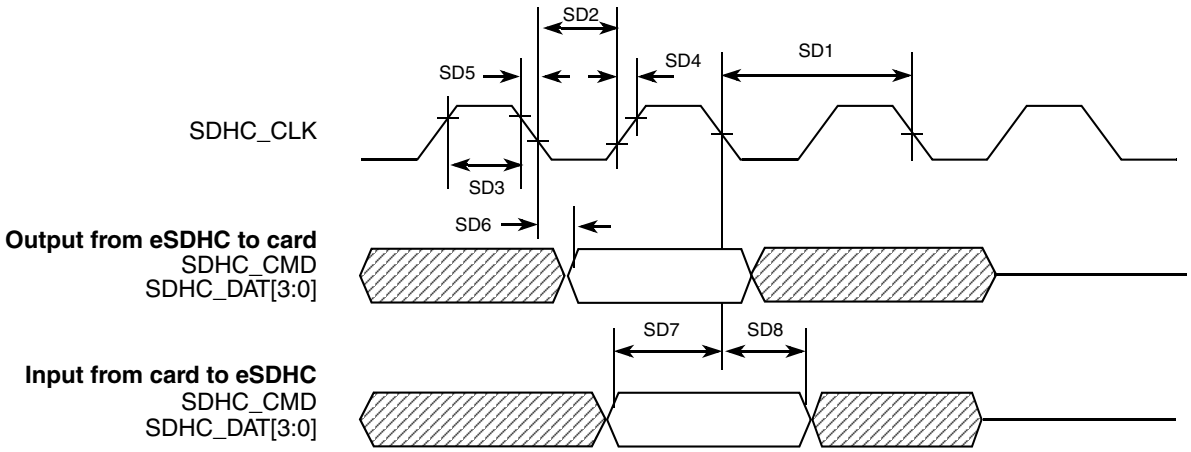


Figure 20. eSDHC timing

4.15.2 eSDHC electrical DC characteristics

Table 21 lists the eSDHC electrical DC characteristics.

Table 21. MMC/SD interface electrical specifications

Num	Parameter	Design value	Min	Max	Unit	Condition/remark
Bus signal line load						
7	Pull-up resistance	47	10	100	kΩ	Internal PU
8	Open drain resistance	NA	NA	NA	kΩ	For MMC cards only
Open drain signal level						For MMC cards only
9	Output high voltage		V_{DD} – 0.2		V	I_{OH} = –100 µA
10	Output low voltage			0.3	V	I_{OL} = 2 mA
Bus signal levels						
11	Output high voltage		0.75 x V_{DD}		V	I_{OH} = –100 µA @V_{DD} min
12	Output low voltage			0.125 x V_{DD}	V	I_{OL} = 100 µA @V_{DD} min
13	Input high voltage		0.625 x V_{DD}	V_{DD} + 3	V	
14	Input low voltage		V_{SS} – 0.3	0.25 x V_{DD}	V	

4.16 SIM timing specifications

Each SIM card interface consist of a total of 12 pins (two separate ports of six pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data, like a standard UART. All six (or five when a bidirectional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other. There are no required timing relationships between the signals in normal mode. However, there are some in reset and power down sequences.

All SIM signals use pad type pad_msr. SIM timing is fairly relaxed compared to other interfaces and can be met at 50 pF loading with any slew rate setting other than 00.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

4.16.1 General timing requirements

Figure 21 shows the timing of the SIM module, and Table 22 lists the timing parameters.

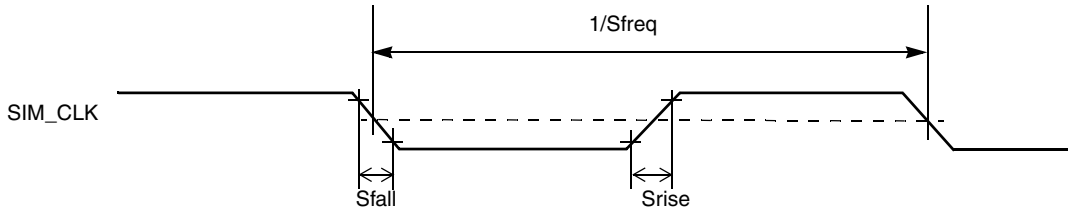


Figure 21. SIM clock timing diagram

Table 22. SIM timing specification—High Drive strength

Num	Description	Symbol	Min	Max	Unit
1	SIM clock frequency (SIM_CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM_CLK rise time [2]	S_{rise}	–	20	ns
3	SIM_CLK fall time [3]	S_{fall}	–	20	ns
4	SIM input transition time (RX, SIM_PD)	S_{trans}	–	25	ns

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

4.16.2 Reset sequence

4.16.2.1 Cards with internal reset

The reset sequence for this kind of SIM card is as follows (see Figure 22):

- After powerup, the clock signal is enabled on SIM_CLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40,000 clock cycles after T0.

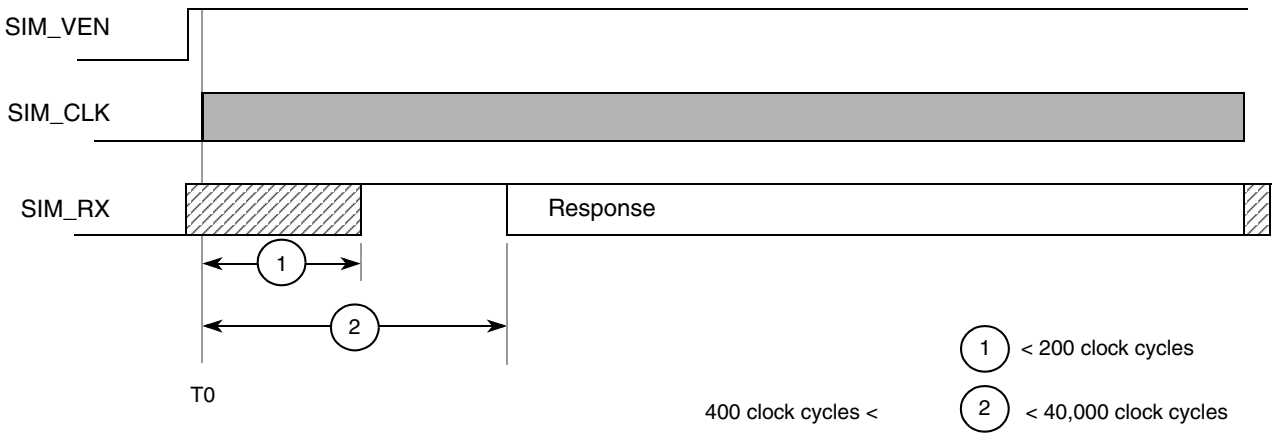


Figure 22. Internal-reset card reset sequence

4.16.2.2 Cards with active-low reset

The sequence of reset for this kind of card is as follows (see Figure 23):

1. After powerup, the clock signal is enabled on SIM_CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. SIM_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
4. SIM_RST is set high (time T1)
5. SIM_RST must remain high for at least 40,000 clock cycles after T1 and a response must be received on RX between 400 and 40,000 clock cycles after T1.

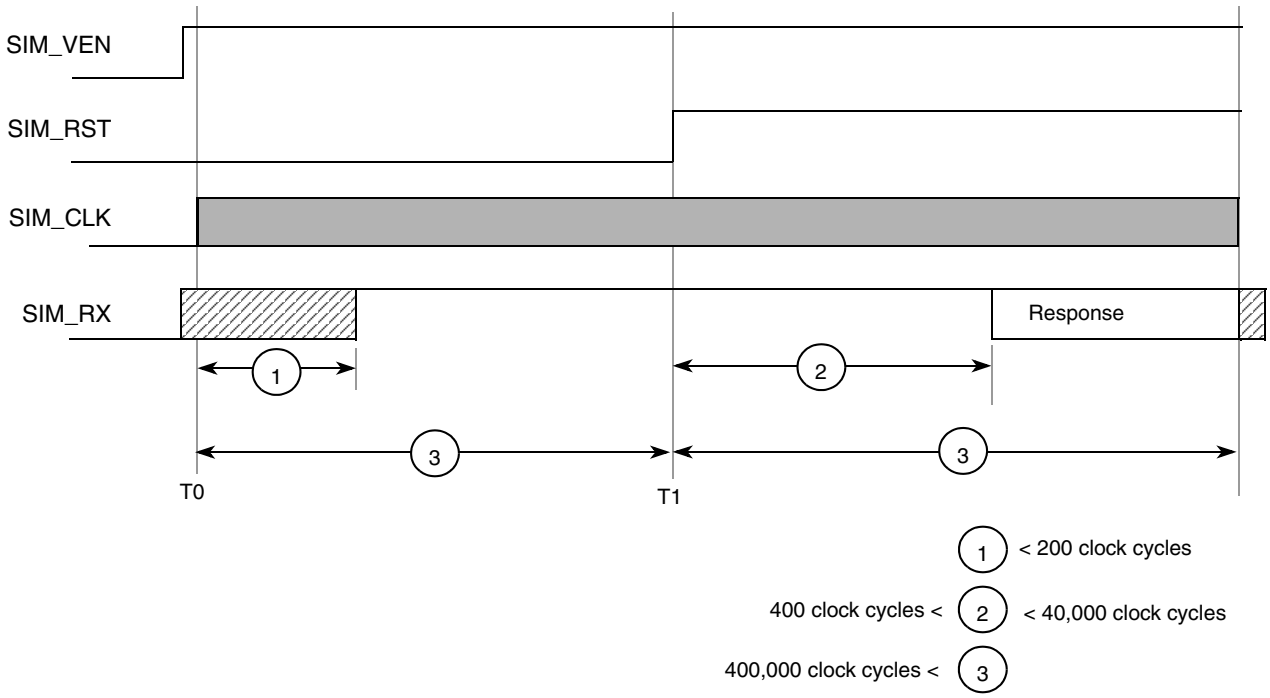


Figure 23. Active-low-reset card reset sequence

4.16.3 Power-down sequence

Power down sequence for SIM interface is as follows:

1. SIM_PD port detects the removal of the SIM card
2. SIM_RST goes low
3. SIM_CLK goes low
4. SIM_TX goes low
5. SIM_VEN goes low

Each of these steps is completed in one CKIL period (usually 32 kHz). Power-down may be started in response to a card-removal detection or launched by the processor. Figure 24 and Table 23 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

Table 23. Timing requirements for power-down sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 ÷ f_{CKIL}	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8 ÷ f_{CKIL}	1.2	µs
3	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 ÷ f_{CKIL}	1.8	µs
4	SIM presence detect to SIM reset low	S_{pd2rst}	0.9 ÷ f_{CKIL}	25	ns

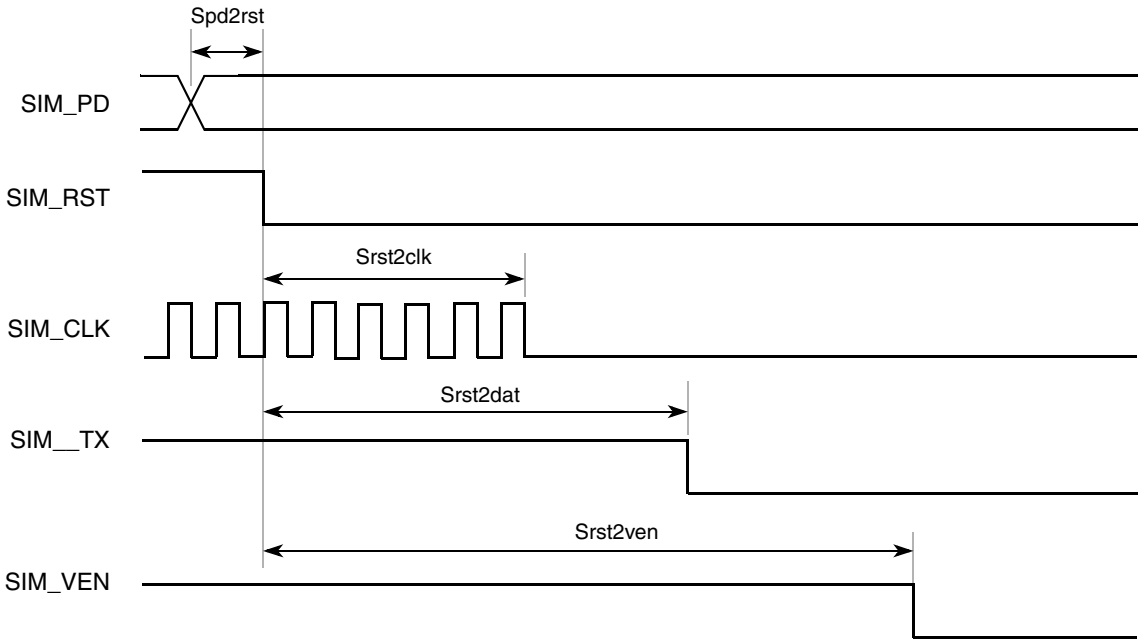


Figure 24. SmartCard interface power-down AC timing

4.17 SSI timing specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

All SSI signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF. When the SSI_MCLK output is not used, the maximum SSI bit clock (SSI_BCLK) frequency is such that timing can also be met at slew rate settings 10 and 01.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 24. SSI timing — master modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	15.15	—	ns	2
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	80	—	ns	3
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedance		0	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		15	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capacitive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

Table 25. SSI timing — slave modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	80	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedance		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		15	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capacitive load of 25pF.

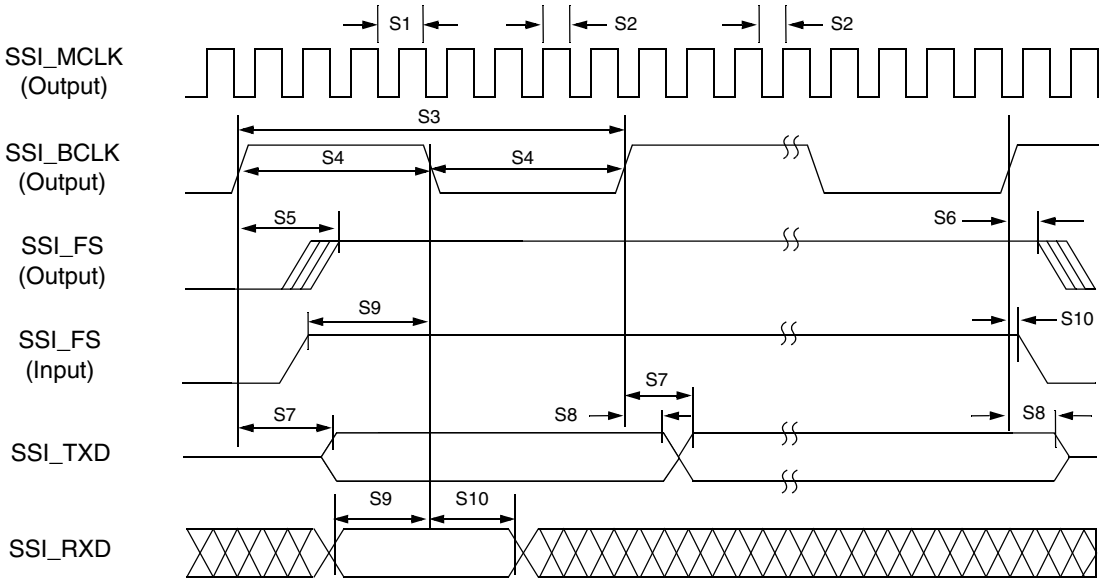


Figure 25. SSI timing — master modes

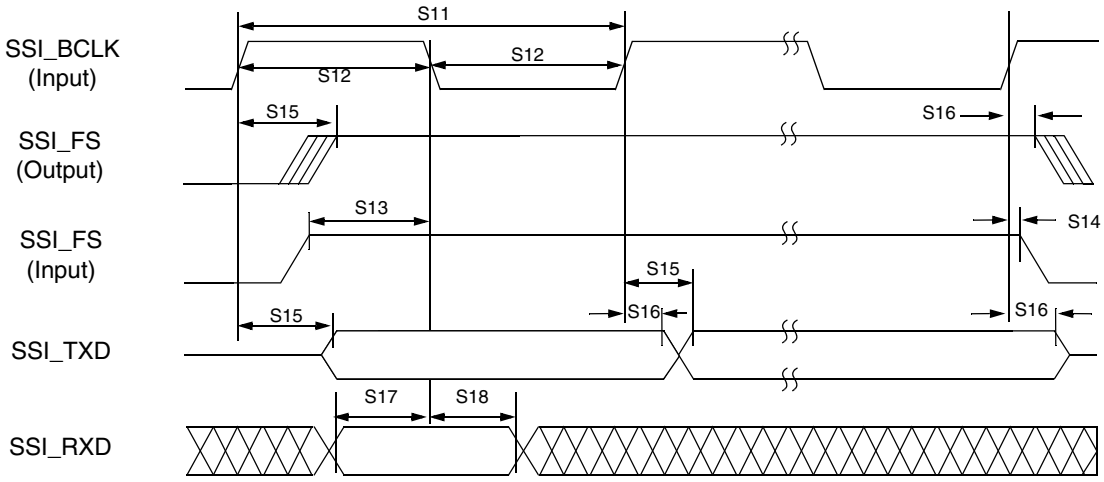


Figure 26. SSI timing — slave modes

4.18 12-bit ADC specifications

Table 26. ADC parameters[1]

Characteristic	Name	Min	Typical	Max	Unit
Frequency of operation		200kHz	—	12MHz	
ADC clock period	t_{ADC}	8.33	—	500	ns
Low reference voltage	V_{REFL}	V_{SS}	—	V_{REFH}	V
High reference voltage	V_{REFH}	V_{REFL}	—	AV_{DD}	V
Integral non-linearity (10% to 90% input signal range)[2]	INL	—	±3	—	lsb

Table 26. ADC parameters[1] (continued)

Characteristic	Name	Min	Typical	Max	Unit
Differential non-linearity (10% to 90% input signal range)[3]	DNL	—	±0.6	—	lsb
Monotonicity		Guaranteed			
Conversion time		—	—	6	t_{ADC} cycles
Sample time		—	—	1	t_{ADC} cycles
ADC power-up time[4]	t_{ADPU}	—	—	13	t_{ADC} cycles[5]
Recovery from auto standby	t_{REC}	—	0	6	t_{ADC} cycles
Input impedance	X_{IN}	—	2k	—	Ω
Input injection current[6], per pin	I_{ADI}	—	—	3	mA
V_{REFH} current	I_{VREFH}	—	100	—	nA
Offset voltage internal reference (at the y intercept)	$V_{OFFSET0}$	—	±20	—	LSB
Offset voltage internal reference (at the 50% FSR point)	$V_{OFFSET50}$	—	±12	—	LSB
Gain error (transfer path)	E_{GAIN}	—	±0.2	—	%
Spurious free dynamic range	SFDR	—	57	—	dB
Signal-to-noise plus distortion	SINAD	—	55	—	dB
Signal-to-noise ratio	SNR	—	60	—	dB
Effective number of bits	ENOB	—	9	—	Bits

1 All ADC parameter measurements are preliminary pending full characterization.
These measurements were made at V_{DD} = 3.3 V, V_{REFH} = 3.3 V, and V_{REFL} = ground.
2 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
3 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
4 Includes power-up of ADC and V_{REF}
5 ADC clock cycles
6 The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

4.19 12-bit DAC timing specifications

Table 27 shows electrical specifications of DAC.

Table 27. DAC parameters[1]

Characteristic	Name	Min	Typical	Max	Unit
Range of digital input words: 497 to 3599 (0x1F1–0xE0F)	LSB	—	806	—	uV
Monotonicity		Guaranteed			
Conversion time (high-speed)		1	—	—	us
Conversion time (low-speed)		2	—	—	us
Conversion rate (high-speed)		—	—	1M	conv/sec
Conversion rate (low-speed)		—	—	500K	conv/sec
Output swing		AVSS + 0.04	—	AVDD – 0.04	V

Table 27. DAC parameters[1] (continued)

Characteristic	Name	Min	Typical	Max	Unit
Integral non-linearity (497 to 3599)	INL	—	—	±8.0	lsb
Differential non-linearity (497 to 3599)	DNL	—	—	±0.5	lsb
Gain error (497 to 3599)	E_{GAIN}	—	±0.26	—	%
Effective number of bits	ENOB	9	—	—	bits
DAC power-up time	t_{DAPU}	—	—	11	us
Output load resistance	R_L	3K	—	—	Ohm
Output load capacitance	C_L	—	400	—	pF
Power supply ripple rejection	PSRR	—	60	—	dB

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground

4.20 mcPWM timing specifications

Table 28. mcPWM timing

Num	Characteristic	Min	Max	Unit
G1	FB_CLK high to output valid	—	7	ns
G2	FB_CLK high to output invalid	1	—	ns
G3	Input valid to FB_CLK high	3	—	ns
G4	FB_CLK high to input invalid	1	—	ns

4.21 I²C timing specifications

Table 29 lists specifications for the I²C input timing parameters shown in Figure 27.

Table 29. I²C input timing specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	$1/f_{SYS}$
I2	Clock low period	8	—	$1/f_{SYS}$
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	$1/f_{SYS}$
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	$1/f_{SYS}$
I9	Stop condition setup time	2	—	$1/f_{SYS}$

Table 30 lists specifications for the I²C output timing parameters shown in Figure 27.

Table 30. I²C output timing specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	$1/f_{SYS}$
I2[1]	Clock low period	10	—	$1/f_{SYS}$
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	7	—	$1/f_{SYS}$
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	10	—	$1/f_{SYS}$
I7[1]	Data setup time	2	—	$1/f_{SYS}$
I8[1]	Start condition setup time (for repeated start condition only)	20	—	$1/f_{SYS}$
I9[1]	Stop condition setup time	10	—	$1/f_{SYS}$

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 30. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR. However, the numbers given in Table 30 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

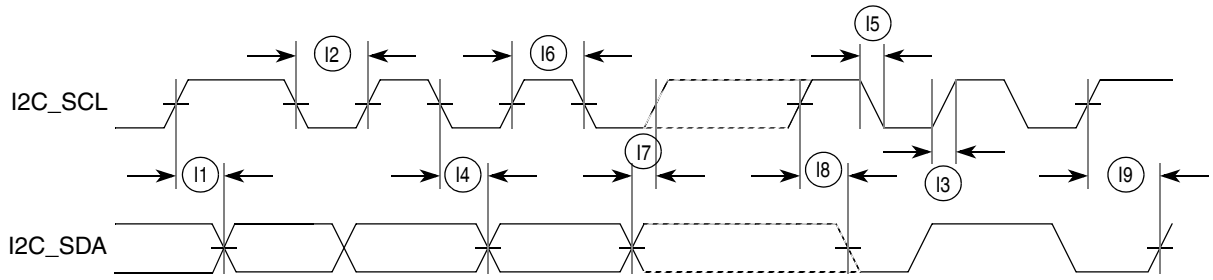


Figure 27. I²C input/output timings

4.22 Ethernet assembly timing specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

All Ethernet signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

4.22.1 Receive signal timing specifications

The following timing specs meet the requirements for MII and RMII interfaces for a range of transceiver devices.

Table 31. Receive signal timing

Num	Characteristic	MII mode		RMII mode		Unit
		Min	Max	Min	Max	
—	RXCLK frequency	—	25	—	50	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	4	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	2	—	ns
E3	RXCLK pulse width high	35%	65%	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	35%	65%	RXCLK period

1 In MII mode, n = 3; In RMII mode, n = 1

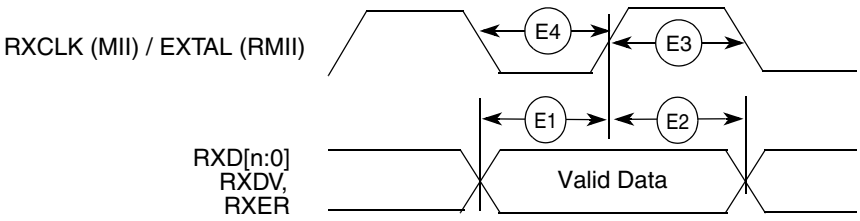


Figure 28. MII/RMII receive signal timing diagram

4.22.2 Transmit signal timing specifications

Table 32. Transmit signal timing

Num	Characteristic	MII mode		RMII mode		Unit
		Min	Max	Min	Max	
—	TXCLK frequency	—	25	—	50	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	4	—	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	—	14	ns
E7	TXCLK pulse width high	35%	65%	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	35%	65%	t_{TXCLK}

1 In MII mode, n = 3; In RMII mode, n = 1

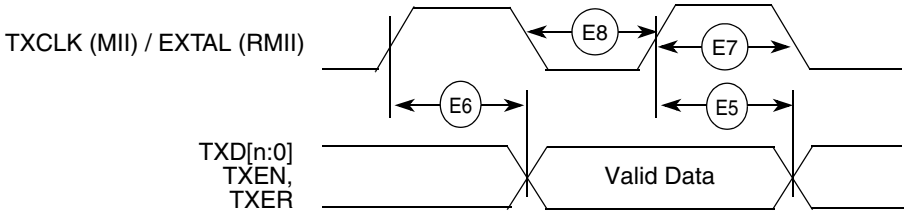


Figure 29. MII/RMII transmit signal timing diagram

4.22.3 Asynchronous input signal timing specifications

Table 33. MII/RMII transmit signal timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

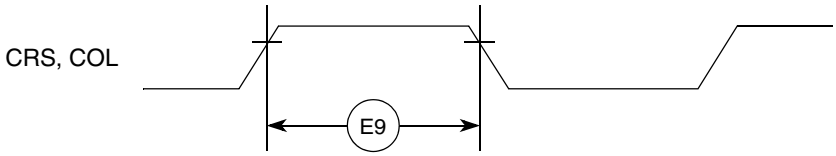


Figure 30. MII/RMII async inputs timing diagram

4.22.4 MDIO serial management timing specifications

Table 34. MDIO serial management channel signal timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

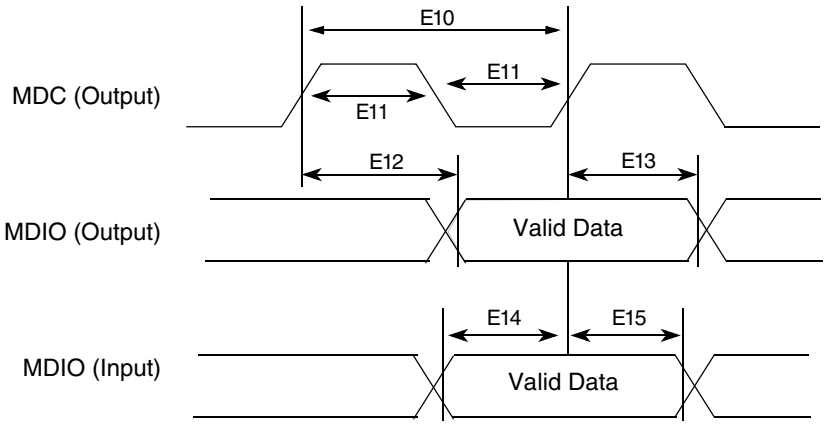


Figure 31. MDIO serial management channel timing diagram

4.23 32-bit timer module timing specifications

Table 35 lists timer module AC timings.

Table 35. Timer module AC timing specifications

Name	Characteristic	Min	Max	Unit
T1	DT*n*IN cycle time (*n* = 0:3)	3	—	$1/f_{SYS/2}$
T2	DT*n*IN pulse width (*n* = 0:3)	1	—	$1/f_{SYS/2}$

4.24 DSPI timing specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. Table 36 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF54418 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

All DSPI signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 36. DSPI module AC timing specifications[1]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
Master Mode						
—	DSPI_SCK frequency	f_{SCK}	—	50	MHz	
DS1	DSPI_SCK cycle time	t_{SCK}	20	—	ns	2
DS2	DSPI_SCK duty cycle	—	$(t_{sck} \div 2) - 2.0$	$(t_{sck} \div 2) + 2.0$	ns	3
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	$(t_{sck} \div 2) - 2.0$	—	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	$(t_{sck} \div 2) - 3.0$	—	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 36. DSPI module AC timing specifications[1] (continued)

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS6	DSPI_SCK to DSPI_SOUT invalid	—	–5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
—	DSPI_SCK frequency	f_{SCK}	—	$f_{SYS} \div 8$	MHz	
DS9	DSPI_SCK cycle time	t_{SCK}	$8 \div f_{SYS}$	—	ns	
DS10	DSPI_SCK duty cycle	—	$(t_{sck} \div 2) - 2.0$	$(t_{sck} \div 2) + 2.0$	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	—	12	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	—	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	—	2	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	—	7	—	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	—	10	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	—	10	ns	

1 Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTAR*n*[CPHA] = 0. Data is sampled on the DSPI_SIN pin on the odd-numbered DSPI_SCK edges and driven on the DSPI_SOUT pin on even-numbered DSPI edges.

2 When in master mode, the baud rate is programmable in DCTAR*n*[DBR], DCTAR*n*[PBR], and DCTAR*n*[BR].

3 This specification assumes a 50/50 duty cycle setting. The duty cycle is programmable in DCTAR*n*[DBR], DCTAR*n*[CPHA], and DCTAR*n*[PBR].

4 The DSPI_PCS*n* to DSPI_SCK delay is programmable in DCTAR*n*[PCSSCK] and DCTAR*n*[CSSCK].

5 The DSPI_SCK to DSPI_PCS*n* delay is programmable in DCTAR*n*[PASC] and DCTAR*n*[ASC].

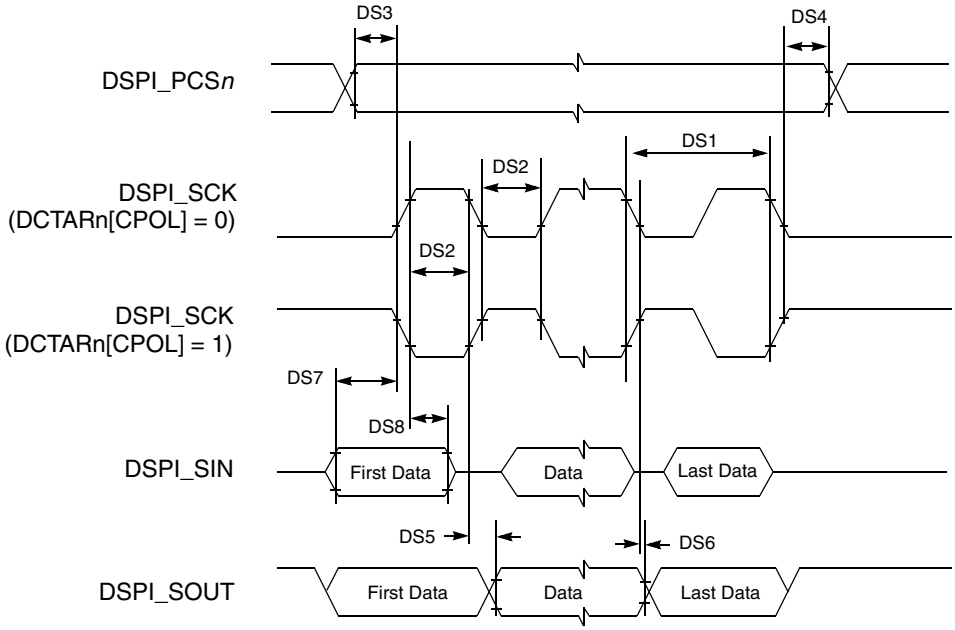


Figure 32. DSPI Classic SPI timing — master Mode

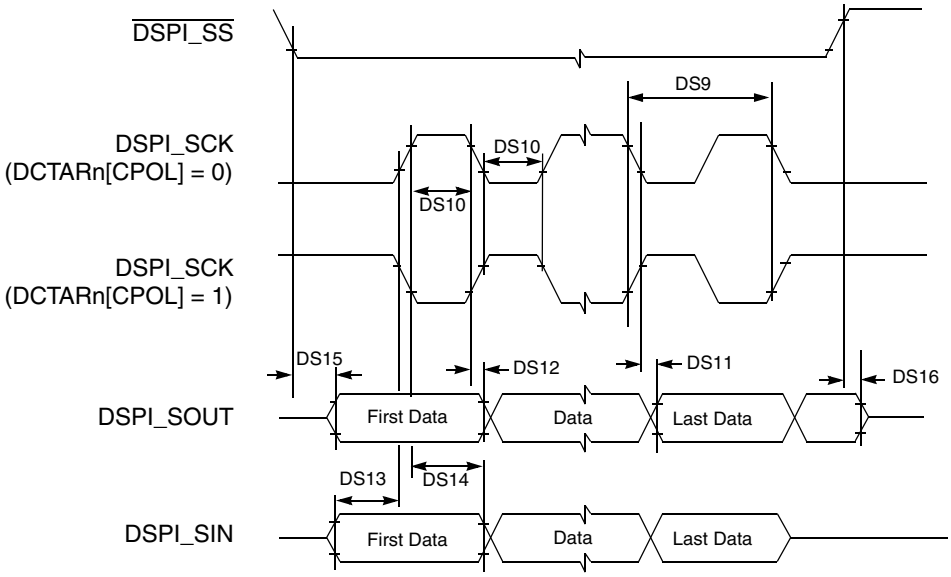


Figure 33. DSPI Classic SPI timing — slave mode

4.25 SBF timing specifications

The Serial boot facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 37 provides the AC timing specifications for the SBF.

All SBF signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 37. SBF AC timing specifications

Name	Characteristic	Symbol	Min	Max	Unit	Notes
—	SBF_CK frequency	f_{SBFCK}	—	62.5	MHz	
SB1	SBF_CK cycle time	t_{SBFCK}	16.67	—	ns	1
SB2	SBF_CK high/low time	—	30%	—	t_{SBFCK}	
SB3	$\overline{SBF\_CS}$ to SBF_CK delay	—	$t_{SBFCK} - 2.0$	—	ns	
SB4	SBF_CK to $\overline{SBF\_CS}$ delay	—	$t_{SBFCK} - 2.0$	—	ns	
SB5	SBF_CK to SBF_DO valid	—	—	5	ns	
SB6	SBF_CK to SBF_DO invalid	—	–5	—	ns	
SB7	SBF_DI to SBF_SCK input setup	—	10	—	ns	
SB8	SBF_CK to SBF_DI input hold	—	0	—	ns	

1 At reset, the SBF_CK cycle time is $t_{REF} \times 60$. The first byte of data read from the serial memory contains a divider value that is used to set the SBF_CK cycle time for the duration of the serial boot process.

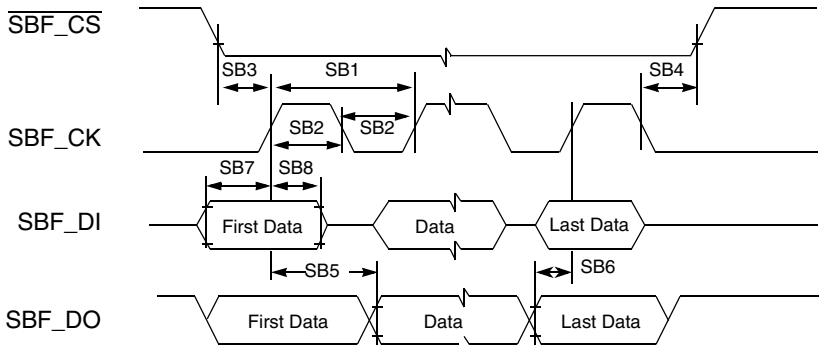


Figure 34. SBF timing

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

4.26 1-Wire timing specifications

Specifications for the 1-Wire interface are provided by Maxim Integrated Products, Inc. Please refer to data sheet information for the appropriate device at www.maxim-ic.com.

4.27 General purpose I/O timing specifications

Table 38. GPIO timing[1]

Num	Characteristic	Min	Max	Unit
G1	FB_CLK high to GPIO output valid	—	9	ns
G2	FB_CLK high to GPIO output invalid	1	—	ns
G3	GPIO input valid to FB_CLK high	9	—	ns
G4	FB_CLK high to GPIO input invalid	1.5	—	ns

1 These general purpose specifications apply to the following signals: $\overline{\text{IRQ}}n$, all UART signals, all timer signals, FlexCAN signals, $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$, and all signals configured as GPIO.

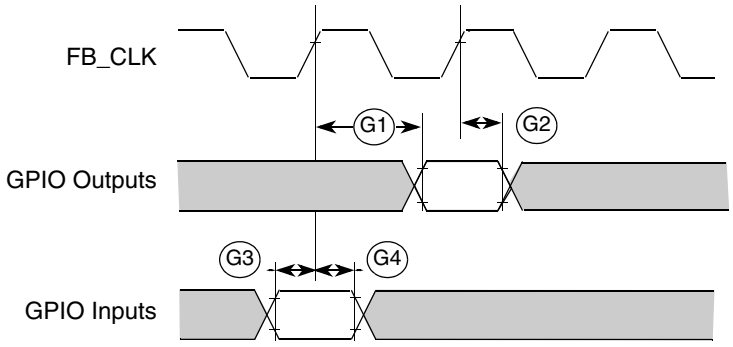


Figure 35. GPIO timing

4.28 Rapid general purpose I/O timing specifications

RGPIO signals use a mix of pad types: pad_fsr, pad_msr, and pad_ssr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.

Table 39. RGPIO timing

Num	Characteristic	Min	Max	Unit
RG1	PST_CLK high to RGPIO output valid	—	6	ns
RG2	PST_CLK high to RGPIO output Invalid	0.5	—	ns
RG3	RGPIO input valid to PST_CLK high	6	—	ns
RG4	PST_CLK high to RGPIO input invalid	1.5	—	ns

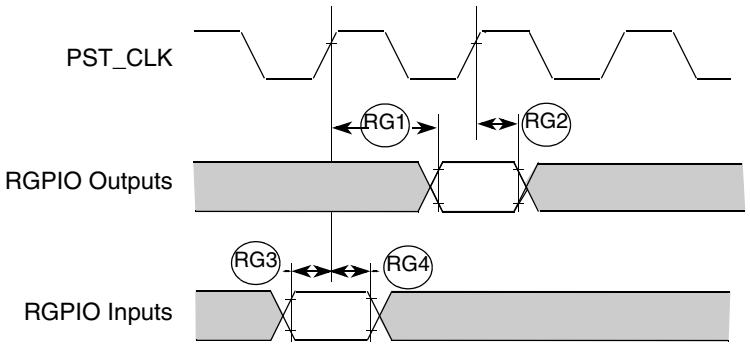


Figure 36. RGPIO timing

4.29 JTAG and boundary scan timing specifications

All JTAG signals use pad type pad_msr except for TCLK which use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 40. JTAG and boundary scan timing

Num	Characteristics[1]	Min	Max	Unit
J1	TCLK frequency of operation	DC	25	MHz
J2	TCLK cycle period	40	—	ns
J3	TCLK clock pulse width	20	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	20	—	ns
J7	TCLK low to boundary scan output data valid	—	13	ns
J8	TCLK low to boundary scan output high-Z	—	13	ns
J9	TMS, TDI input data setup time to TCLK rise	4	—	ns
J10	TMS, TDI input data hold time after TCLK rise	10	—	ns
J11	TCLK low to TDO data valid	—	12	ns
J12	TCLK low to TDO high-Z	—	0	ns
J13	$\overline{\text{TRST}}$ assert time	32	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

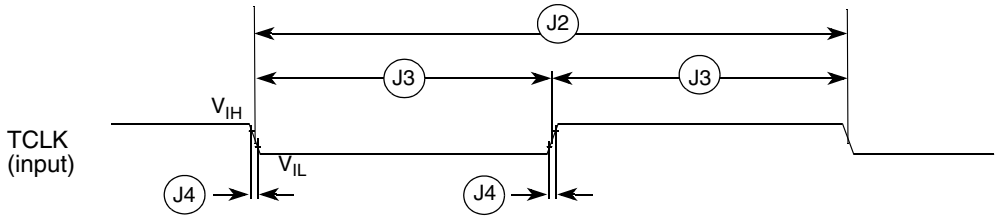


Figure 37. Test clock input timing

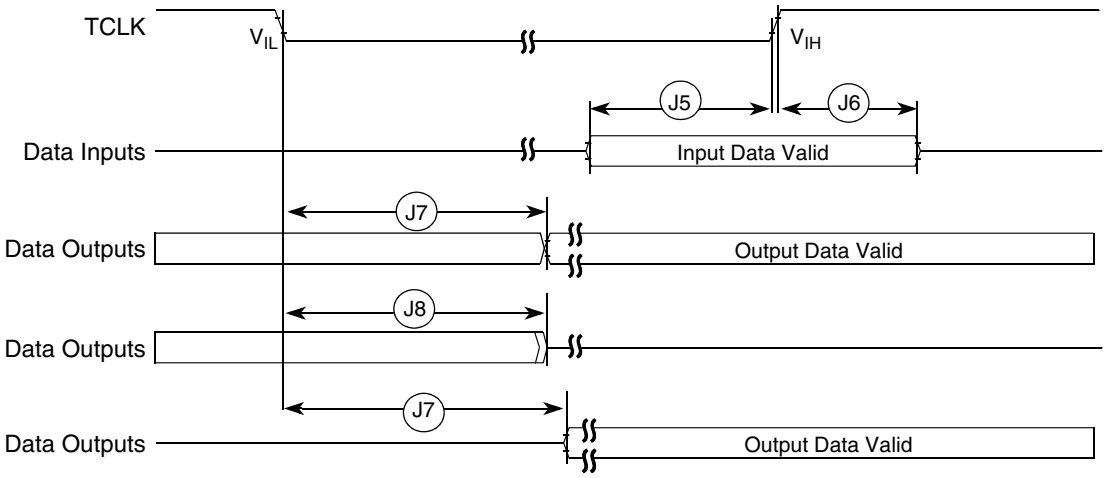


Figure 38. Boundary scan (JTAG) timing

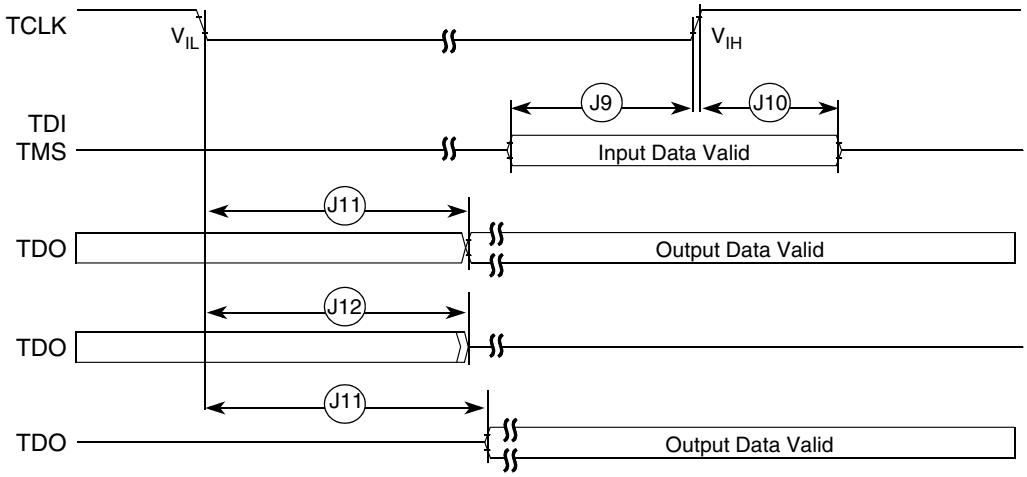


Figure 39. Test access port timing

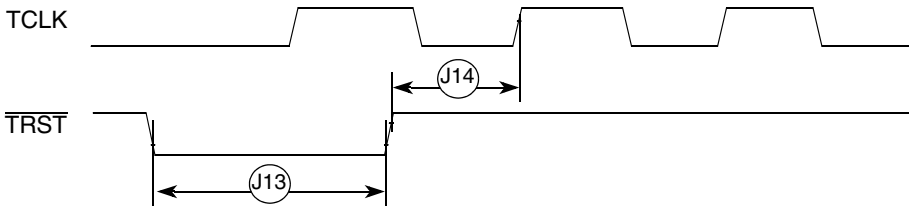


Figure 40. $\overline{\text{TRST}}$ timing

4.30 Debug AC timing specifications

Table 41 lists specifications for the debug AC timing parameters shown in Figure 41 and Table 42.

All debug signals use pad type pad_msr except for PSTCLK which use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 41. Debug AC timing specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	0.5	0.5	$1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	0.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

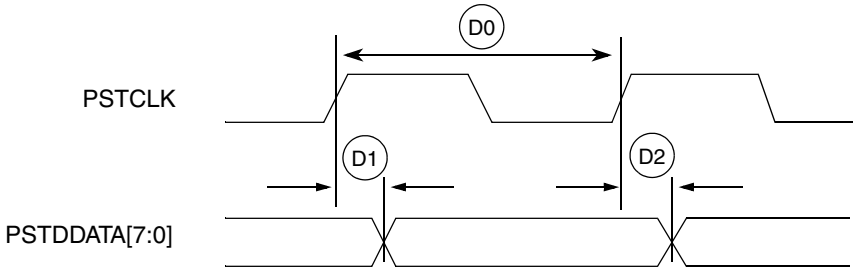


Figure 41. Real-time trace AC timing

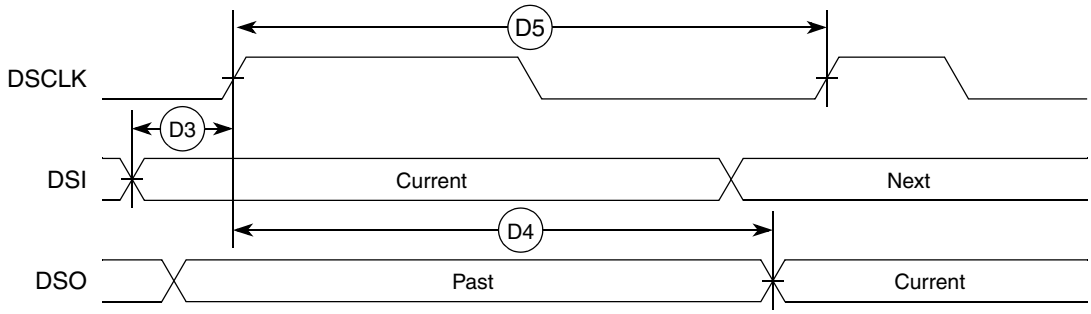


Figure 42. BDM serial port AC timing

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

5 Package information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 42 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 42. Package information

Device	Package type	Case outline numbers
MCF54410	196 MAPBGA	98ASA00321D
MCF54415	256 MAPBGA	98ARH98219A
MCF54416		
MCF54417		
MCF54418		

6 Product documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

7 Revision history

Table 43 summarizes revisions to this document.

Table 43. Revision history

Rev. No.	Date	Summary of changes
2	10 Jun 2009	In Section 2.2, "Supply voltage sequencing" added the following note: **NOTE** All I/O VDD pins must be powered on when the device is functioning, except when in standby mode. In standby mode, all I/O VDD pins, except VSTBY_RTC (battery), can be switched off. Added Section 3.2, "Pinout—169 MAPBGA" and Section 3.3, "Pinout—256 MAPBGA" and updated Table 5 with pin locations. In Section 4.1, "Absolute maximum ratings": • Added USB OTG, USB host, ADC, DAC/ADC, and RTC standby supply voltages In Section 4.5, "DC electrical specifications": • Added RTC standby supply voltage • Split out Power Supplies and I/O Characteristics to two separate tables In Section 4.10, "FlexBus timing specifications": • Changed maximum frequency to 100MHz and updated specs throughout the table • Changed FB2 maximum from 5 to 6 • Added notes to Figure 11 and Figure 12 In Section 4.12, "DDR SDRAM controller timing specifications": • Changed minimum frequency from 50 to 100 • Changed maximum DD1 from 20 to 10 • Changed DD5 from 2 to 0.5 x t_{SDCK} – 1 • Changed DD6 from 1.2 x t_{SDCK} to WL + 0.2 x t_{SDCK} • Changed DD7 from 1.5 to 0.7 • Changed DD8 from 1.0 to 0.7 • Changed DD9 from 1.0 to 0.5 • Changed DD10 from 0.25 x t_{SDCK} + 0.5 to 0.375 x t_{SDCK} In Section 4.17, "SSI timing specifications": • Changed S7, S9, S15, and S17 from 10 to 15 In Section 4.22.2, "Transmit signal timing specifications": • Changed E5 for MII from 5 to 4 In Section 4.20, "mcPWM timing specifications": • Changed G2 from 2 to 1 In Section 4.24, "DSPI timing specifications": • Changed DS3 from (2 x 1/fsys) – 2.0 to (t_{sck} ³ 2) – 2.0 • Changed DS4 from (2 x 1/fsys) – 3.0 to (t_{sck} ³ 2) – 3.0 • Changed DS7 from 7 to 6 • Changed DS11 from 4 to 12 In Section 4.25, "SBF timing specifications": • Changed SB5 maximum from 5 to 3 • Changed SB6 minimum from –5 to 5 In Section 4.26, "1-Wire timing specifications": • Added link to 1-wire specs In Section 4.27, "General purpose I/O timing specifications": • Changed G2 from 1.5 to 1 In Section 4.28, "Rapid general purpose I/O timing specifications": • Changed RG1 from 3 to 6 • Changed RG2 from 1.5 to 0.5 • Changed RG3 from 3 to 6 In Section 4.29, "JTAG and boundary scan timing specifications": • Changed J9-12 and J14 from TBD In Section 4.30, "Debug AC timing specifications": • Changed D2 from 1.5 to 0.5

Table 43. Revision history (continued)

Rev. No.	Date	Summary of changes
3	31 July 2009	Changed 169MAPBGA package to 196MAPBGA throughout. MCF54410 device now supports a single SSI module and one Ethernet controller with IEEE 1588 support
4	17 Aug 2009	Updated MCF5441*x* Signal Information and Muxing table with 196MAPBGA pin locations Changed SD_D*n* pin locations on 256 MAPBGA package Added note to Section 4.6, "Output pad loading and slew rate"
5	29 Jan 2010	Added orderable part numbers
6		Swapped locations of RTC_EXTAL and RTC_XTAL pins in Table 5, Figure 7, and Figure 8 Corrected instances of MCF5445*x* to MCF5441*x* Added thermal characteristic s to Table 7 Added case outline numbers to Table 42 Changed PLL supply voltage from "–0.5 to +2.0" to "–0.3 to +4.0" in Table 6 Miscellaneous corrections based on information from shared review comments by team members
7	October 2011	• Updated the pinouts in Table 5, "MCF5441x Signal information and muxing". • Updated the Figure 7, "MCF54410 Pinout (196 MAPBGA)". • Removed the symbol ADC_IN7/DAC1_OUT from Table 9, "Latch-up results". • Updated Table 11, "I/O electrical specifications". • Updated Table 13, "DDR pad drive strengths".
8	June 2012	• In Table 7, added the thermal characteristics for the 196 MAPBGA package. • In Table 42, updated the case outline number for the 196 MAPBGA package from "98ARH98217" to "98ASA00321D".

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Document Number: MCF54418
Rev. 8
06/2012