±15V, 128-Tap, Low-Drift Digital Potentiometers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND, V_{SS} = GND .....-0.3V to +34V
V_{SS} to GND, V_{DD} = GND .....-34V to +0.3V
V_{DD} to V_{SS} .....-0.3V to +34V
V_{DD} to V_{CC} .....-6.3V to +28.75V
V_{CC} to V_{SS} .....-0.3V to +34V
V_{CC} to GND .....-0.3V to +6V
DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$ .....-0.3V to (V_{CC} + 0.3V)
H, L, W, IN+, IN-, OUT .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Maximum Continuous Current into H, L, and W
MAX5436–MAX5439 .....±1mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 6.94mW/°C above +70°C) 556mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{SS} = -15V, V_{CC} = +5V, V_H = V_{DD}, V_L = V_{SS}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (voltage-divider mode)						
Resolution	2^N		128			Taps
Integral Nonlinearity	INL	(Note 1)			±1	LSB
Differential Nonlinearity	DNL	(Note 1)			±1	LSB
End-to-End Resistor Tempco	TC_R			35		ppm/°C
Ratiometric Resistor Tempco				5		ppm/°C
Full-Scale Error		R_{HL} = 50kΩ (MAX5436/MAX5437)		-0.3		LSB
Zero-Scale Error		R_{HL} = 50kΩ (MAX5436/MAX5437)		+0.3		LSB
Full-Scale Error		R_{HL} = 100kΩ (MAX5438/MAX5439)		-0.15		LSB
Zero-Scale Error		R_{HL} = 100kΩ (MAX5438/MAX5439)		+0.15		LSB
DC PERFORMANCE (variable-resistor mode)						
Resolution	2^N		128			Taps
Integral Nonlinearity	INL	(Note 2)			±1	LSB
Differential Nonlinearity	DNL	(Note 2)			±1	LSB
DC PERFORMANCE (resistor characteristics)						
Wiper Resistance	W_R	(Note 3)		0.9	2	kΩ
Wiper Capacitance	W_C	Midscale		6		pF
End-to-End Resistance	R_{HL}	MAX5438/MAX5439	75	100	125	kΩ
		MAX5436/MAX5437	37.5	50	62.5	
DIGITAL INPUTS						
Input High Voltage		V_{CC} = 4.75V to 5.25V (Note 4)	2.4			V
Input Low Voltage		V_{CC} = 4.75V to 5.25V			0.8	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +15V, V_{SS} = -15V, V_{CC} = +5V, V_H = V_{DD}, V_L = V_{SS}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage		V_{CC} = 2.7V to 3.6V	2.0			V
Input Low Voltage		V_{CC} = 2.7V to 3.6V			0.6	V
Input Leakage Current					±1.0	µA
Input Capacitance				5.0		pF
DYNAMIC CHARACTERISTICS (analog)						
Wiper -3dB Bandwidth	BW_W	R_{HL} = 50kΩ, midscale, V_H = 1.5V_{P-P}, C_{WIPER} = 20pF, voltage-divider mode		400		kHz
		R_{HL} = 100kΩ, midscale, V_H = 1.5V_{P-P}, C_{WIPER} = 20pF, voltage-divider mode		200		
Wiper Settling Time	t_{IL}	C_{WIPER} = 20pF, code 1 to code 127, settle to 0.5LSB		5		µs
AMPLIFIER CHARACTERISTICS (analog)						
Input Bias Current	I_B			15		nA
Input Offset Voltage	V_{OS}			±6		mV
Offset-Voltage Temperature Drift	V_{OSD}			10		µV/°C
Input Offset Current	I_{OS}			2		nA
Unity-Gain Bandwidth	UBW_A	C_{LOAD} = 250pF		100		kHz
Slew Rate	SR			0.25		V/µs
Large-Signal Voltage Gain	A_{VO}	R_{LOAD} = 100kΩ, V_{OUT} = ±14V		100		V/mV
Input Noise	V_N	f = 1kHz		110		nV/√Hz
Input Compliance	CMR_I		V_{SS} + 1		V_{DD} - 2	V
Output Compliance	CMR_O	I_{LOAD} = ±5mA	V_{SS} + 1		V_{DD} - 1	V
DC CMRR	CMRR			68		dB
DC PSRR	PSRR			70		dB
TIMING CHARACTERISTICS (digital) (Note 5, Figure 3)						
SCLK Clock Frequency	f_{CLK}		0		10	MHz
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		10			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CSO}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns
POWER SUPPLIES						
Positive Analog Supply Voltage	V_{DD}		0		31.5	V
Negative Analog Supply Voltage	V_{SS}		-28.8		0	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +15V, V_{SS} = -15V, V_{CC} = +5V, V_H = V_{DD}, V_L = V_{SS}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Separation	V_{DS}	V_{DD} - V_{SS}	9.0		31.5	V
Digital Supply Voltage	V_{CC}		2.70		5.25	V
Digital Supply to Negative Analog Supply Separation	V_{CS}	V_{CC} - V_{SS}	2.7		31.5	V
Power-On Reset Threshold	POR			1.6		V
Digital Supply Current	I_{CC}	(Note 4)		30	50	µA
Positive Analog Supply Current	I_{DD}	MAX5436/MAX5438 $\overline{SHDN}$ = GND for MAX5437/MAX5439		30	60	µA
		$\overline{SHDN}$ = V_{CC}		105	215	
Negative Analog Supply Current	I_{SS}	MAX5436/MAX5438 $\overline{SHDN}$ = GND for MAX5437/MAX5439		55	110	µA
		$\overline{SHDN}$ = V_{CC}		130	250	

Note 1: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H = V_{DD} and L = V_{SS}. The wiper terminal is unloaded.

Note 2: The DNL and INL are measured with the potentiometer configured as a variable resistor. H is unconnected and L = V_{SS}. The wiper terminal is driven with a source current of 80µA for the 50kΩ configuration and 40µA for the 100kΩ configuration.

Note 3: The wiper resistance is measured assuming the source currents given in Note 2.

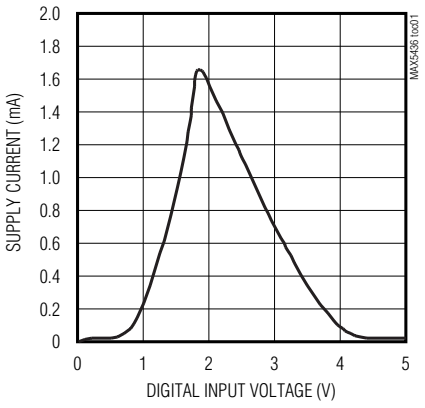
Note 4: The device draws current in excess of the specified supply current when the digital inputs are driven with voltages between (V_{CC} - 0.5V) and (GND + 0.5V). See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics* section.

Note 5: Guaranteed by design and characterization.

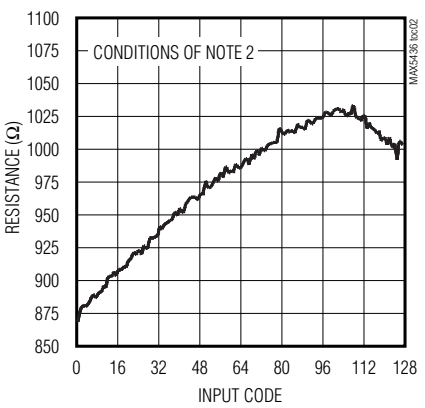
Typical Operating Characteristics

(V_{DD} = +15V, V_{SS} = -15V, V_{CC} = +5V, V_H = V_{DD}, V_L = V_{SS}, T_A = +25°C, unless otherwise noted.)

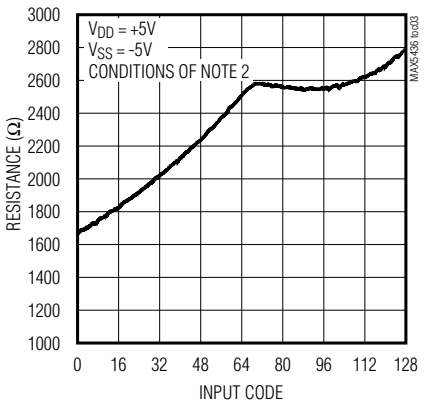
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



WIPER RESISTANCE vs. INPUT CODE



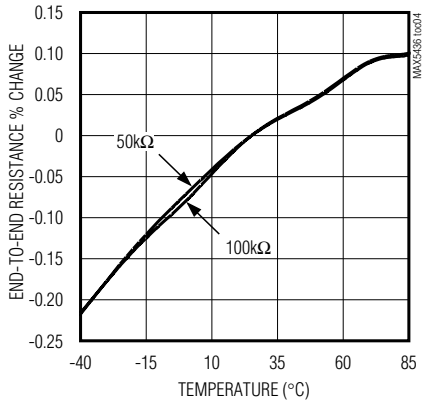
WIPER RESISTANCE vs. INPUT CODE



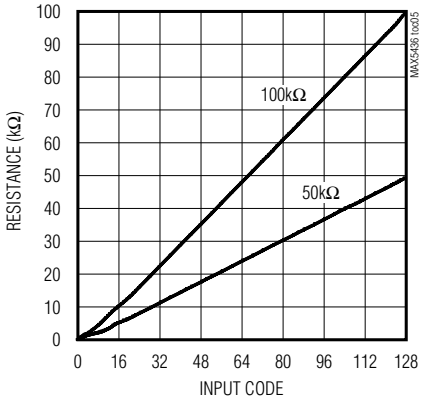
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V, V_{CC} = +5V, V_H = V_{DD}, V_L = V_{SS}, T_A = +25°C, unless otherwise noted.)

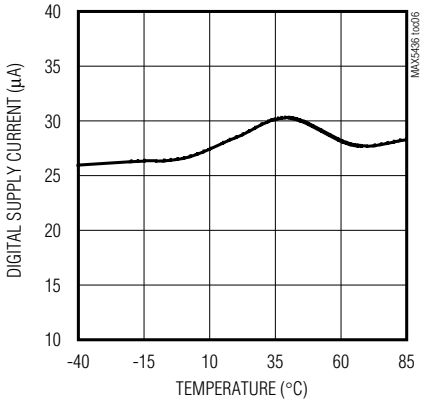
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



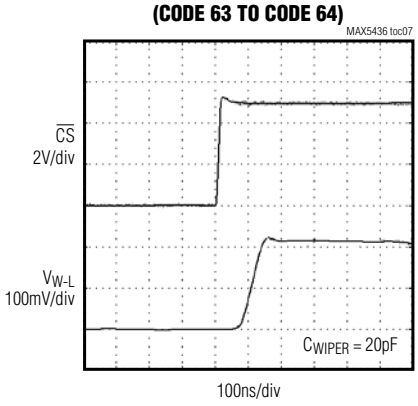
W-TO-L RESISTANCE CHANGE vs. INPUT CODE



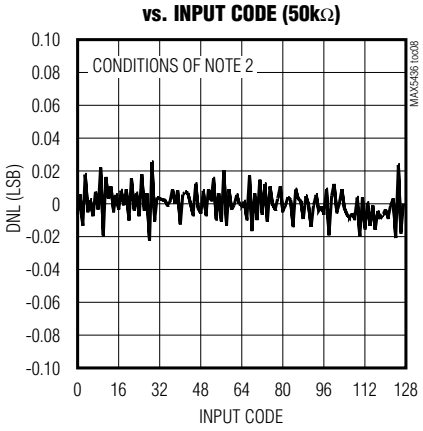
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



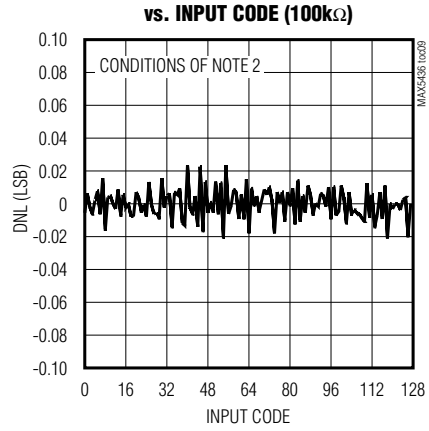
MIDSCALE SWITCHING TRANSIENT (CODE 63 TO CODE 64)



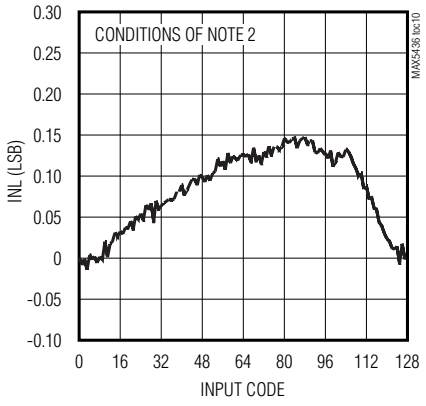
VARIABLE-RESISTOR DNL vs. INPUT CODE (50kΩ)



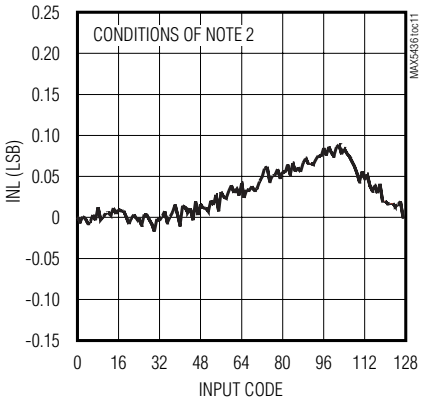
VARIABLE-RESISTOR DNL vs. INPUT CODE (100kΩ)



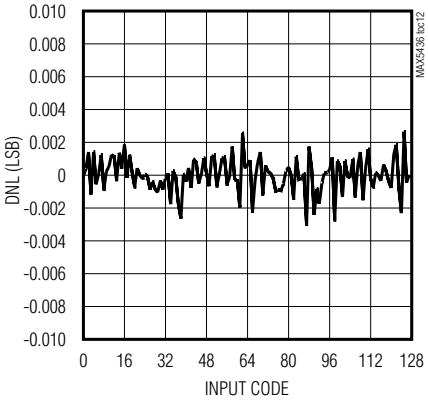
VARIABLE-RESISTOR INL vs. INPUT CODE (50kΩ)



VARIABLE-RESISTOR INL vs. INPUT CODE (100kΩ)



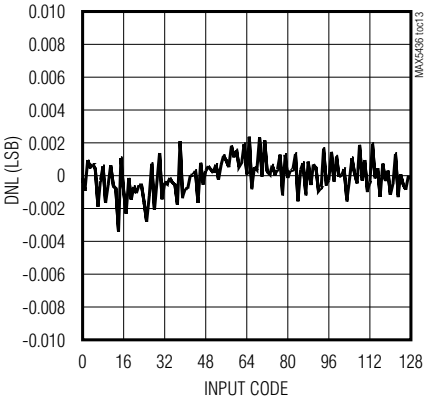
VOLTAGE-DIVIDER DNL vs. INPUT CODE (50kΩ)



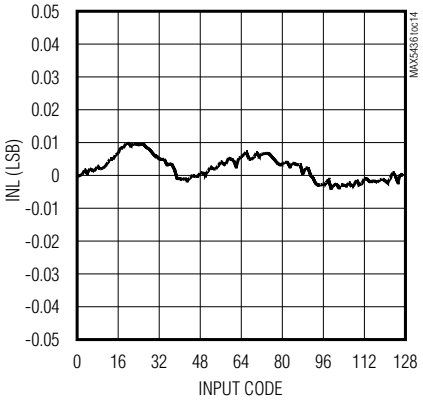
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V, V_{CC} = +5V, V_H = V_{DD}, V_L = V_{SS}, T_A = +25°C, unless otherwise noted.)

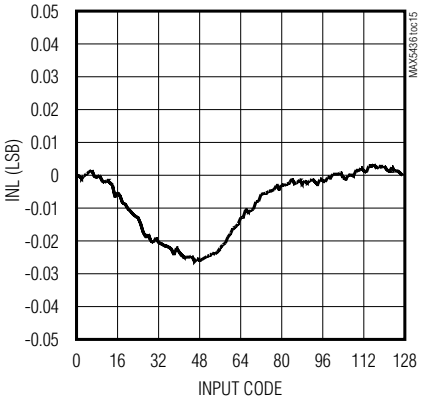
VOLTAGE-DIVIDER DNL vs. INPUT CODE (100kΩ)



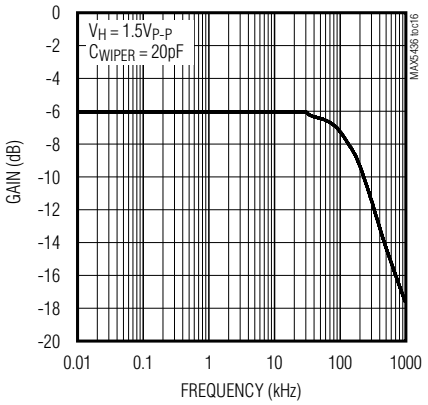
VOLTAGE-DIVIDER INL vs. INPUT CODE (50kΩ)



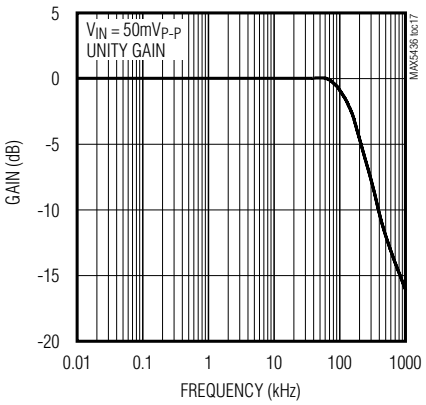
VOLTAGE-DIVIDER INL vs. INPUT CODE (100kΩ)



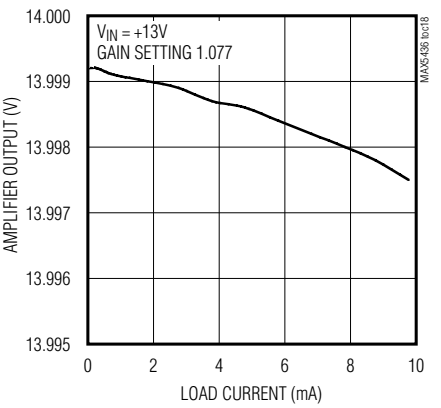
WIPER FREQUENCY RESPONSE AT MIDSCALE (100kΩ)



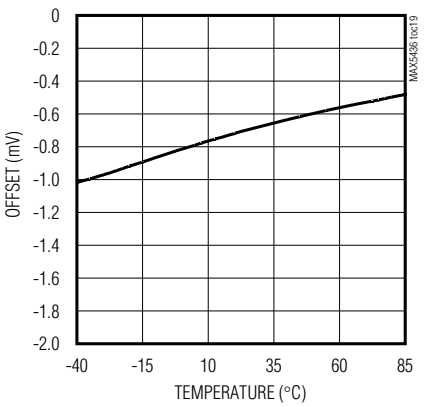
AMPLIFIER SMALL-SIGNAL FREQUENCY RESPONSE



AMPLIFIER OUTPUT vs. OUTPUT LOAD CURRENT



AMPLIFIER INPUT-REFERRED OFFSET vs. TEMPERATURE



Pin Description

PIN		NAME	DESCRIPTION
MAX5436/ MAX5438	MAX5437/ MAX5439		
1	1	SCLK	Serial Clock Input
2	2	DIN	Serial Data Input
3	3	$\overline{CS}$	Chip Select
—	4	$\overline{SHDN}$	Amplifier Shutdown
4	5	GND	Analog and Digital Ground
5	6	V_{SS}	Negative Analog Supply. Bypass with a 0.1µF capacitor to GND.
—	7	OUT	Amplifier Output
—	8	IN-	Amplifier Negative Input
—	9	IN+	Amplifier Positive Input
6	10	V_{DD}	Positive Analog Supply. Bypass with a 0.1µF capacitor to GND.
7	11	H	High Terminal of Resistor
8	12	W	Wiper Terminal of Resistor
9	13	L	Low Terminal of Resistor
10	14	V_{CC}	Digital Supply. Bypass with a 0.1µF capacitor to GND.

Detailed Description

Digital Interface Operation

The MAX5436–MAX5439 use a 3-wire SPI/QSPI/MICROWIRE-compatible serial data interface to control the wiper position. This write-only interface contains three inputs: chip select ($\overline{CS}$), data in (DIN), and serial clock (SCLK). When $\overline{CS}$ is taken low, data from DIN is synchronously loaded into the serial shift register on the rising edge of each SCLK pulse (Figure 2). The 8-bit data word requires 8 clock pulses to input the serial data. Note that the first bit of the data word, D7, is unused and should be ignored. Therefore, the second rising edge of SCLK loads the MSB. After all the data bits have been shifted in, they are latched into the potentiometer control register when $\overline{CS}$ transitions from low to high, the wiper position is then updated. Note that if $\overline{CS}$ is not kept low during the entire data stream, the data will be corrupted and the device will need to be reloaded.

Applications Information

Power-Up Sequencing

The MAX5436–MAX5439 have been designed so that any of the supplies can turn on first without causing any unwanted crowbar currents to flow. Note that both digital and analog supplies are required to power up the wiper and uncommitted amplifier (MAX5437/MAX5439 only).

Adjustable Gain Amplifier

The MAX5436/MAX5438 are used with the MAX427 to make a digitally adjustable gain circuit as shown in Figure 4. The normal feedback resistor is replaced with the MAX5436/MAX5438 in a variable-resistor configuration so that the gain of the circuit can be digitally controlled. The MAX5437/MAX5439 can use the internal high-voltage amplifier to make this digitally adjustable gain circuit.

LCD Biasing Control Applications

The MAX5436–MAX5439 are ideal for LCDs that require separate voltage for contrast control in addition to the main supply voltage. Figure 5a shows the MAX5436–MAX5439 being used for LCD contrast control along with the MAX629, which provides the LCD supply voltage. A similar circuit with an additional buffer circuit is shown in Figure 5b.

DATA WORD							
D7	D6	D5	D4	D3	D2	D1	D0
Don't Care	(MSB)						(LSB)
First Bit Loaded							**Last Bit Loaded**

Figure 1. Serial Data Format

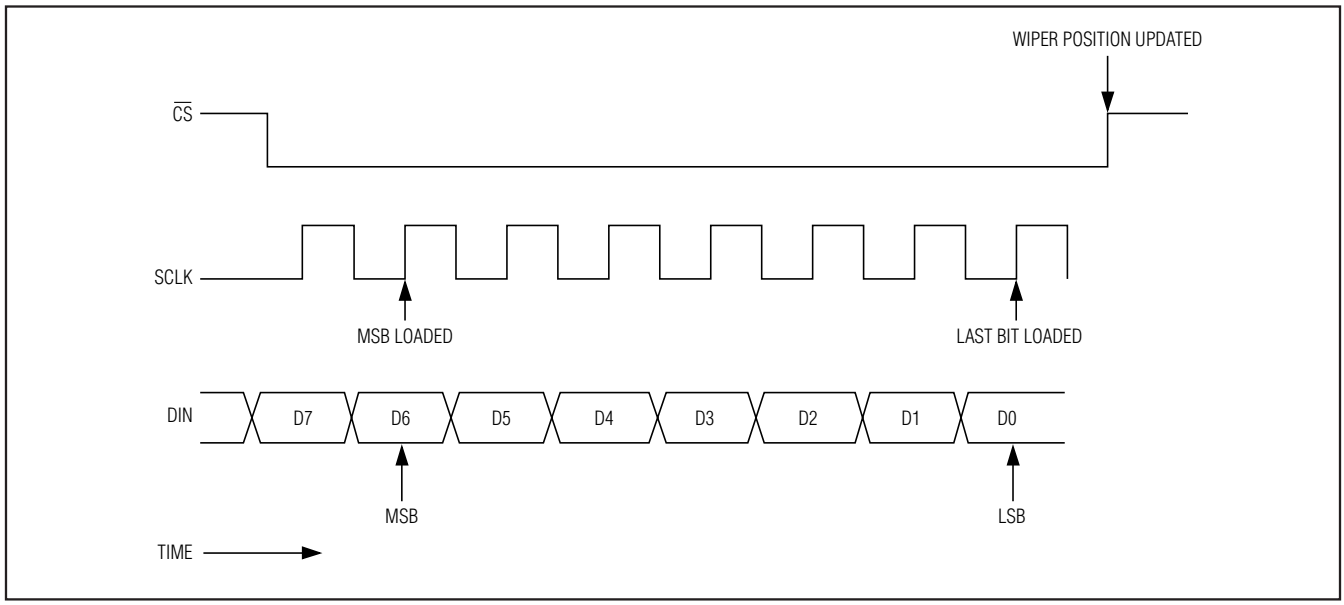


Figure 2. Serial Interface Timing Diagram

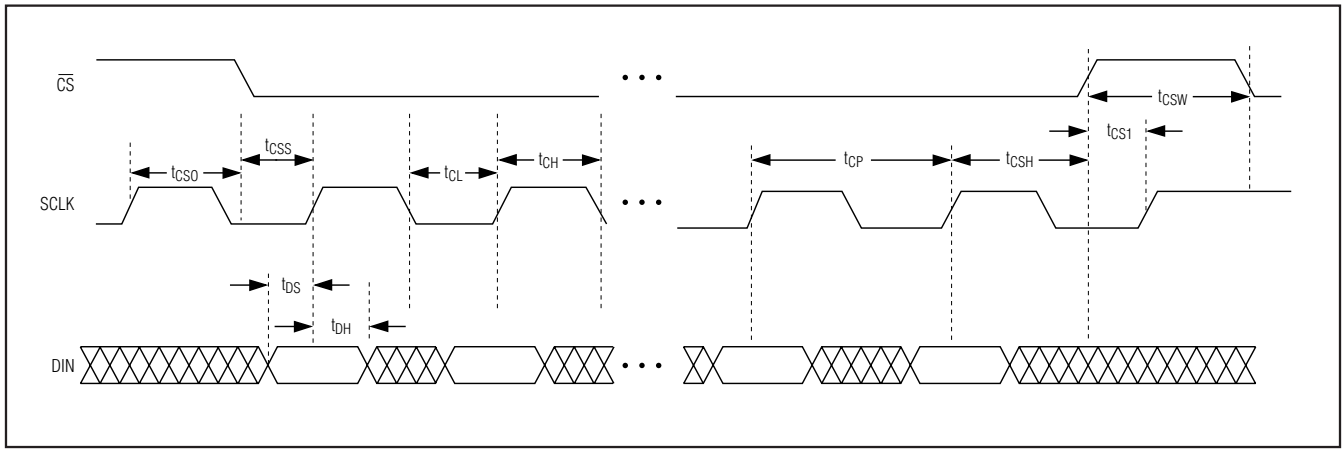


Figure 3. Detailed Serial-Interface Timing Diagram

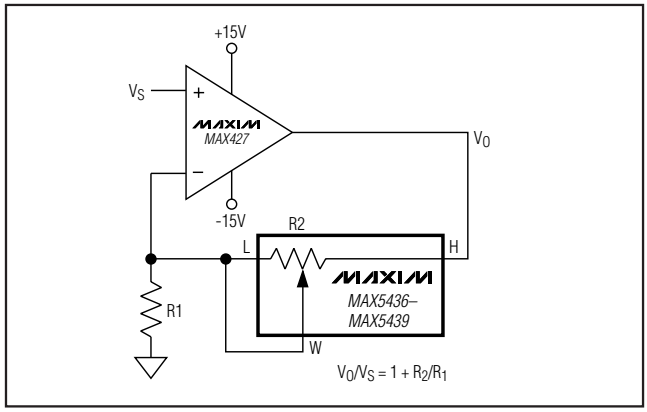


Figure 4. Noninverting Amplifier

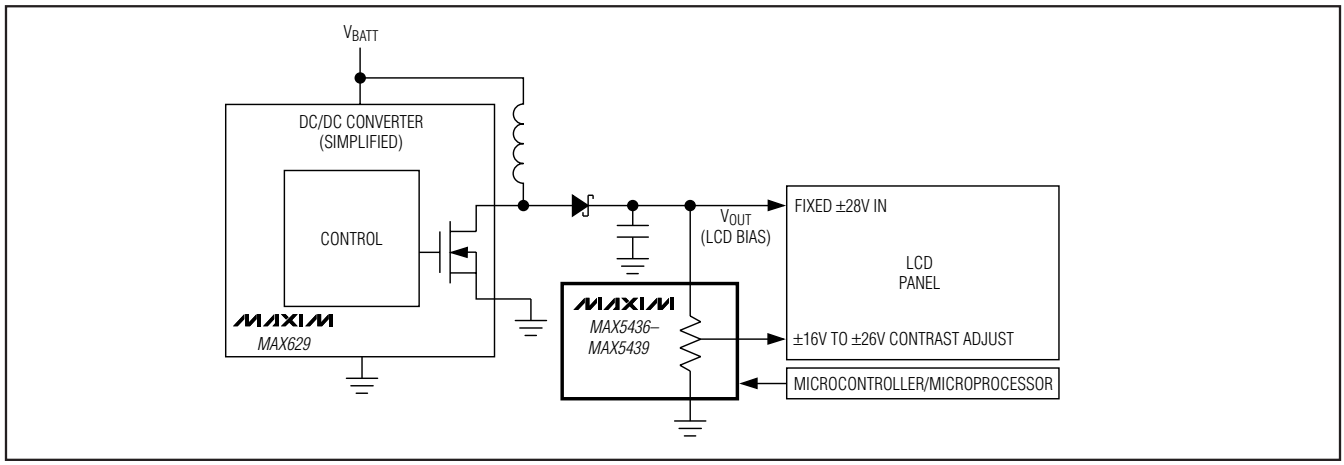


Figure 5a. Simplified LCD Contrast Control Circuit

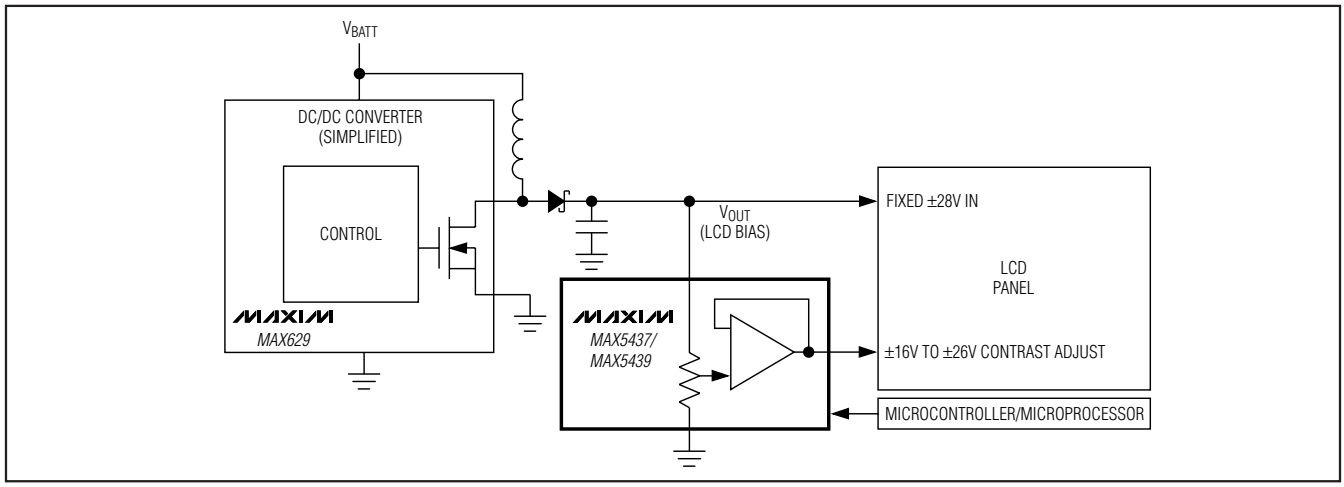
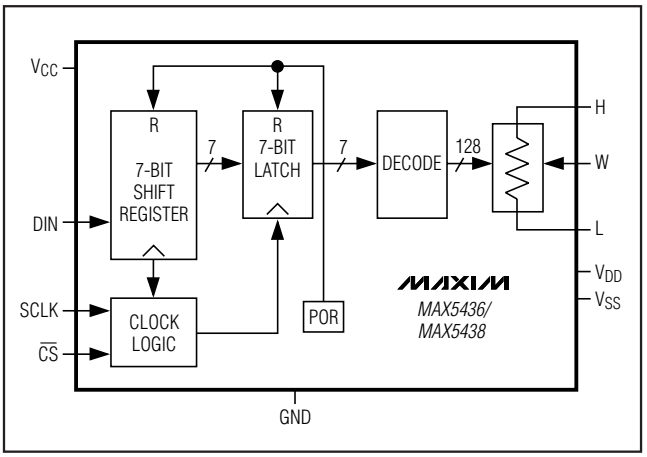
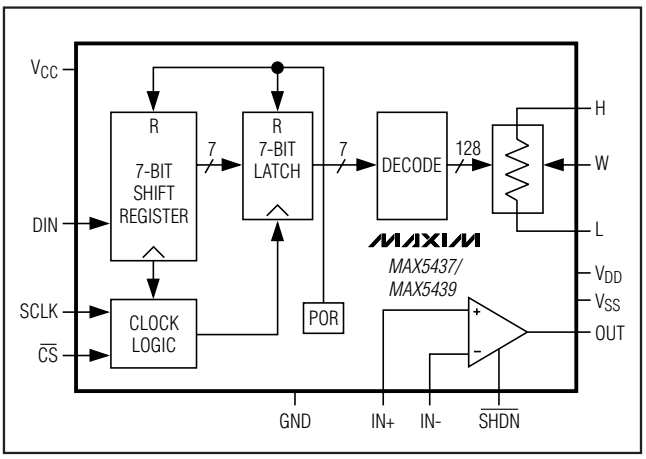


Figure 5b. Simplified LCD Contrast Control Circuit with Buffer

±15V, 128-Tap, Low-Drift Digital Potentiometers

Functional Diagrams





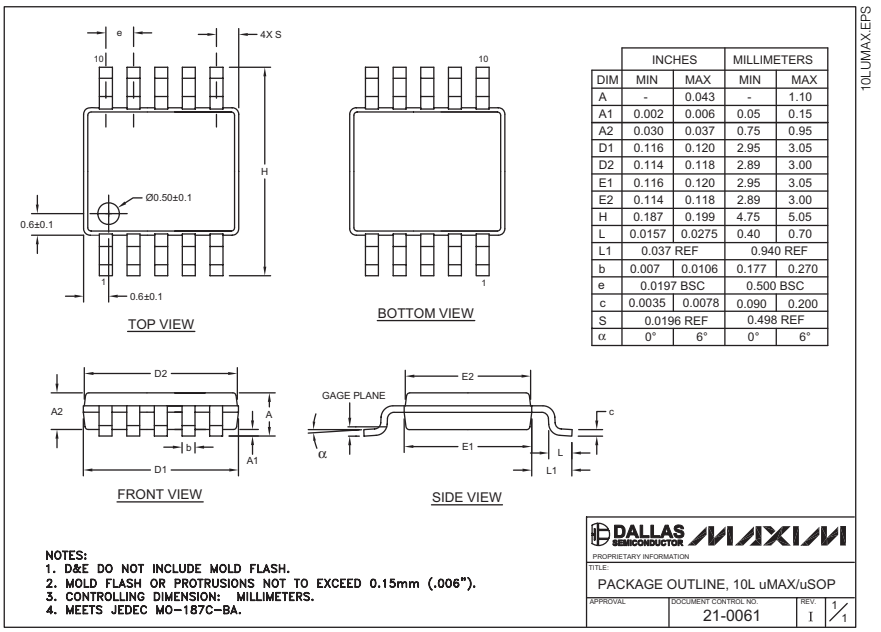
Chip Information

TRANSISTOR COUNT: 2556

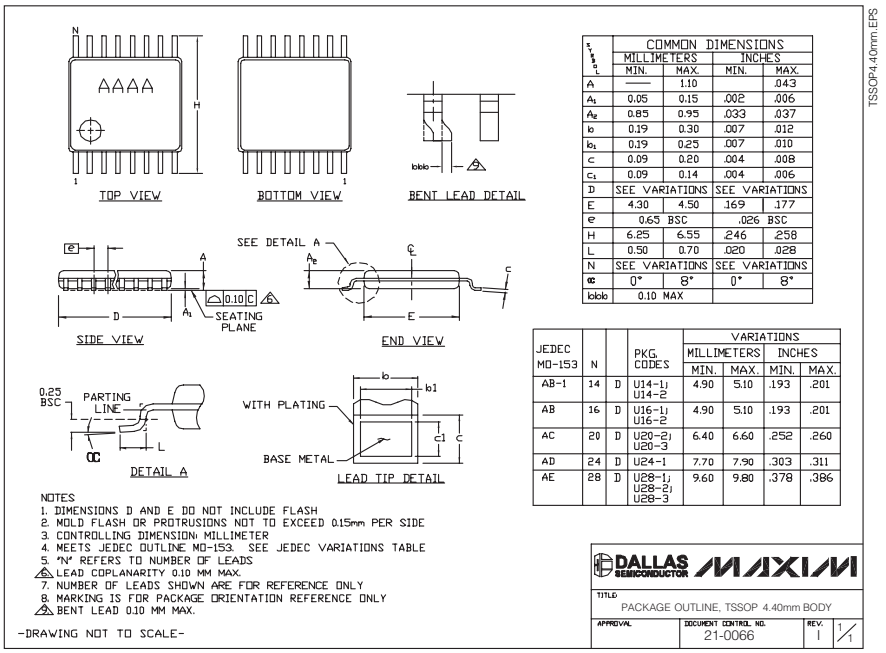
PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°



SYMBOL	COMMON DIMENSIONS MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

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