+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
DIN, DOUT, $\overline{CS}$, SCLK, $\overline{LDAC}$ to GND .....-0.3V to +6V
REF to GND .....-0.3V to (V_{DD} + 0.3V)
OUT_ to GND .....-0.3V to V_{DD}
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic QSOP (derate 8.3mW/°C about +70°C)...667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX5258)

(V_{DD} = +4.5V to +5.5V, V_{REF} = +4.096V, GND = 0, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution			8			Bits
Integral Nonlinearity (Note 1)	INL			±0.1	±1	LSB
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic (all codes)		±0.05	±1	LSB
Zero-Code Error	ZCE	Code = 0A hex		±2.5	±20	mV
Zero-Code Error Supply Rejection		Code = 0A hex		0.02	1	LSB
Zero-Code Temperature Coefficient		Code = 0A hex		±10		µV/°C
Full-Scale Error		Code = FF hex		±1	±30	mV
Full-Scale Error Supply Rejection		Code = FF hex		0.25	1	LSB
Full-Scale Temperature Coefficient		Code = FF hex		±10		µV/°C
REFERENCE INPUTS						
Input Voltage Range			0		V_{DD}	V
Input Resistance			161	230	300	kΩ
Input Capacitance				20		pF
DAC OUTPUTS						
Output Voltage Swing		R_L = 10kΩ to GND	0		V_{DD} - 0.3	V
Output Voltage Range		R_L = 10kΩ to GND	0		V_{REF}	V
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 × V_{DD}			V
Input Low Voltage	V_{IL}				0.3 × V_{DD}	V

ELECTRICAL CHARACTERISTICS (MAX5258) (continued)

(V_{DD} = +4.5V to +5.5V, V_{REF} = +4.096V, GND = 0, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	I_{IN}	V_{IN} = 0 to V_{DD}			±1.0	µA
Input Capacitance	C_{IN}	(Note 3)		10		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate		Code = FF hex		0.55		V/µs
Output Settling Time		To 1/2 LSB, from code 0A to code FF hex (Note 2)		10		µs
Digital Feedthrough		Code = 00 hex		0.15		nV-s
Digital-to-Analog Glitch Impulse		Code = 80 to code = 7F hex		30		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = $4V_{p-p}$ at 1kHz centered at 2.5V code = FF hex		68		dB
		V_{REF} = $4V_{p-p}$ at 10kHz centered at 2.5V code = FF hex		55		
Multiplying Bandwidth		V_{REF} = $0.1V_{p-p}$ centered at V_{DD}/2, -3dB bandwidth		700		kHz
Wideband Amplifier Noise				16		µV
POWER REQUIREMENTS						
Power-Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}			1.4	2.6	mA
Shutdown Supply Current	I_{SHDN}			0.45	10	µA

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

ELECTRICAL CHARACTERISTICS (MAX5259)

(V_{DD} = +2.7V to +3.3V, V_{REF} = +2.5V, GND = 0, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V, and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution			8			Bits
Integral Non Linearity (Note 1)	INL			±0.1	±1	LSB
Differential Non Linearity (Note 1)	DNL	Guaranteed monotonic (all codes)		±0.1	±1	LSB
Zero-Code Error	ZCE	Code = 0A hex		±2.5	±20	mV
Zero-Code Error Supply Rejection		Code = 0A hex.		0.15	1	LSB
Zero-Code Temperature Coefficient		Code = 0A hex		±10		µV/°C
Full-Scale Error		Code = FF hex		±0.7	±30	mV
Full-Scale Error Supply Rejection		Code = FF hex		0.2	1	LSB
Full-Scale Temperature Coefficient		Code = FF hex		±10		µV/°C
REFERENCE INPUTS						
Input Voltage Range			0		V_{DD}	V
Input Resistance			161	218	300	kΩ
Input Capacitance				20		pF
DAC OUTPUTS						
Output Voltage Swing		R_L = 10kΩto GND	0		V_{DD} – 0.3	V
Output Voltage Range		R_L = 10kΩ to GND	0		V_{REF}	V
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DD}			±1.0	µA
Input Capacitance	C_{IN}	(Note 3)		10		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.2mA	V_{DD} – 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate		Code = FF hex		0.55		V/µs
Output Settling Time		To 1/2 LSB, from code 0A to code FF hex (Note 2)		7		µs

ELECTRICAL CHARACTERISTICS (MAX5259) (continued)

(V_{DD} = +2.7V to +3.3V, V_{REF} = +2.5V, GND = 0, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V, and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Feedthrough		Code = 00 hex		0.1		nV-s
Digital-to-Analog Glitch Impulse		Code = 80 to code = 7F hex		20		nV-S
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 2.5V_{p-p} at 1kHz centered at 1.5V code = FF hex		65		dB
		V_{REF} = 2.5V_{p-p}at 10kHz centered at 1.5V code = FF hex		54		
Multiplying Bandwidth		V_{REF} = 0.1V_{p-p} centered at V_{DD}/2, -3dB bandwidth		700		kHz
Wideband Amplifier Noise				60		µV
POWER REQUIREMENTS						
Power-Supply Voltage	V_{DD}		2.7		3.6	V
Supply Current	I_{DD}			1.3	2.6	mA
Shutdown Supply Current	I_{SHDN}			0.24	10	µA

TIMING CHARACTERISTICS (MAX5258)

(V_{REF} = +4.096V, GND = 0, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Rise-to-$\overline{CS}$ Fall-Setup Time	t_{VDCS}			5		µs
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}		40	20		ns
$\overline{CS}$ Rise-to-$\overline{LDAC}$ Fall-Setup Time (Note 4)	t_{CLL}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		90			ns
SCLK Clock Frequency (Note 5)	f_{CLK}			10		MHz
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall-to-SCLK Rise-Setup Time	t_{CSS}		40			ns
SCLK Rise-to-$\overline{CS}$ Rise-Hold Time	t_{CSH}		0			ns
DIN to SCLK Rise-to-Setup Time	t_{DS}		40			ns
DIN to SCLK Rise-to-Hold Time	t_{DH}		0			ns
SCLK Rise-to-DOUT Valid Propagation Delay (Note 6)	t_{DO1}				200	ns
SCLK Fall-to-DOUT Valid Propagation Delay (Note 7)	t_{DO2}				210	ns
$\overline{CS}$ Rise-to-SCLK Rise-Setup Time	t_{CS1}		40			ns

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

TIMING CHARACTERISTICS (MAX5259)

(V_{REF} = +2.5V, GND = 0, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Rise-to-$\overline{CS}$ Fall-Setup Time	t_{VDCS}			5		µs
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}		40	20		ns
$\overline{CS}$ Rise-to-$\overline{LDAC}$ Fall-Setup Time (Note 4)	t_{CLL}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		90			ns
SCLK Clock Frequency (Note 5)	f_{CLK}			10		MHz
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall-to-SCLK Rise-Setup Time	t_{CSS}		40			ns
SCLK Rise-to-$\overline{CS}$ Rise-Hold Time	t_{CSH}		0			ns
DIN to SCLK Rise-to-Setup Time	t_{DS}		40			ns
DIN to SCLK Rise-to-Hold Time	t_{DH}		0			ns
SCLK Rise-to-DOUT Valid Propagation Delay (Note 6)	t_{DO1}				200	ns
SCLK Fall-to-DOUT Valid Propagation Delay (Note 7)	t_{DO2}				210	ns
$\overline{CS}$ Rise-to-SCLK Rise-Setup Time	t_{CS1}		40			ns

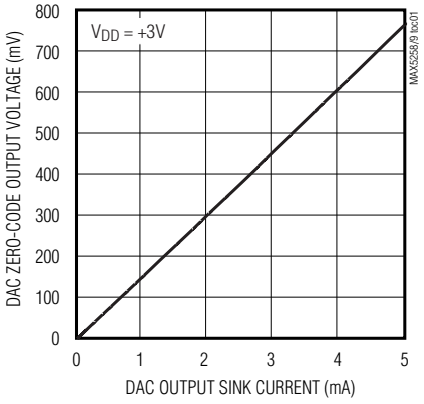
Note 1: INL and DNL are measured with R_L referenced to ground. Nonlinearity is measured from the first code that is greater than or equal to the maximum offset specification to code FF hex (full scale). (See *DAC Linearity and Voltage Offset* section.)
Note 2: Output settling time is measured from the 50% point of the rising edge of $\overline{CS}$ to 1/2LSB of the final value of V_{OUT}.
Note 3: Guaranteed by design, not production tested.
Note 4: If $\overline{LDAC}$ is activated prior to the rising edge of $\overline{CS}$, it must remain low for t_{LDAC} or longer after $\overline{CS}$ goes high.
Note 5: When DOUT is not used. If DOUT is used, f_{CLK} (max) is 4MHz due to SCLK to DOUT propagation delay.
Note 6: Serial data is clocked-out at SCLK's rising edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).
Note 7: Serial data is clocked-out at SCLK's falling edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

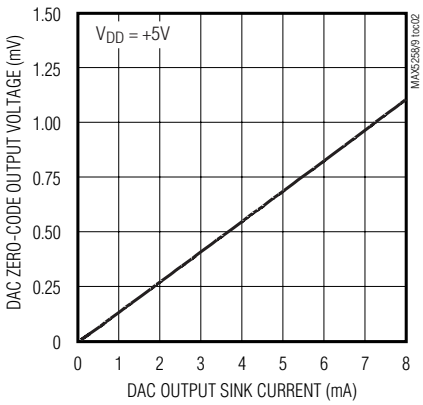
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

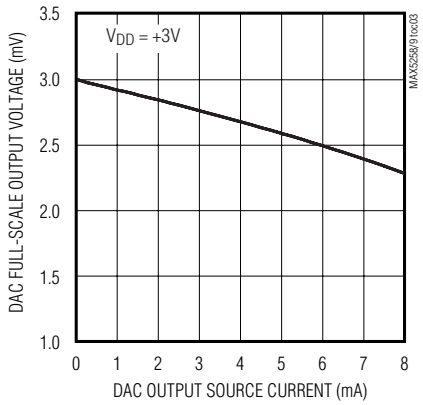
DAC ZERO-CODE OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



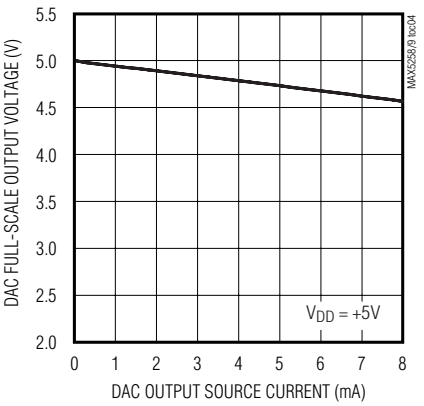
DAC ZERO-CODE OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



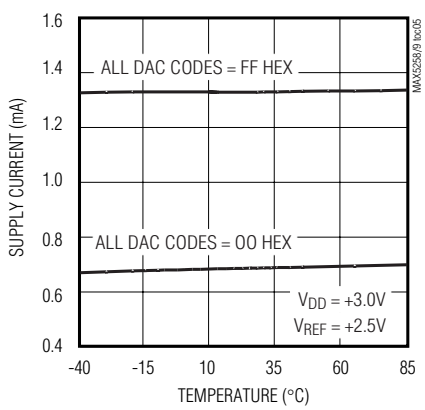
DAC FULL-SCALE OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



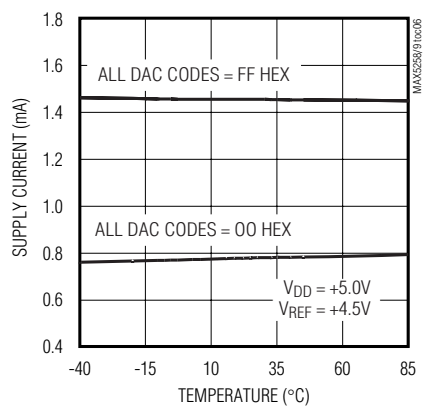
DAC FULL-SCALE OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



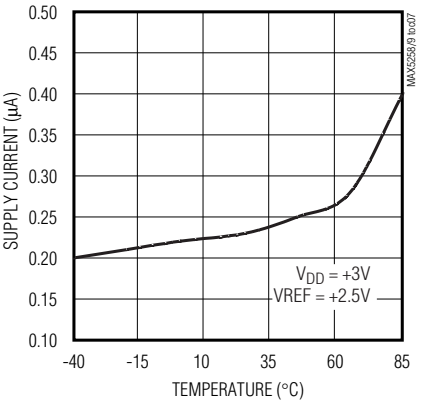
SUPPLY CURRENT vs. TEMPERATURE



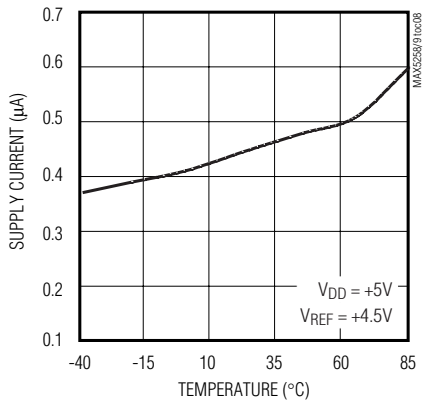
SUPPLY CURRENT vs. TEMPERATURE



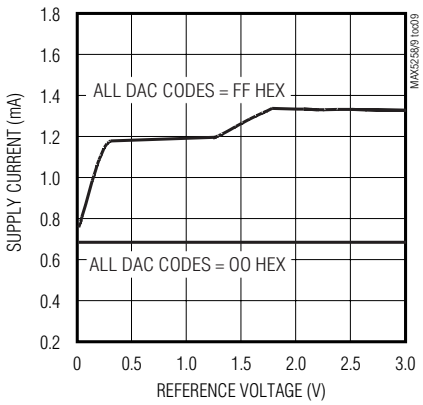
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. REFERENCE VOLTAGE (V_{DD} = +3V)

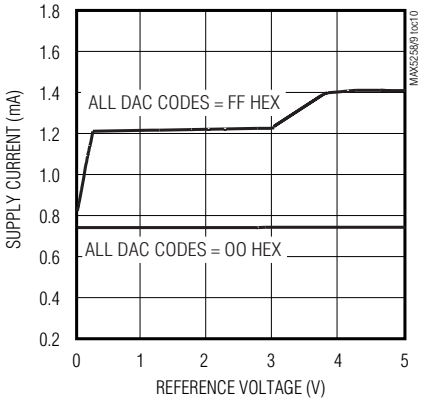


+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

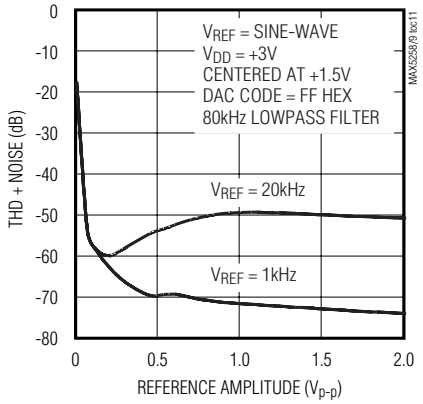
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

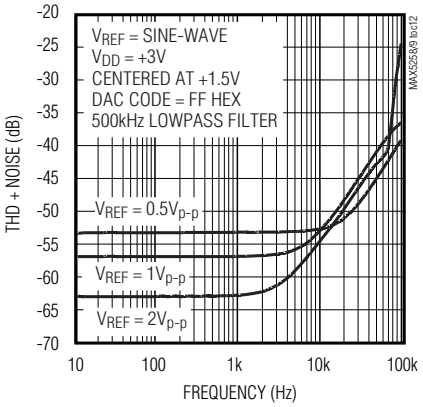
SUPPLY CURRENT vs. REFERENCE VOLTAGE (V_{DD} = +5V)



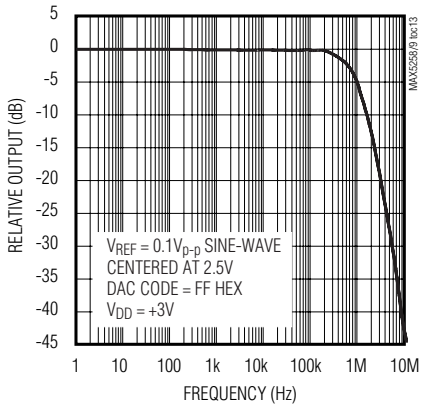
THD + NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



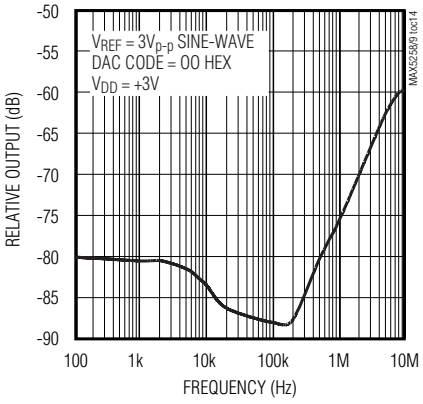
THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



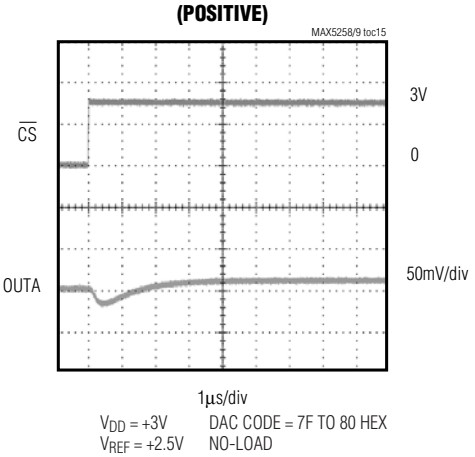
REFERENCE INPUT FREQUENCY RESPONSE



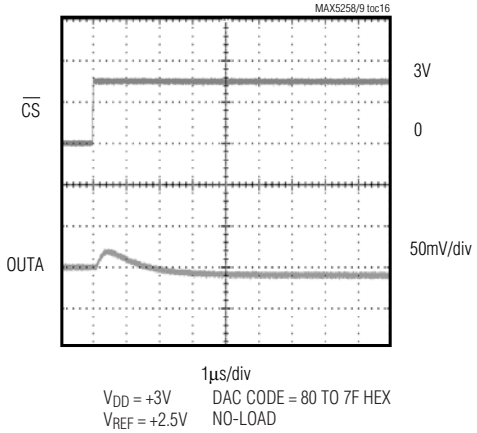
REFERENCE FEEDTHROUGH vs. FREQUENCY



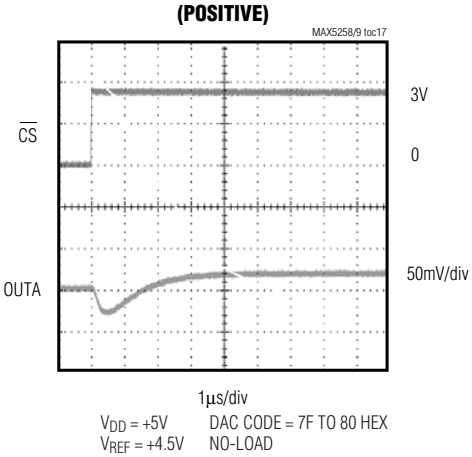
WORST-CASE 1LSB DIGITAL STEP CHANGE (POSITIVE)



WORST-CASE 1LSB DIGITAL STEP CHANGE (NEGATIVE)



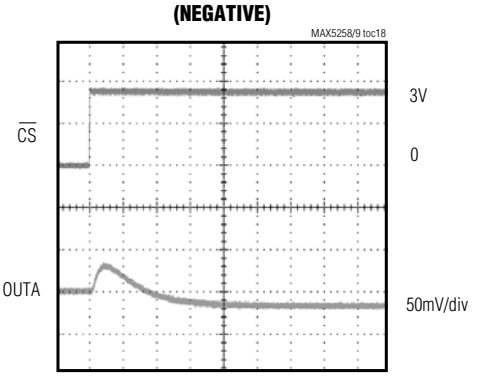
WORST-CASE 1LSB DIGITAL STEP CHANGE (POSITIVE)



Typical Operating Characteristics (continued)

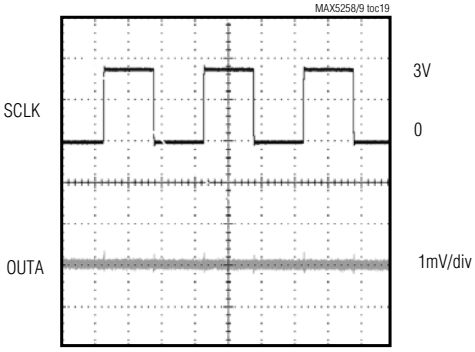
(T_A = +25°C, unless otherwise noted.)

WORST-CASE 1LSB DIGITAL STEP CHANGE (NEGATIVE)



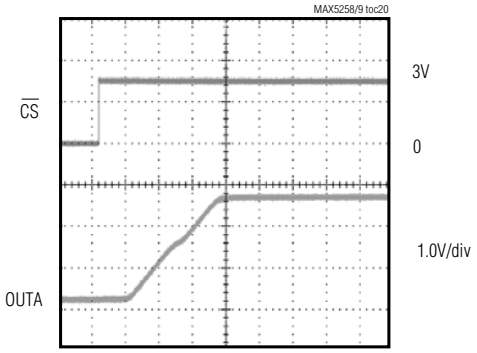
1µs/div
V_{DD} = +5V DAC CODE = 80 TO 7F HEX
V_{REF} = +4.5V NO-LOAD

CLOCK FEEDTHROUGH



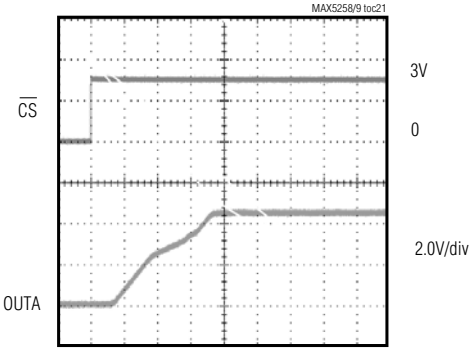
1µs/div
V_{DD} = +3V DAC CODE = 00 HEX
V_{REF} = +2.5V NO-LOAD
SCLK = 333 kHz

POSITIVE SETTLING TIME



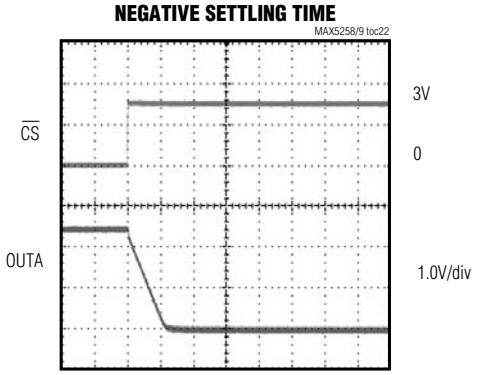
2µs/div
V_{DD} = +3V DAC CODE = 00 TO FF HEX
V_{REF} = +2.5V NO-LOAD

POSITIVE SETTLING TIME



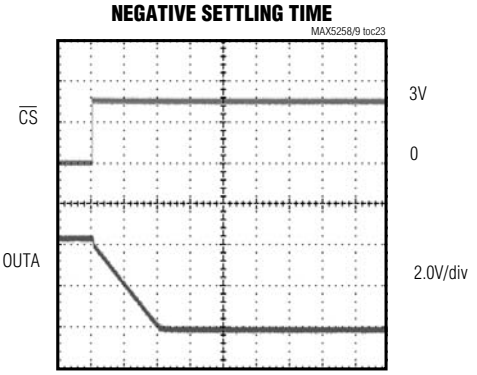
4µs/div
V_{DD} = +5V DAC CODE = 00 TO FF HEX
V_{REF} = +4.5V NO-LOAD

NEGATIVE SETTLING TIME



4µs/div
V_{DD} = +3V DAC CODE = FF TO 00 HEX
V_{REF} = +2.5V NO-LOAD

NEGATIVE SETTLING TIME



4µs/div
V_{DD} = +5V DAC CODE = FF TO 00 HEX
V_{REF} = +4.5V NO-LOAD

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

Pin Description

PIN	NAME	FUNCTION
1	OUTB	DAC B Voltage Output
2	OUTA	DAC A Voltage Output
3	GND	Ground
4	V_{DD}	Power Supply
5	REF	Reference Voltage Input
6	$\overline{LDAC}$	Load DAC Input. Driving this asynchronous input low transfers the contents of each input register to its respective DAC registers.
7	OUTE	DAC E Voltage Output
8	OUTF	DAC F Voltage Output
9	OUTG	DAC G Voltage Output
10	OUTH	DAC H Voltage Output
11	$\overline{CS}$	Chip Select Input. Data is shifted in and out when $\overline{CS}$ is low. Programming commands are executed when $\overline{CS}$ returns high.
12	SCLK	Serial Clock Input. Data is clocked in on the rising edge and clocked out on the falling edge (default) or rising edge (A2 = 1; see Table 1).
13	DIN	Serial Data Input. Data is clocked in on the rising edge of SCLK.
14	DOUT	Serial Data Output. Sinks and sources current. Data at DOUT can be clocked out on the falling edge (mode 0) or rising edge (mode 1) of SCLK (Table 1).
15	OUTD	DAC D Voltage Output
16	OUTC	DAC C Voltage Output

Detailed Description

Serial Interface

At power-on, the serial interface and all DACs are cleared and set to code zero. The serial data output (DOUT) is set to transition on SCLK's falling edge.

The MAX5258/MAX5259 communicate with microprocessors (µPs) through a synchronous, 3-wire interface (Figure 1). Data is sent MSB first and can be transmitted in two 4-bit and one 8-bit (byte) packets, or one 16-bit word. The first two bits are ignored. A 4-wire interface adds a line for $\overline{LDAC}$, allowing asynchronous updating. Data is transmitted and received simultaneously.

Figure 2 shows the detailed serial-interface timing. Note that the clock should be low if it is stopped between updates. DOUT does not go into a high-impedance state if the clock idles or $\overline{CS}$ is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. Data at DOUT is clocked out 16 clock cycles later, either at SCLK's falling edge (default or mode 0) or rising edge (mode 1).

$\overline{CS}$ must be low to enable the device. If $\overline{CS}$ is high, the interface is disabled and DOUT remains unchanged. $\overline{CS}$ must go low at least 40ns before the first rising edge of the clock pulse to properly clock in the first bit. With $\overline{CS}$ low, data is clocked into the MAX5258/MAX5259's internal shift register on the rising edge of the external serial clock. Always clock in the full 16 bits.

Serial Input Data Format and Control Codes

The 16-bit serial input format, shown in Figure 3, comprises two "don't care" bits, three DAC address bits (A2, A1, A0), three control bits (C2, C1, C0), and eight data bits (D7…D0). The 6-bit address/control code configures the DAC as shown in Table 1.

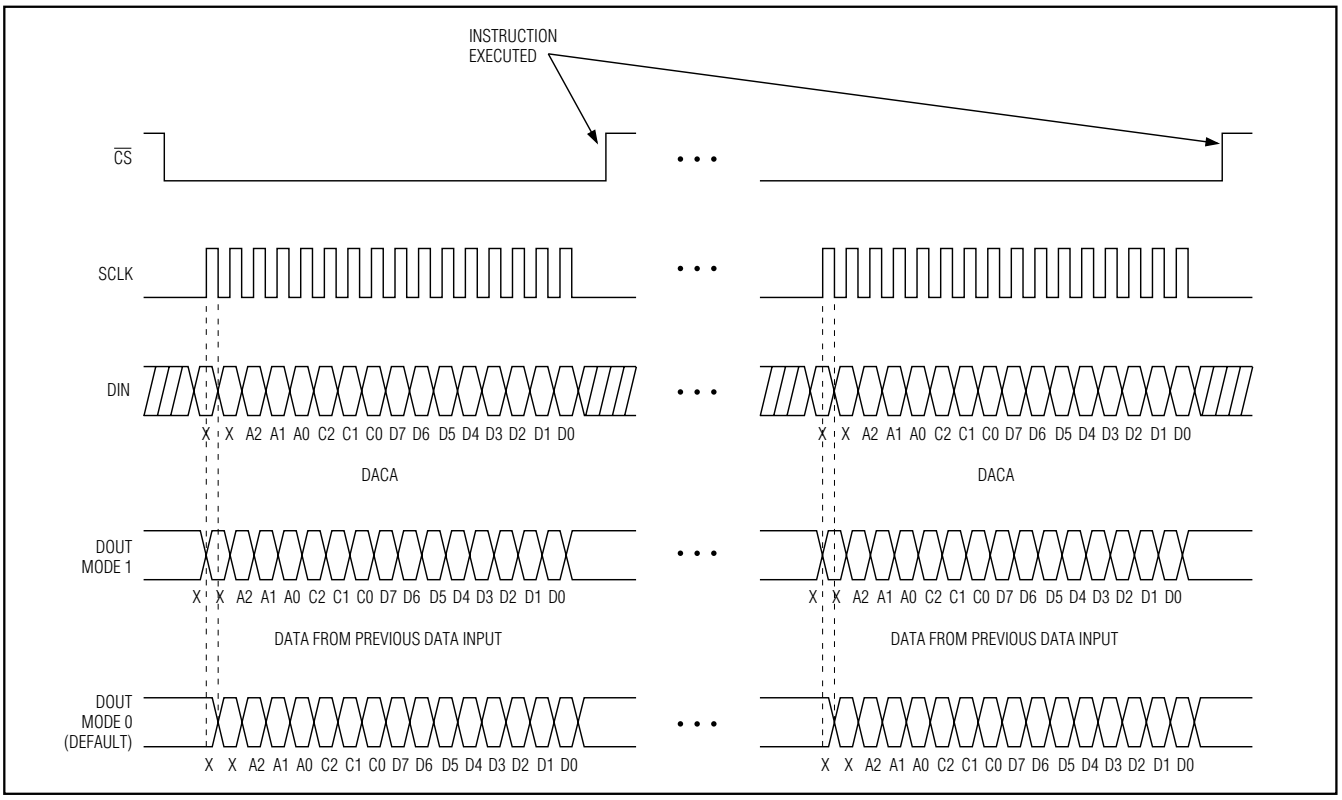


Figure 1. 3-Wire Interface Timing

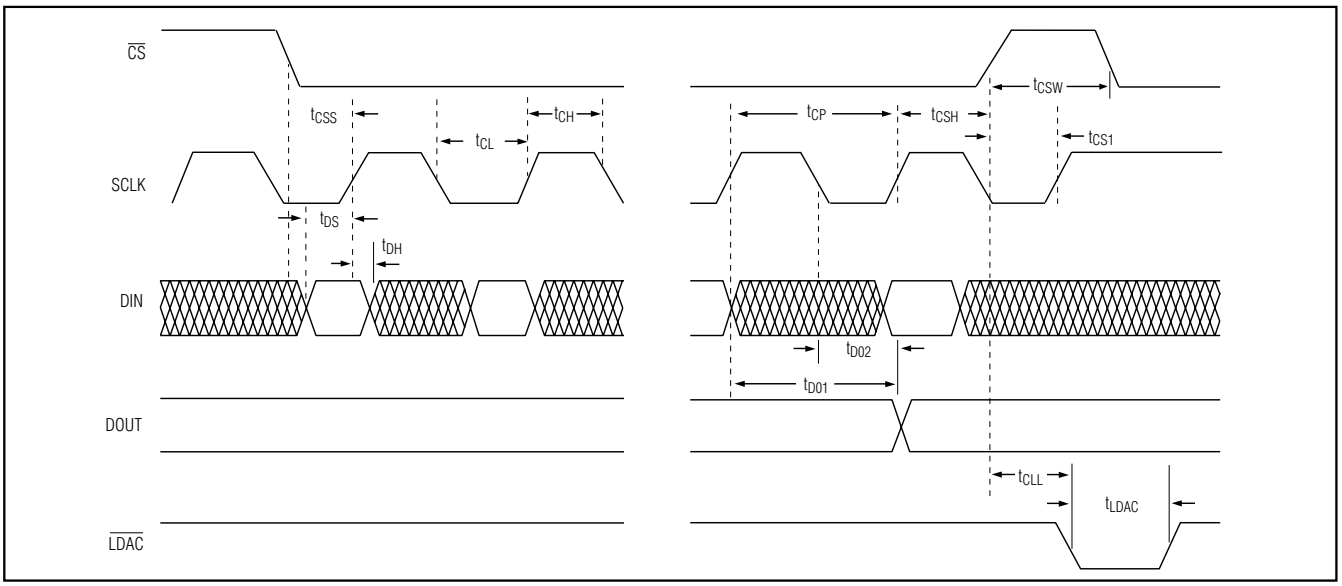


Figure 2. Detailed Serial-Interface Timing Diagram

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD*							$\overline{\text{LDAC}}$	FUNCTION
A2	A1	A0	C2	C1	C0	D7……D0		
X	X	X	0	0	0	XXXXXXXX	X	No operation (NOP); shift data in shift registers.
X	X	X	0	0	1	XXXXXXXX	X	Clears all input and DAC registers and sets all DAC outputs to zero.
X	X	X	0	1	0	XXXXXXXX	X	Software shutdown. Output buffers can be individually shut down with zeros in the corresponding data bits.
0	X	X	0	1	1	XXXXXXXX	X	DOUT Phase Mode 0. DOUT transitions on the falling edge of SCLK.
1	X	X	0	1	1	XXXXXXXX	X	DOUT Phase Mode 1. DOUT transitions on the rising edge of SCLK.
X	X	X	1	0	0	8-bit DAC data	X	Loads all DACs with the same data
0	0	0	1	0	1	8-bit DAC data	H	Load input register A. All DAC outputs unchanged.
0	0	1	1	0	1	8-bit DAC data	H	Load input register B. All DAC outputs unchanged.
0	1	0	1	0	1	8-bit DAC data	H	Load input register C. All DAC outputs unchanged.
0	1	1	1	0	1	8-bit DAC data	H	Load input register D. All DAC outputs unchanged.
1	0	0	1	0	1	8-bit DAC data	H	Load input register E. All DAC outputs unchanged.
1	0	1	1	0	1	8-bit DAC data	H	Load input register F. All DAC outputs unchanged.
1	1	0	1	0	1	8-bit DAC data	H	Load input register G. All DAC outputs unchanged.
1	1	1	1	0	1	8-bit DAC data	H	Load input register H. All DAC outputs unchanged.
0	0	0	1	1	0	8-bit DAC data	H	Load input register A. Update OUTA. All other DAC outputs unchanged.
0	0	1	1	1	0	8-bit DAC data	H	Load input register B. Update OUTB. All other DAC outputs unchanged.
0	1	0	1	1	0	8-bit DAC data	H	Load input register C. Update OUTC. All other DAC outputs unchanged.
0	1	1	1	1	0	8-bit DAC data	H	Load input register D. Update OUTD. All other DAC outputs unchanged.
1	0	0	1	1	0	8-bit DAC data	H	Load input register E. Update OUTE. All other DAC outputs unchanged.
1	0	1	1	1	0	8-bit DAC data	H	Load input register F. Update OUTF. All other DAC outputs unchanged.
1	1	0	1	1	0	8-bit DAC data	H	Load input register G. Update OUTG. All other DAC outputs unchanged.
1	1	1	1	1	0	8-bit DAC data	H	Load input register H. Update OUTH. All other DAC outputs unchanged.
X	X	X	1	1	1	XXXXXXXX	H	Software LDAC command. Updates all DACs from their respective input registers.

** The first two bits are "don't care."*

No Operation (NOP)

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care			0	0	0	Don't Care							

($\overline{LDAC}$ = X)

The no-operation (NOP) command allows data to be shifted through the MAX5258/MAX5259 shift register without affecting the input or DAC registers. This is useful in daisy-chaining (see the *Daisy-Chaining Devices* section). For this command, the data bits are "Don't Cares." As an example, three MAX5258s are daisy-chained (A, B, and C), and devices A and C need to be updated. The 48-bit-wide command would consist of one 16-bit word for device C, followed by an NOP instruction for device B and a third 16-bit word with data for device A. At the rising edge of $\overline{CS}$, device B will not change state.

Clear

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care			0	0	1	Don't Care							

($\overline{LDAC}$ = X)

The clear command clears all input and DAC registers and sets all DAC outputs to zero. This command brings the DAC out of shutdown.

Software Shutdown

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care			0	1	0	8-Bit Data							

($\overline{LDAC}$ = X)

Shuts down all output buffer amplifiers and voltage references. Output buffers can be individually disabled with the corresponding zeros in the data bits (D7-D0). If all data bits are zero, only the power-on reset circuit is active, and the device draws 10µA (max). There are four ways to bring the device out of shutdown: POR, CLEAR, LOAD SAME DATA, LOAD INPUT, AND DAC REGISTERS.

Set DOUT Phase—SCLK Falling (Mode 0, Default)

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	X	X	0	1	1	8-Bit Data							

($\overline{LDAC}$ = X)

This command sets DOUT to transition at the falling edge of SCLK. The same command also updates all DAC registers with the contents of their respective input registers, identical to the $\overline{LDAC}$ command. This is the default mode on power-up.

Set DOUT Phase—SCLK Rising (Mode 1)

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	X	X	0	1	1	8-Bit Data							

($\overline{LDAC}$ = X)

Mode 1 sets the serial output DOUT to transition at the rising edge of SCLK. Once this command is issued, DOUT's phase is latched and will not change except on power-up or if the specific command to set the phase to falling edge is issued.

This command also loads all DAC registers with the contents of their respective input registers, and is identical to the $\overline{LDAC}$ command.

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

Load All DACs with Shift-Register Data

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care			1	0	0	8-Bit Data							

($\overline{LDAC}$ = X)

All eight DAC registers are updated with shift-register data. This command allows all DACs to be set to any analog value within the reference range. This command can be used to substitute CLEAR if code 00 (hex) is programmed, which clears all DACs. This command brings the device out of shutdown.

Load Input Register, DAC Registers Unchanged (Single Update Operation)

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address			1	0	1	8-Bit Data							

($\overline{LDAC}$ = X)

When performing a single update operation, A2-A0 selects the respective input register. At the rising edge of $\overline{CS}$, the selected input register is loaded with the current shift-register data. All DAC outputs remain unchanged. This pre-loads individual data in the input register without changing the DAC outputs.

Load Input and DAC Registers

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address			1	1	0	8-Bit Data							

($\overline{LDAC}$ = X)

This command directly loads current shift-register data in the selected input and DAC registers at the rising edge of $\overline{CS}$. A2-A0 set the DAC address.

For example, to load all eight DAC registers simultaneously with individual settings, eight commands are required. First perform seven single input register update operations (C2 = 1, C1 = 0, C0 = 1) for DACs A, B, C, D, E, F, and G (C2 = 1, C1 = 0, C0 = 1). The final command loads input register H and updates all eight DAC registers from their respective input registers. This command brings the device out of shutdown.

Software "$\overline{LDAC}$" Command

A2	A1	A0	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address			1	1	1	8-Bit Data							

($\overline{LDAC}$ = X)

All DAC registers are updated with the contents of their respective input registers at the rising edge of $\overline{CS}$. This is a synchronous software command that performs the same function as the asynchronous $\overline{LDAC}$.

LDAC Operation (Hardware)

$\overline{LDAC}$ is typically used in 4-wire interfaces (Figure 4). This command is level sensitive, and it allows asynchronous hardware control of the DAC outputs. With $\overline{LDAC}$ low, all eight DAC registers are transparent, and any time an input register is updated, the DAC output immediately follows.

Serial Data Output

DOUT is the internal shift-register's output. DOUT can be programmed to clock out data on the falling edge of SCLK (mode 0) or the rising edge (mode 1). In mode 0, output data lags input data by 16.5 clock cycles, maintaining compatibility with MICROWIRE and SPI. In mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to mode 0 timing. DOUT never three-states; it always actively drives either high or low and remains unchanged when $\overline{CS}$ is high.

Interfacing to the Microprocessor

The MAX5258/MAX5259 are MICROWIRE (Figure 5) and SPI/QSPI (Figure 6) compatible. For SPI and QSPI, clear the CPOL and CPHA configuration bits (CPOL = CPHA = 0). The SPI/QSPI CPOL = CPHA = 1 configuration can also be used if the DOUT output is ignored.

The MAX5258/MAX5259 can interface with Intel's 80C5X/80C3X family in mode 0 if the SCLK clock polarity is inverted. Universally, if a serial port is not available, three lines from one of the parallel ports can be used for bit manipulation.

Digital feedthrough at the voltage outputs is greatly minimized by operating the serial clock only to update the registers. See the Clock Feedthrough photo in the *Typical Operating Characteristics* section. The clock idle state is low.

Daisy-Chaining Devices

Any number of MAX5258/MAX5259s can be daisy-chained by connecting DOUT of one device to DIN of the following device in the chain with all devices in mode zero. The NOP instruction (Table 1) allows data to be passed from DIN to DOUT without changing the input or DAC registers of the passing device. A 3-wire interface updates daisy-chained or individual MAX5258/MAX5259s simultaneously by bringing $\overline{CS}$ high (Figure 7).

Analog Section

DAC Operation

The MAX5258/MAX5259 use a matrix decoding architecture for the DACs, which saves power in the overall system. The external reference voltage is divided down by a resistor string placed in a matrix fashion. Row and column decoders select the appropriate tab from the resistor string to provide the needed analog voltages. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output. Figure 8 shows a simplified diagram of one of the eight DACs.

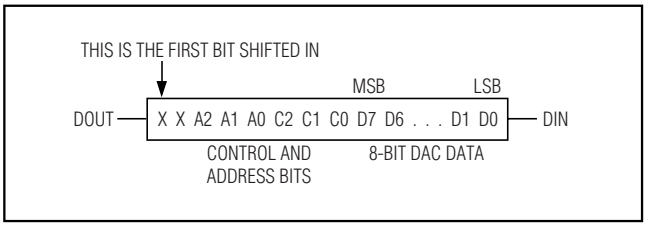


Figure 3. Serial Input Format

Reference Input

The voltage at REF sets the full-scale output voltage for all eight DACs. The 230kΩ typical input impedance at REF is code independent. The output voltage for any DAC can be represented by a digitally programmable voltage source as follows:

$$V_{OUT} = (NB \times V_{REF}) / 256,$$

where NB is the numerical value of the DAC's binary input code.

Output Buffer Amplifiers

All MAX5258/MAX5259 voltage outputs are internally buffered by precision unity-gain followers that slew at about 0.55V/µs. The outputs can swing from GND to V_{DD}. With a 0 to V_{REF} (or V_{REF} to 0) output transition, the amplifier outputs will typically settle to 1/2LSB in 10µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive (≥10kΩ) or capacitive (≤100pF) loads.

Applications Information

DAC Linearity and Voltage Offset

The output buffer can have a negative input offset voltage that would normally drive the output negative, but since there is no negative supply, the output remains at GND (Figure 9). When linearity is determined using the endpoint method, it is measured between code 10 (0A hex) and full-scale code (FF hex) after offset and gain error are calibrated out. With a single-supply, negative offset causes the output not to change with an input code transition near zero (Figure 9). Thus, the lowest code that produces a positive output is the lower endpoint.

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

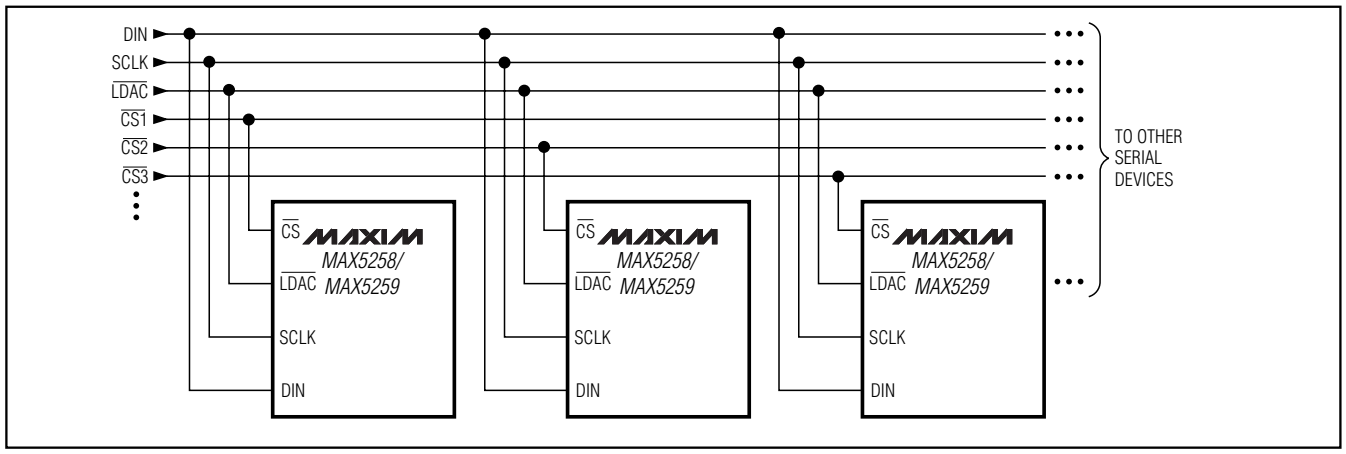


Figure 4. Multiple MAX5258's Sharing One DIN Line. (Simultaneously Update by Strobing $\overline{LDAC}$, or Specifically Update by Enabling an Individual $\overline{CS}$)

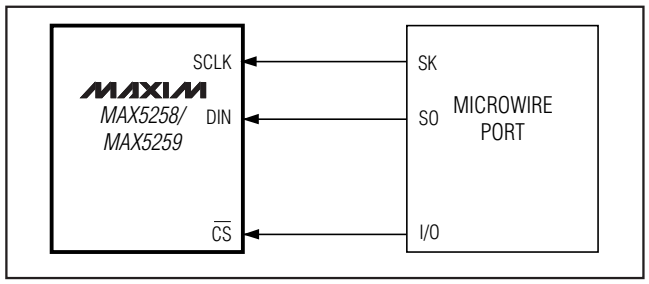


Figure 5. Connections for MICROWIRE

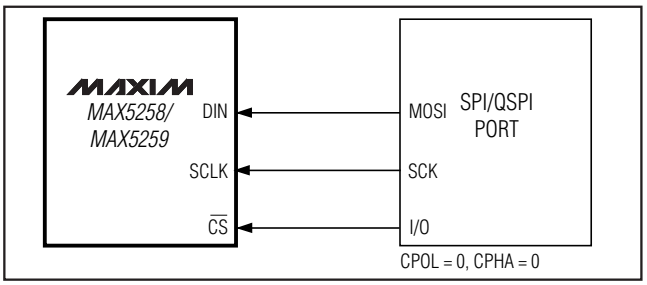


Figure 6. Connections for SPI/QSPI

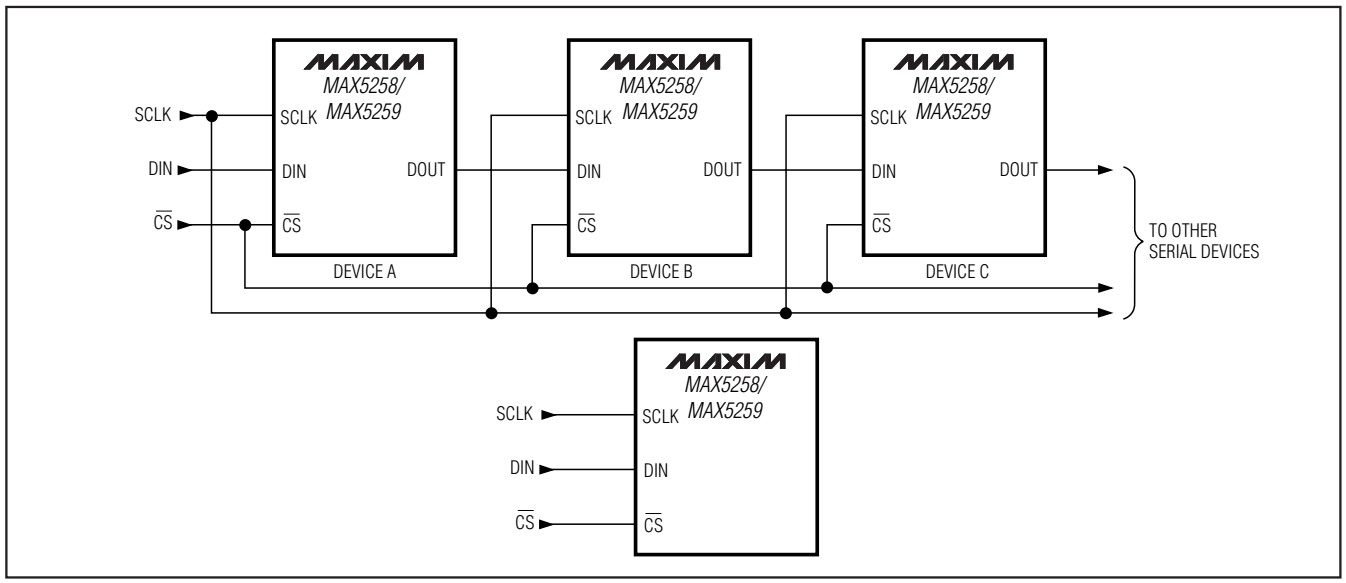


Figure 7. Daisy-Chained or Individual MAX5258s Simultaneously Updated by Bringing $\overline{CS}$ High (Only Three Wires Are Required)

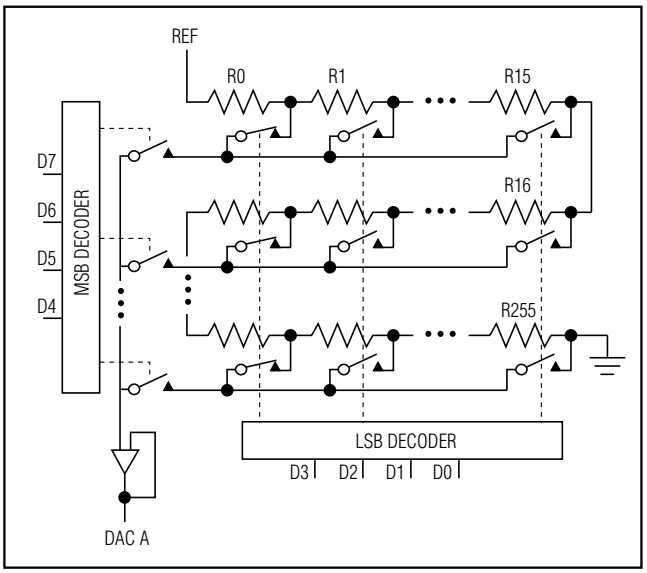


Figure 8. DAC Simplified Circuit Diagram

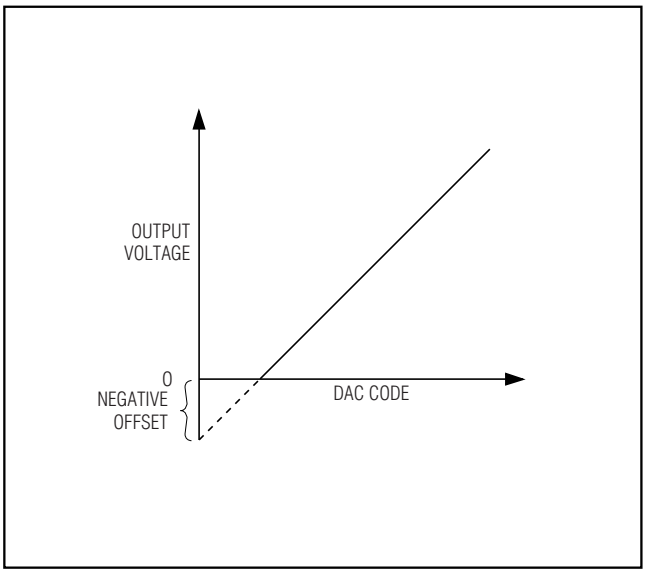


Figure 9. Effect of Negative Offset (Single Supply)

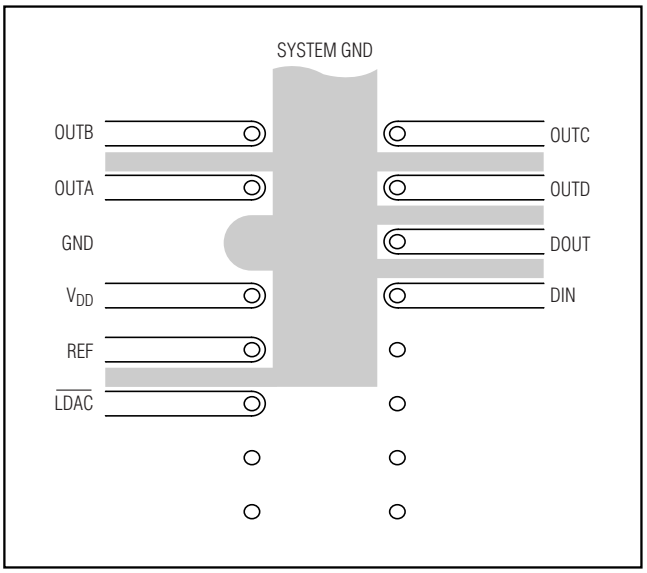


Figure 10. Suggested PC Board Layout for Minimizing Crosstalk (Bottom View)

Power Sequencing

The voltage applied to REF should not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REF and V_{DD} to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered-up.

Power-Supply Bypassing and Ground Management

Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and GND as possible. Careful PC board layout minimizes crosstalk among DAC outputs and digital inputs. Figure 10 shows suggested circuit board layout to minimize crosstalk.

Unipolar-Output, Two-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input are the same polarity. Figure 11 shows the MAX5258/MAX5259 unipolar configuration, and Table 2 shows the unipolar code.

+3V/+5V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

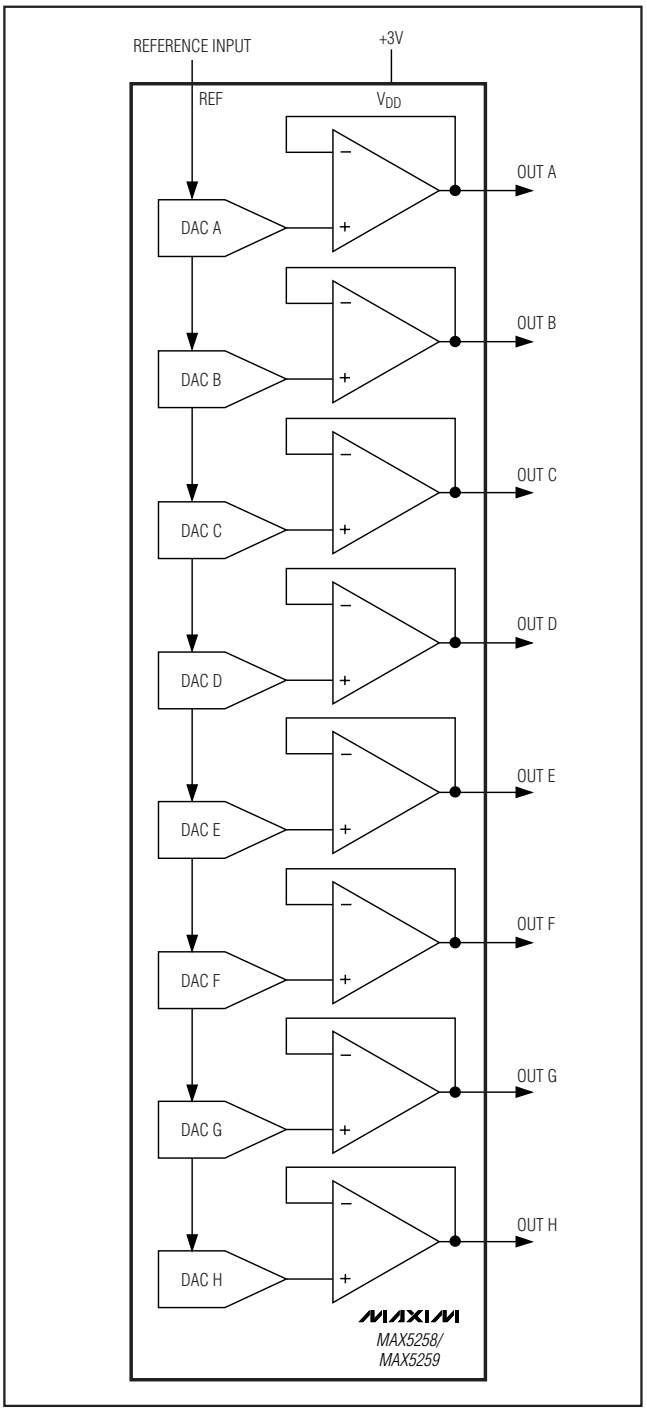


Figure 11. Unipolar Output Circuit

Table 2. Unipolar Code Table

DAC CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{REF}(255/256)$
1000	0001	$+V_{REF}(129/256)$
1000	0000	$+V_{REF}(128/256) = +V_{REF}/2$
0111	1111	$+V_{REF}(127/256)$
0000	0001	$+V_{REF}(1/256)$
0000	0000	0

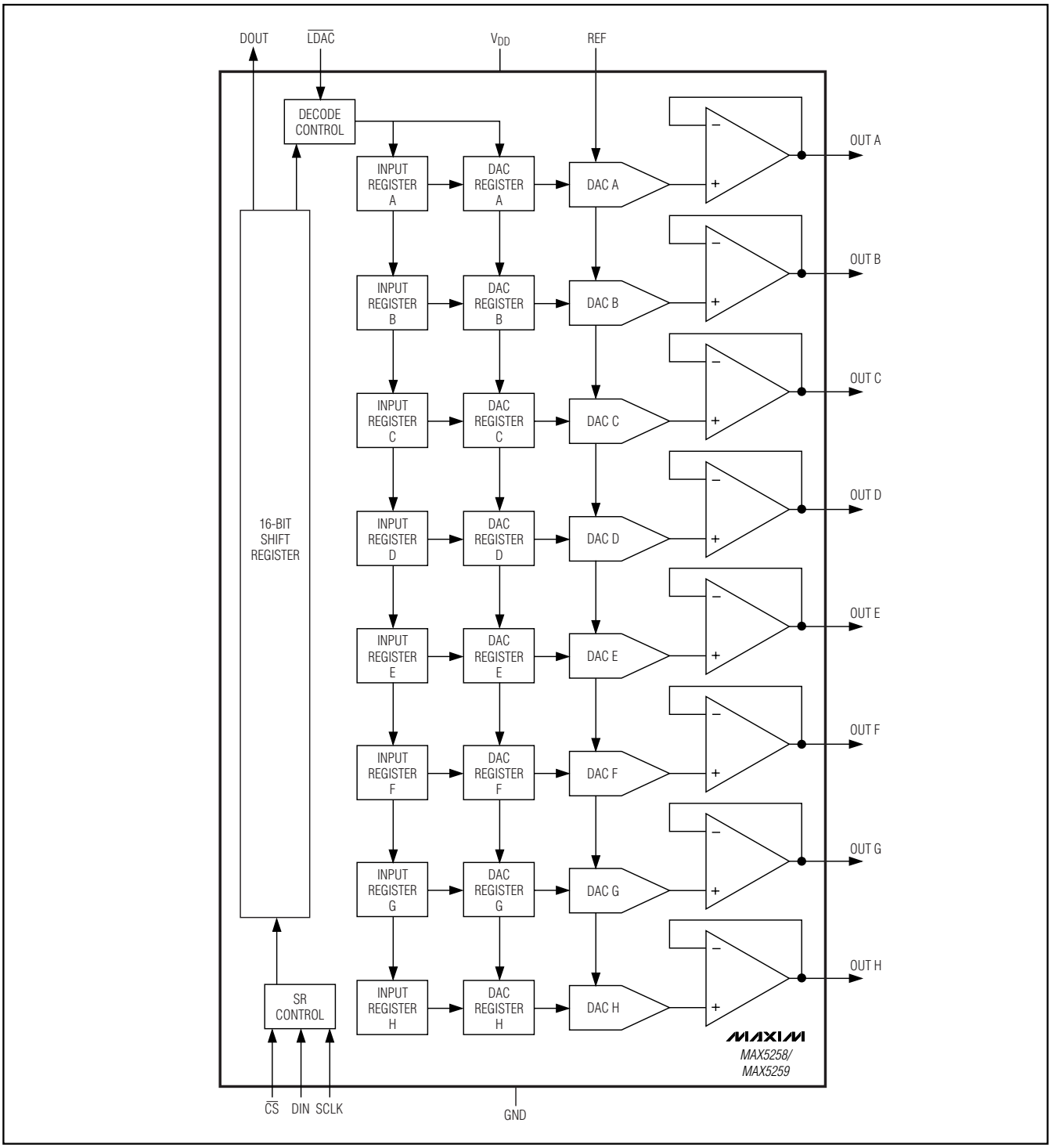
Note: 1LSB = $(V_{REF}) \times (2^8) = +V_{REF}\,(1 / 256)$

Chip Information

TRANSISTOR COUNT: 13625

PROCESS: BiCMOS

Functional Diagram

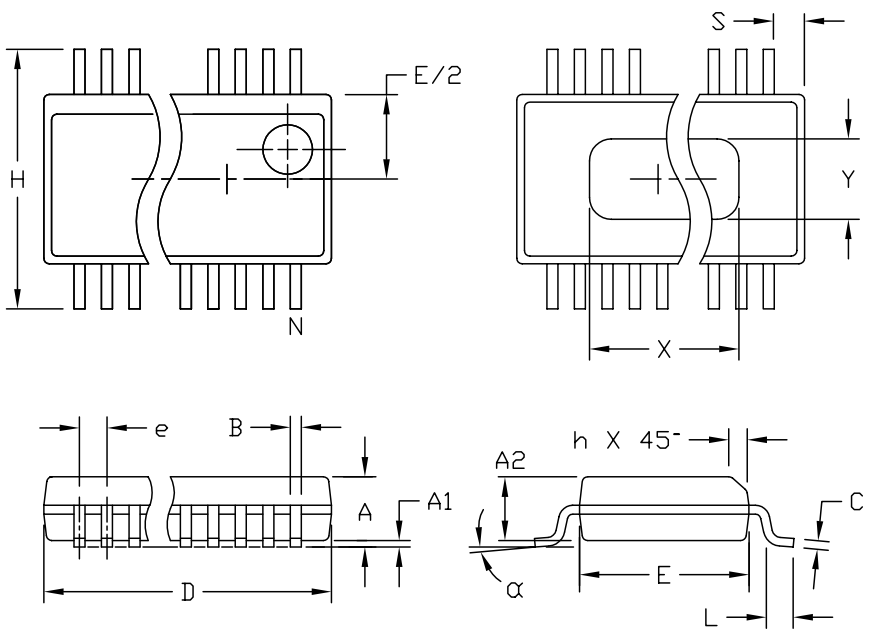


+5V/+3V, Low-Power, 8-Bit Octal DAC with Rail-to-Rail Output Buffers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1