Dual 1.5/3.0/6.0Gbps SAS/SATA Redriver

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} ....-0.3V to +4.0V
All Other Pins (Note 1) .... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Output Current DAP, DAM, HBM, HBP.........90mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 25.6mW/°C above +70°C).......2051mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)
20-Pin TQFN..6°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2)
20-Pin TQFN..39°C/W
Operating Temperature Range .... 0°C to +70°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -55°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: All I/O pins are clamped by internal diodes.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_{CL} = 10nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Power-Supply Range	V_{CC}			3.0		3.6	V
Power-Down Current	I_{PWRDN}	EN = GND			0.35	2	mA
Supply Current	I_{CC}	EN = V_{CC}	BA = BB = V_{CC}		100	130	mA
			BA = BB = GND		85	100	
Input Impedance, Differential	$Z_{RX-DIFF-DC}$	DC		85	100	115	Ω
Output Impedance, Differential	$Z_{TX-DIFF-DC}$	DC		85	100	115	Ω
AC PERFORMANCE							
Input Return Loss, Differential (Note 4)	$RL_{RX-DIFF}$	0.1GHz < f ≤ 0.3GHz				-18	dB
		0.3GHz < f ≤ 0.6GHz				-14	
		0.6GHz < f ≤ 1.2GHz				-10	
		1.2GHz < f ≤ 2.4GHz				-8	
		2.4GHz < f ≤ 3.0GHz				-8	
		3.0GHz < f ≤ 6.0GHz				-1	
Input Return Loss, Common Mode (Note 4)	RL_{RX-CM}	0.1GHz < f ≤ 0.3GHz				-6	dB
		0.3GHz < f ≤ 0.6GHz				-5	
		0.6GHz < f ≤ 1.2GHz				-5	
		1.2GHz < f ≤ 2.4GHz				-5	
		2.4GHz < f ≤ 3.0GHz				-5	
		3.0GHz < f ≤ 6.0GHz				-1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 10nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Return Loss, Differential (Note 4)	$RL_{TX-DIFF}$	0.1GHz < f ≤ 0.3GHz			-14	dB
		0.3GHz < f ≤ 0.6GHz			-8	
		0.6GHz < f ≤ 1.2GHz			-8	
		1.2GHz < f ≤ 2.4GHz			-8	
		2.4GHz < f ≤ 3.0GHz			-8	
		3.0GHz < f ≤ 6.0GHz			-1	
Output Return Loss, Common Mode (Note 4)	RL_{TX-CM}	0.1GHz < f ≤ 0.3GHz			-8	dB
		0.3GHz < f ≤ 0.6GHz			-5	
		0.6GHz < f ≤ 1.2GHz			-5	
		1.2GHz < f ≤ 2.4GHz			-5	
		2.4GHz < f ≤ 3.0GHz			-5	
		3.0GHz < f ≤ 6.0GHz			-1	
Differential Input Signal Range	$V_{RX-DFF-PP}$	SATA 1.5Gbps, 3Gbps, 6Gbps, M = GND	225		1600	mV_{P-P}
		SAS 1.5Gbps, 3Gbps, M = V_{CC}	275		1600	
		SAS 6.0Gbps, M = V_{CC}	300		1600	
OOB Squelch Threshold	$V_{SQ-DIFF}$	SATA OOB, M = GND	50		150	mV_{P-P}
		SAS OOB, M = V_{CC}	120		220	
Differential Output-Voltage Swing	$V_{TX-DIFF-PP}$	f = 750MHz, 1.5GHz; BA = BB = GND	450		650	mV_{P-P}
		f = 750MHz, 1.5GHz; BA = BB = V_{CC}	900		1300	
Propagation Delay	t_{PD}			300		ps
Output Rise/Fall Time	$t_{TX-RISE-FALL}$	Figure 1 (Notes 4, 5)	40		40	ps
Deterministic Jitter	$t_{TX-DJ-DD}$	Up to 6.0Gbps (Notes 4, 6)			15	ps_{P-P}
Random Jitter	$t_{TX-RJ-DD}$	Up to 6.0Gbps (Notes 4, 6)			1.4	ps_{RMS}
OOB Output Startup/Shutdown Time	t_{OOB}	(Note 7)		3	5	ns
Differential Offset Delta	$\Delta V_{OOB,DIFF}$	Difference between OOB and active-mode output offset	-80		+80	mV
Common-Mode Delta	$\Delta V_{OOB,CM}$	Difference between OOB and active-mode output V_{CM}	-50		+50	mV
CONTROL LOGIC						
Input Logic-Level Low	V_{IL}				0.6	V
Input Logic-Level High	V_{IH}		1.4			V
Input Logic Hysteresis	V_{HYST}			100		mV
Input Pulldown Resistor	R_{DOWN}			70		kΩ
ESD PROTECTION						
All Pins		Human Body Model		±5.5		kV

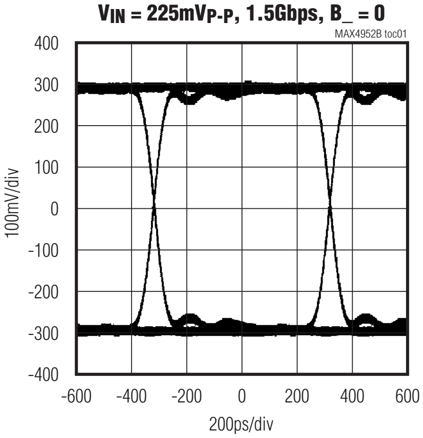
Note 3: This device is 100% production tested at T_A = +70°C. Specifications for all temperature limits are guaranteed by design.
Note 4: Guaranteed by design.
Note 5: Rise and fall times are measured using 20% and 80% levels.
Note 6: DJ measured using K28.5 pattern; RJ measured using D10.2 pattern.
Note 7: Total time for OOB detection circuit to enable/squelch the output.

Dual 1.5/3.0/6.0Gbps SAS/SATA Redriver

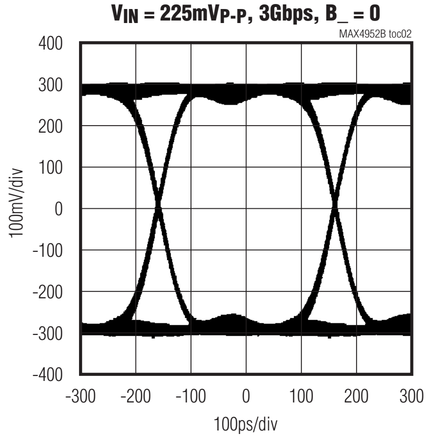
Typical Operating Characteristics

(V_{CC} = +3.3V, M = GND, T_A = +25°C; all eye diagrams measured using K28.5 pattern, unless otherwise noted.)

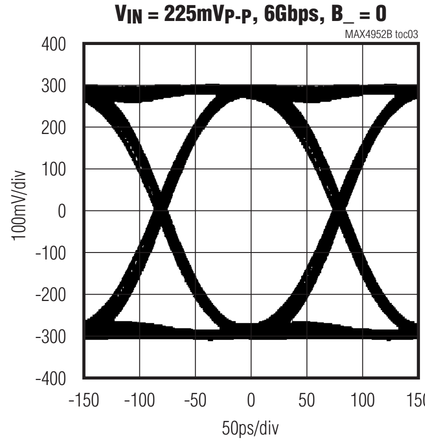
V_{IN} = 225mV$_{P-P}$, 1.5Gbps, B_ = 0



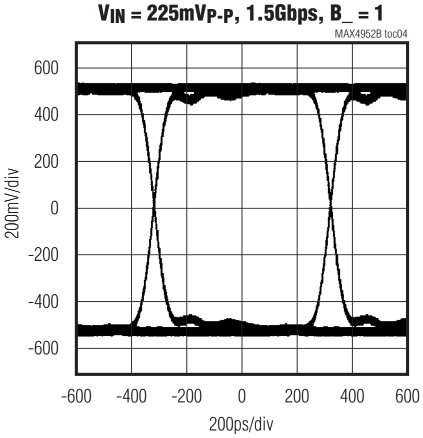
V_{IN} = 225mV$_{P-P}$, 3Gbps, B_ = 0



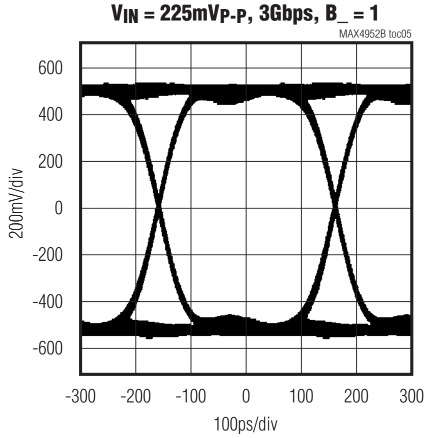
V_{IN} = 225mV$_{P-P}$, 6Gbps, B_ = 0



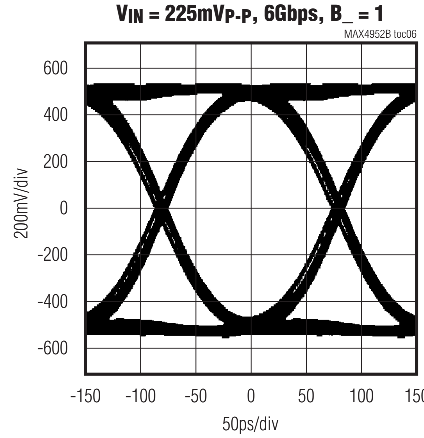
V_{IN} = 225mV$_{P-P}$, 1.5Gbps, B_ = 1



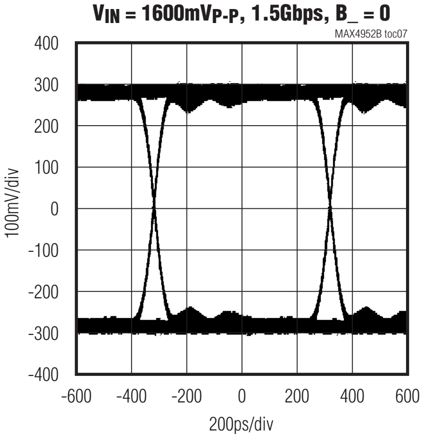
V_{IN} = 225mV$_{P-P}$, 3Gbps, B_ = 1



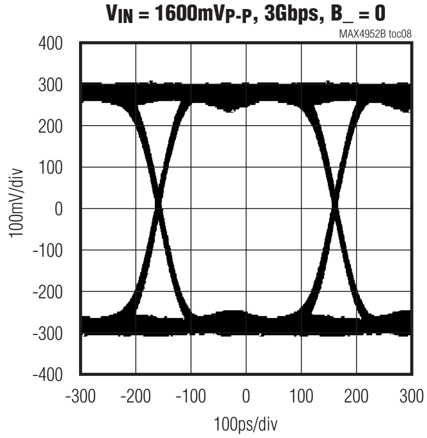
V_{IN} = 225mV$_{P-P}$, 6Gbps, B_ = 1



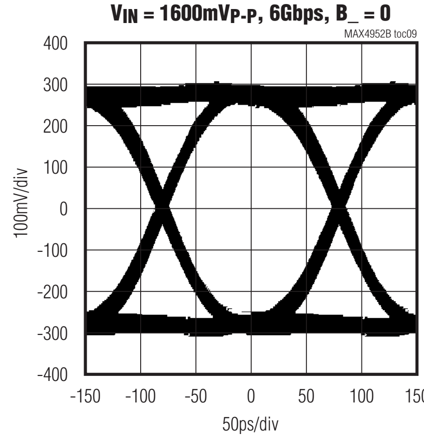
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, B_ = 0



V_{IN} = 1600mV$_{P-P}$, 3Gbps, B_ = 0



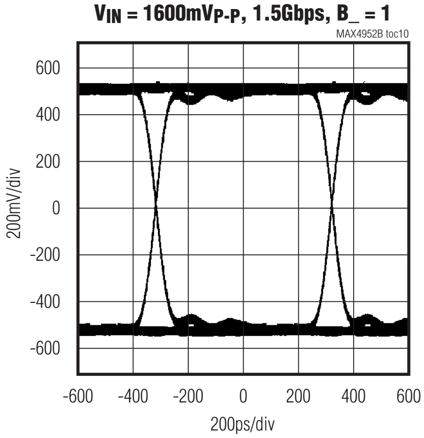
V_{IN} = 1600mV$_{P-P}$, 6Gbps, B_ = 0



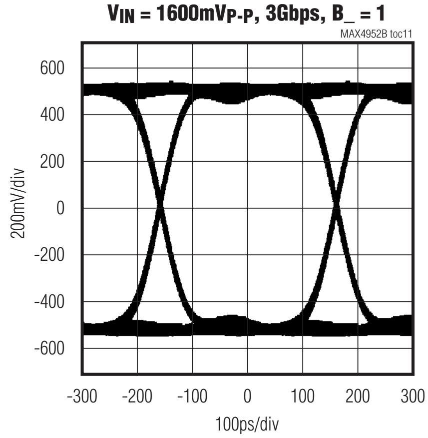
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, M = GND, T_A = +25°C; all eye diagrams measured using K28.5 pattern, unless otherwise noted.)

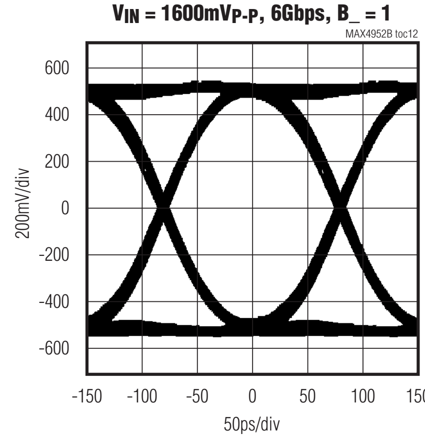
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, B_ = 1



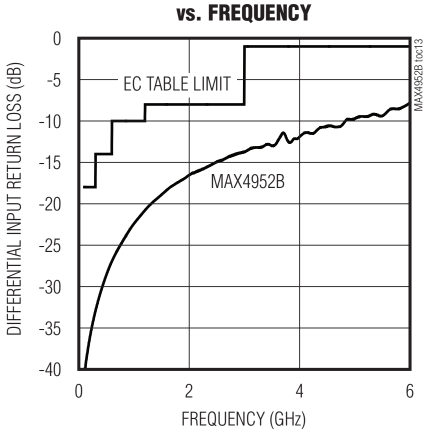
V_{IN} = 1600mV$_{P-P}$, 3Gbps, B_ = 1



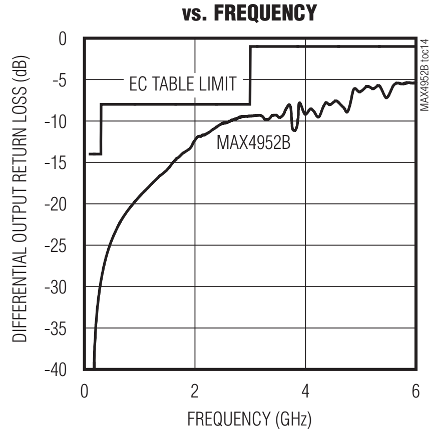
V_{IN} = 1600mV$_{P-P}$, 6Gbps, B_ = 1



DIFFERENTIAL INPUT RETURN LOSS vs. FREQUENCY

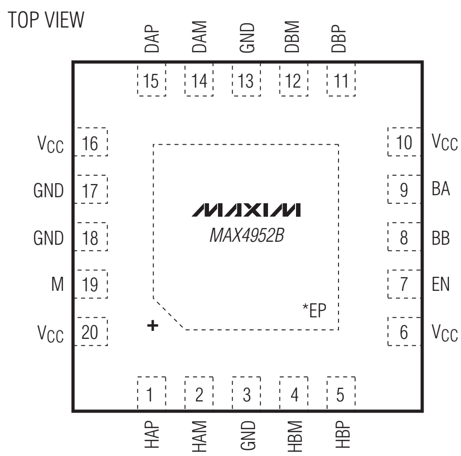


DIFFERENTIAL OUTPUT RETURN LOSS vs. FREQUENCY



Dual 1.5/3.0/6.0Gbps SAS/SATA Redriver

Pin Configuration



TQFN

*CONNECT EXPOSED PAD (EP) TO GND.

Pin Description

PIN	NAME	FUNCTION
1	HAP	Noninverting Input from Host Channel A. HAP must be capacitively coupled (see note).
2	HAM	Inverting Input from Host Channel A. HAM must be capacitively coupled (see note).
3, 13, 17, 18	GND	Ground
4	HBM	Inverting Output to Host Channel B. HBM must be capacitively coupled (see note).
5	HBP	Noninverting Output to Host Channel B. HBP must be capacitively coupled (see note).
6, 10, 16, 20	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with low-ESR 0.01µF and 4.7µF capacitors in parallel as close to the device as possible; recommended for each V_{CC} pin.
7	EN	Enable Input. Drive EN low for low-power standby mode. Drive EN high for normal operation. EN is internally pulled down by a 70kΩ (typ) resistor.
8	BB	Channel B Boost-Enable Input. Drive BB high to enable channel B +6dB output boost. Drive BB low for standard SAS/SATA output level. BB is internally pulled down by a 70kΩ (typ) resistor.
9	BA	Channel A Boost-Enable Input. Drive BA high to enable channel A +6dB output boost. Drive BA low for standard SAS/SATA output level. BA is internally pulled down by a 70kΩ (typ) resistor.
11	DBP	Noninverting Input from Device Channel B. DBP must be capacitively coupled (see note).
12	DBM	Inverting Input from Device Channel B. DBM must be capacitively coupled (see note).
14	DAM	Inverting Output to Device Channel A. DAM must be capacitively coupled (see note).
15	DAP	Noninverting Output to Device Channel A. DAP must be capacatively coupled (see note).
19	M	OOB-Mode Logic Input. M is internally pulled down by a 70kΩ (typ) resistor. Drive M low or leave unconnected for SATA OOB threshold. Drive M high for SAS OOB threshold.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane for proper thermal and electrical operation. Not intended as an electrical connection point.

Note: *For proper operation, Maxim recommends the use of low-ESR, X7R, 10nF, 0402-sized capacitors for all redriver inputs and outputs.*

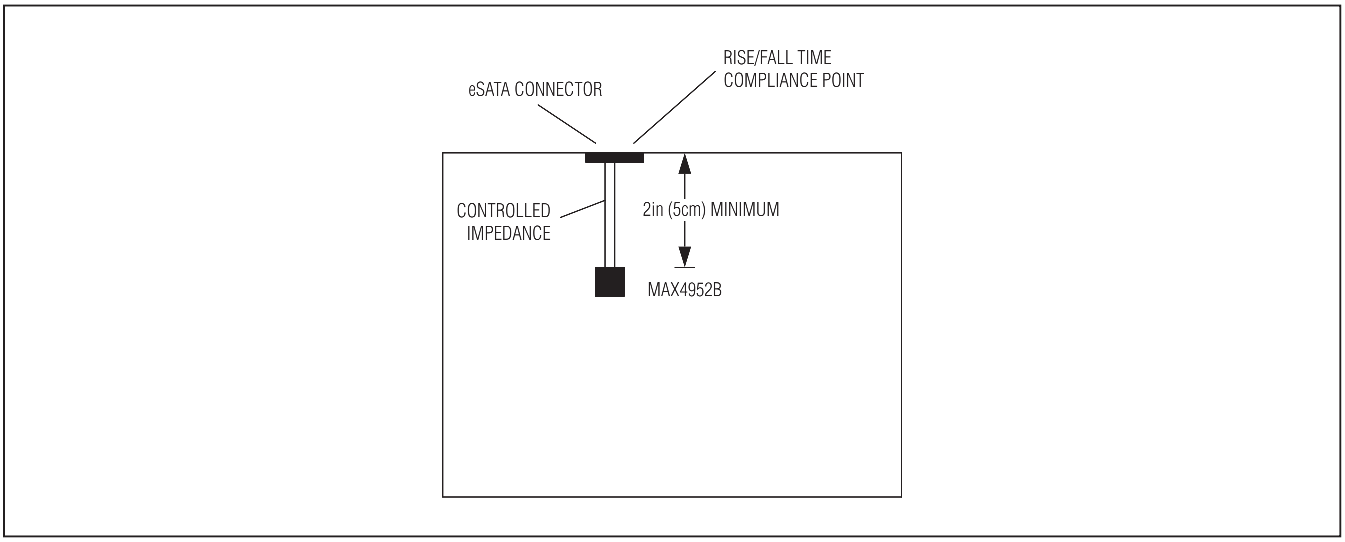
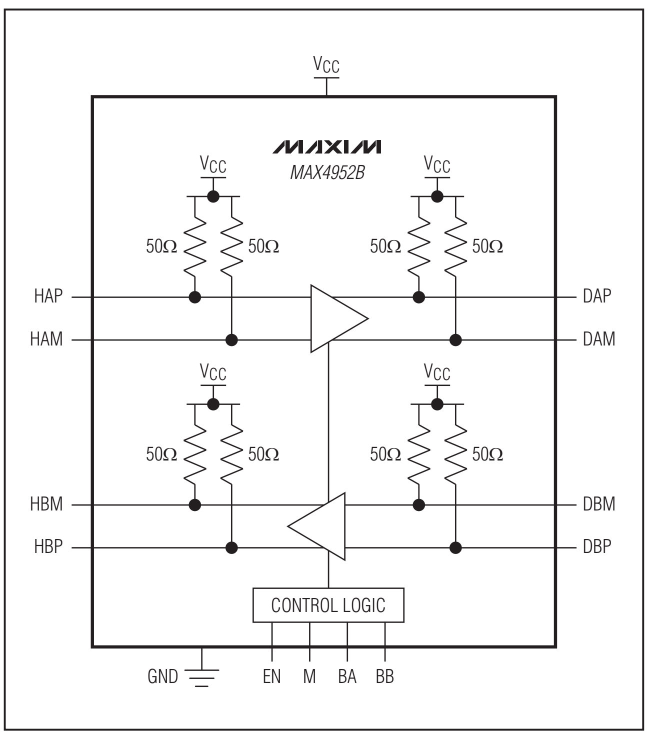


Figure 1. Circuit for Measuring $t_{R/F}$ for MAX4952B (refer to the SATA specifications for compliance measurement)

Functional Diagram/Truth Table



EN	BA	BB	CHANNEL A OUTPUT LEVEL	CHANNEL B OUTPUT LEVEL
0	X	X	Power-Down	Power-Down
1	0	0	No Boost	No Boost
1	0	1	No Boost	Boost
1	1	0	Boost	No Boost
1	1	1	Boost	Boost

X = Don't care.

M	OOB THRESHOLD
0	SATA
1	SAS

Dual 1.5/3.0/6.0Gbps SAS/SATA Redriver

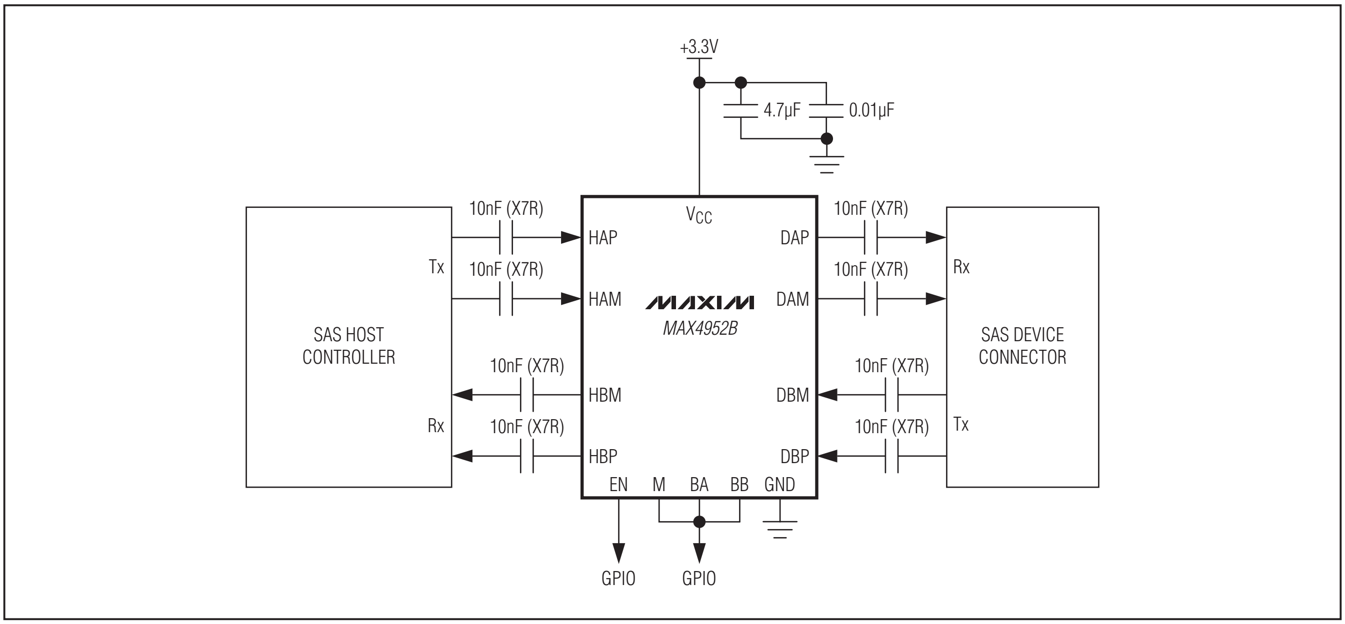


Figure 2. Typical Application Circuit

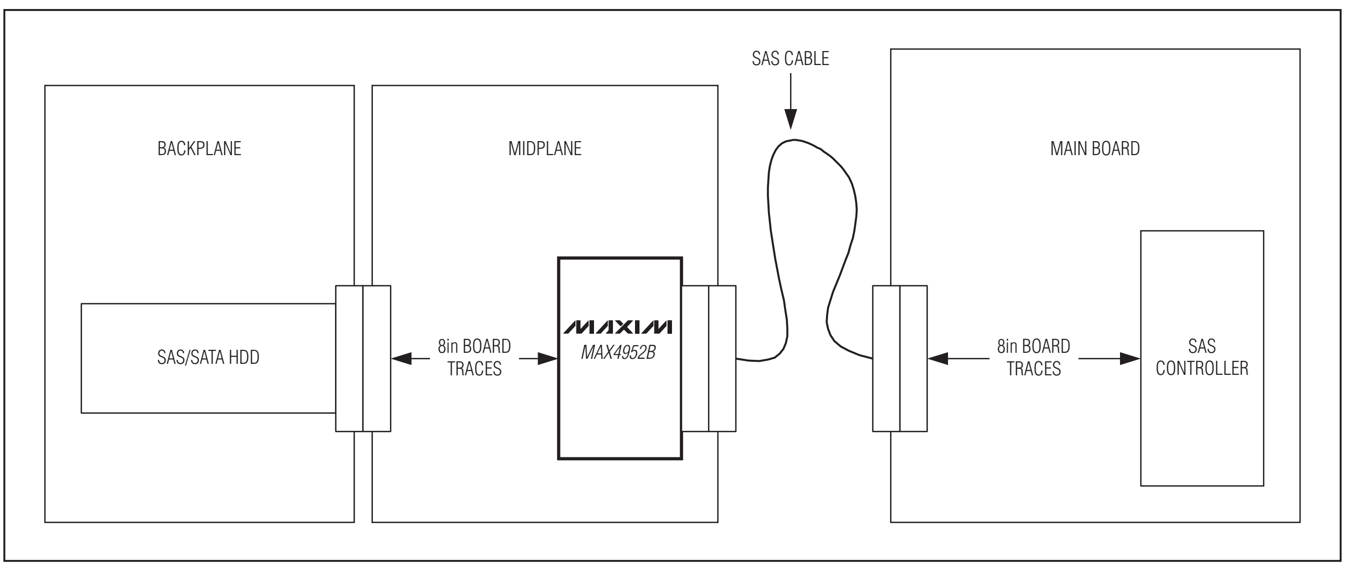


Figure 3. MAX4952B Driving a SAS Cable

Detailed Description

The MAX4952B dual-channel redriver is designed to redrive one full lane of SAS/SATA signals up to 6.0Gbps while operating from a single +3.3V supply.

The MAX4952B features independent output boost and enhances signal integrity at the receiver by re-establishing full output levels. SAS/SATA OOB signaling is supported using high-speed amplitude detection on the inputs and squelch on the corresponding outputs.

Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to V_{CC} (see the *Functional Diagram/Truth Table*) and must be AC-coupled using low-ESR, X7R, 10nF capacitors to the SAS/SATA controller IC and SAS/SATA device for proper operation.

Enable Input (EN)/Power-Down Mode

The MAX4952B features an active-high enable input, EN, which has an internal pulldown resistor of 70kΩ (typ). When EN is driven low or left unconnected, the MAX4952B enters power-down mode and squelches the output. Drive EN high for normal operation.

SAS/SATA Mode Input (M)

The MAX4952B supports both SAS and SATA OOB levels. When in SAS mode, the OOB threshold is $120mV_{P-P}$ (min), and when in SATA mode, the OOB threshold is $50mV_{P-P}$ (min). Signals below the OOB threshold are squelched to prevent unwanted noise from being redriven at the output. Drive M low or leave unconnected to set SATA OOB levels. Drive M high to set SAS OOB levels. See the *Functional Diagram/Truth Table*. M has an internal pulldown resistor of 70kΩ (typ).

Output Boost-Selection Inputs (BA, BB)

The MAX4952B has two digital control logic inputs, BA and BB. BA and BB have internal pulldown resistors of 70kΩ (typ). BA and BB control the boost level of their corresponding redrivers (see the *Functional Diagram/Truth Table*). Drive BA or BB low or leave unconnected for standard SAS/SATA output levels. Drive BA or BB high to boost the output.

Applications Information

Layout

Circuit board layout and design can significantly affect the performance of the MAX4952B. Use good, high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. Place low-ESR 0.01µF and 4.7µF power-supply bypass capacitors in parallel as close to V_{CC} as possible, or, as recommended, on each V_{CC} pin. Always connect V_{CC} to a power plane. The MAX4952B requires coupling capacitors for all redriver inputs and outputs. Maxim recommends high-quality, low-ESR, X7R, 10nF, 0402-sized capacitors.

Exposed-Pad Package

The exposed-pad, 20-pin TQFN package incorporates features that provide a very low-thermal resistance path for heat removal from the IC. The exposed pad on the MAX4952B must be soldered to the circuit board ground plane for proper thermal and electrical performance. For more information on exposed-pad packages, refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX4952B is protected against ESD up to ±5.5kV (Human Body Model) without damage. The ESD structures withstand ±5.5kV in all states (normal operation and powered down). After an ESD event, the MAX4952B continues to function without latchup.

Human Body Model

The MAX4952B is characterized for ±5.5kV ESD protection using the Human Body Model (MIL-STD-883, Method 3015). Figure 4 shows the Human Body Model and Figure 5 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V_{CC} before applying signals, especially if the signal is not current limited.

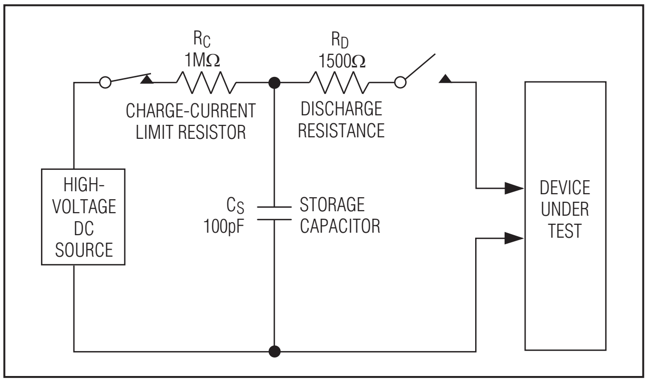


Figure 4. Human Body ESD Test Model

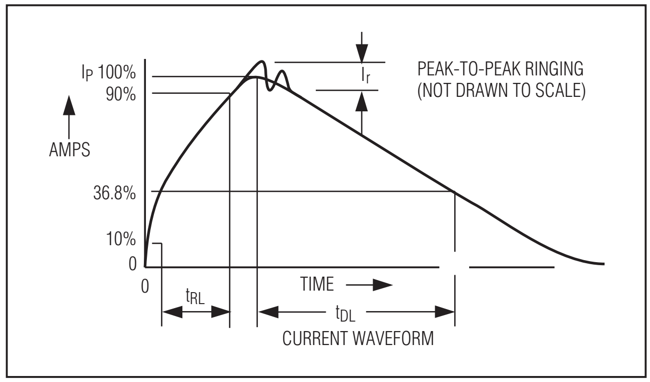


Figure 5. Human Body Current Waveform

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN-EP	T2044+2	21-0139