HDMI 2:1 Low-Frequency Translating Switch

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V+ .....-0.3V to +6V
All Pins (except GND) .....-0.3V to +6V
Continuous Current into Any I/O Terminal 25mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin QSOP (derate 9.1mW/°C above +70°C) 727mW
20-Pin TQFN (derate 16.9mW/°C above +70°C) 1356mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V ±10%, CLP = VL = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V+ Supply Current	I+	V+ = 5.5V, VL = CLP = 3.6V		3	8	µA
V+ Supply Current	I+	V+ = 0V, VL = CLP = 0V, $V_{HPIR\_}$ = +5.5V			200	µA
VL Supply Current	I_{VL}	V+ = 5.5V, VL = CLP = 3.6V			1	µA
CLP Supply Current	I_{CLP}	V+ = 5.5V, VL = CLP = 3.6V			1	µA
ANALOG SWITCH						
On-Resistance	$R_{ON(SCL\_)}$, $R_{ON(SDA\_)}$	V+ = 4.5V, CLP = 3V, $V_{SCL\_}$ or $V_{SDA\_}$ = 0 to 1.5V; $I_{SCL\_}$ or $I_{SDA\_}$ = ±10mA		10	25	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 4.5V, CLP = 3V, $V_{SCL\_}$ or $V_{SDA\_}$ = 0 to 1.5V; $I_{SCL\_}$ or $I_{SDA\_}$ = ±10mA		2	8	Ω
On-Resistance Flatness	R_{FLAT}	V+ = 4.5V, CLP = 3V, $V_{SCL\_}$ or $V_{SDA\_}$ = 0 to 1.5V; $I_{SCL\_}$ or $I_{SDA\_}$ = ±10mA			13	Ω
Off-Leakage Current	$I_{SCL\_(OFF)}$, $I_{SDA\_(OFF)}$	V+ = 5.5V, $V_{SCL\_}$ or $V_{SDA\_}$ = 0V, 5.5V; HIZ1 = HIZ2 = 0V or VL (Note 1)	-5		+5	µA
On-Leakage Current	$I_{SCL\_(ON)}$, $I_{SDA\_(ON)}$	V+ = 5.5V, $V_{SCL\_}$ or $V_{SDA\_}$ = 0V, 5.5V (Note 1)	-5		+5	µA
Output Clamped Voltage	$V_{OVC(SCLO)}$, $V_{OVC(SDAO)}$	V+ = 5V, CLP = 3.3V, VL = 5V, R_P = 1kΩ (Note 2)		3.3		V
SWITCH DYNAMIC CHARACTERISTICS						
SCL_, SDA_ Off-Capacitance	$C_{SCL\_(OFF)}$, $C_{SDA\_(OFF)}$	V+ = 5V, T_A = +25°C, Figure 1		20		pF
SCL_, SDA_ On-Capacitance	$C_{SCL\_(ON)}$, $C_{SDA\_(ON)}$	V+ = 5V, T_A = +25°C, Figure 1		30		pF
Bandwidth	BW	R_S = R_L = 50Ω, C_L = 10pF		40		MHz
Crosstalk	V_{CT}	R_S = R_L = 50Ω, f = 1MHz, Figure 2 (Note 3)		-75		dB
Off-Isolation	V_{ISO}	R_S = R_L = 50Ω, f = 1MHz, Figure 2 (Note 4)		-70		dB
LOGIC INPUT (HPIR1, HPIR2)						
Input Logic-Low Voltage	V_{IL}	V+ = 4.5V			0.8	V
Input Logic-High Voltage	V_{IH}	V+ = 5.5V	3.8			V
Input Logic Leakage	I_{INL}			0.01	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V ±10%, CLP = VL = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUT (SEL, HPD, HIZ1, HIZ2)						
Input Logic-Low Voltage	V_{IL}	V+ = 4.5V, VL = CLP = 3V			0.8	V
Input Logic-High Voltage	V_{IH}	V+ = 5.5V, VL = CLP = 3.6V	2.0			V
Hysteresis	V_{HYST}	3V ≤ VL = CLP ≤ 3.6V		150		mV
Input Logic-Leakage Current	I_{INL}			0.01	1	µA
LOGIC OUTPUT (HPDO1, HPDO2, HPIRO)						
HPDO_ Output Logic-Low Voltage	$V_{OL(HPDO\_)}$	V+ = 4.5V, VL = CLP = 3.0V, I_{SINK} = 4mA			0.5	V
HPDO_ Output Logic-High Voltage	$V_{OH(HPDO\_)}$	V+ = 4.5V, VL = CLP = 3.0V, I_{SOURCE} = 4mA	4.0			V
HPIRO Output Logic-Low Voltage	$V_{OL(HPIRO)}$	V+ = 4.5V, VL = CLP = 3.0V, I_{SINK} = 2mA			0.5	V
HPIRO Output Logic-High Voltage	$V_{OH(HPIRO)}$	V+ = 4.5V, VL = CLP = 3.0V, I_{SOURCE} = 2mA	2.5			V
Output-Logic Leakage Current	I_O	HIZ1 = HIZ2 = 0V or VL			1	µA
TIMING CHARACTERISTICS						
Logic Delay	$t_{PD(HPDO\_)}$	V+ = 4.5V, VL = CLP = 3.0V, C_L = 15pF, SEL = 0V or VL (Figure 3)		33		ns
	$t_{PD(HPIRO)}$	V+ = 4.5V, VL = CLP = 3.0V, C_L = 15pF, SEL = 0V or VL (Figure 3)		33		
ESD PROTECTION						
ESD Protection, Human Body Model		HPIR1, HPIR2, HPDO1, HPDO2, SCL1, SCL2, SDA1, SDA2 (Note 5)		±6		kV
		HPIRO, HPD, SEL, SCLO, SDAO, HIZ1, HIZ2 (Note 6)		±2		
EXESD Leakage Current				1.0		µA

Note 1: Leakage measured at SCLO or SDAO with SCL_ and SDA_ open.
Note 2: Pullup resistor of R_P = 1kΩ at SCLO and SDAO. These resistors are necessary for the clamp/translation to operate correctly.
Note 3: Crosstalk is measured between any two analog inputs, crosstalk = 20log(V_{OUT} / V_{IN}).
Note 4: Off-isolation = 20log10 (V_{SCLO} / $V_{SCL\_}$), V_{SCLO} = output, $V_{SCL\_}$ = input to off switch.
Note 5: Referenced to GND.
Note 6: Any combination of pin to any other pin.

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Test Circuits/Timing Diagrams

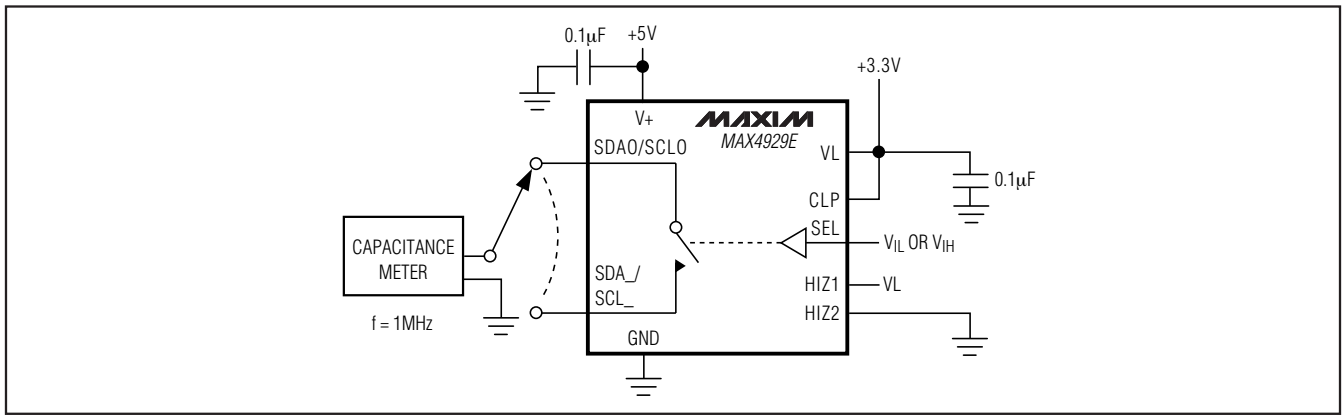


Figure 1. Channel Off-/On-Capacitance

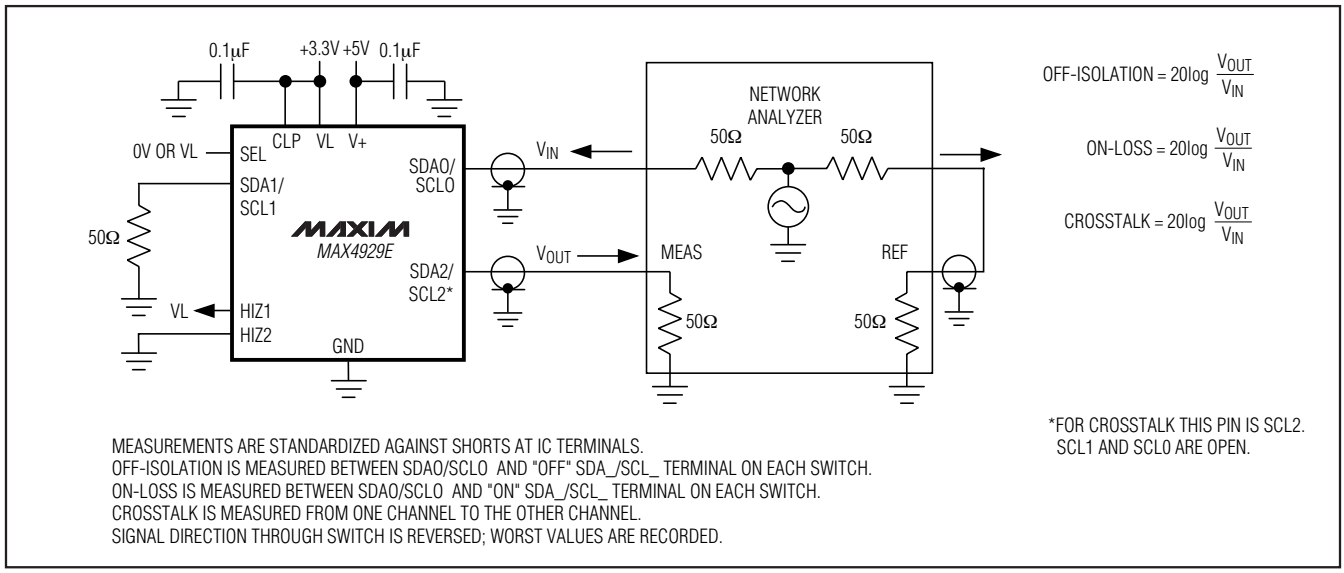


Figure 2. On-Loss, Off-Isolation, and Crosstalk

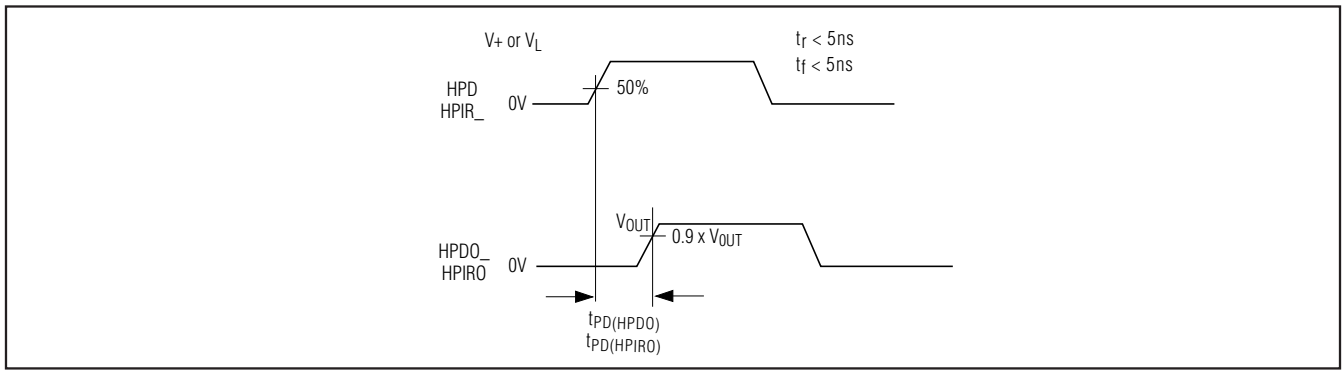
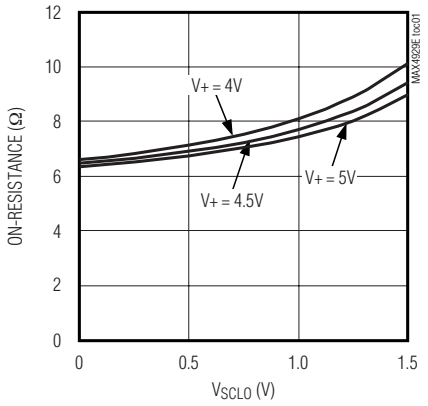


Figure 3. Logic Delay Timing

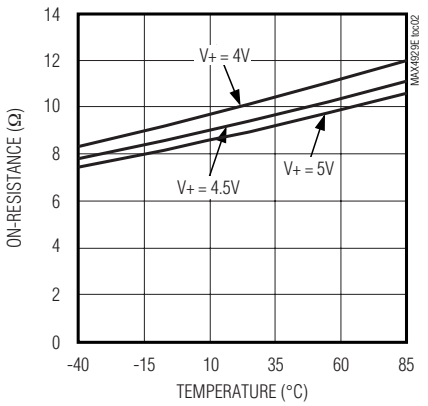
Typical Operating Characteristics

(V+ = 5V, VL = 3.3V, CLP = 3.3V, T_A = +25°C, unless otherwise noted.)

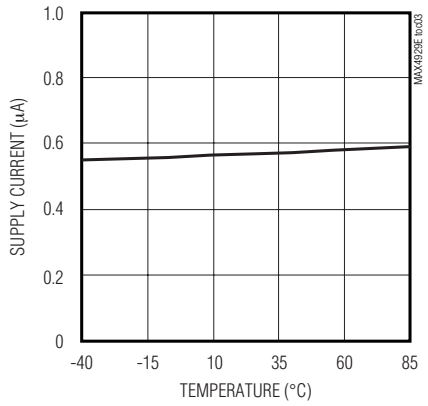
ON-RESISTANCE vs. V_{SCLO}



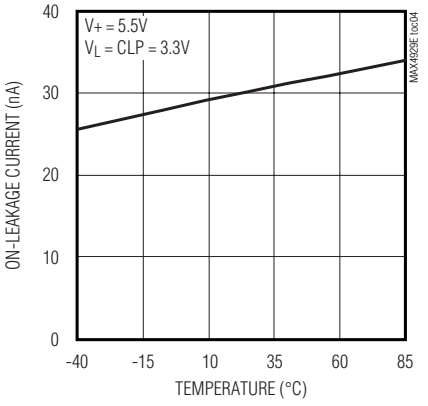
ON-RESISTANCE vs. TEMPERATURE



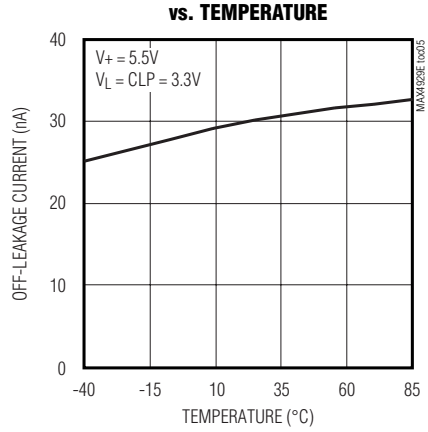
SUPPLY CURRENT vs. TEMPERATURE



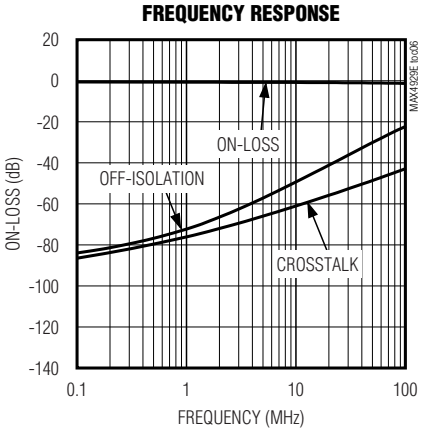
ON-LEAKAGE CURRENT vs. TEMPERATURE



OFF-LEAKAGE CURRENT vs. TEMPERATURE



FREQUENCY RESPONSE

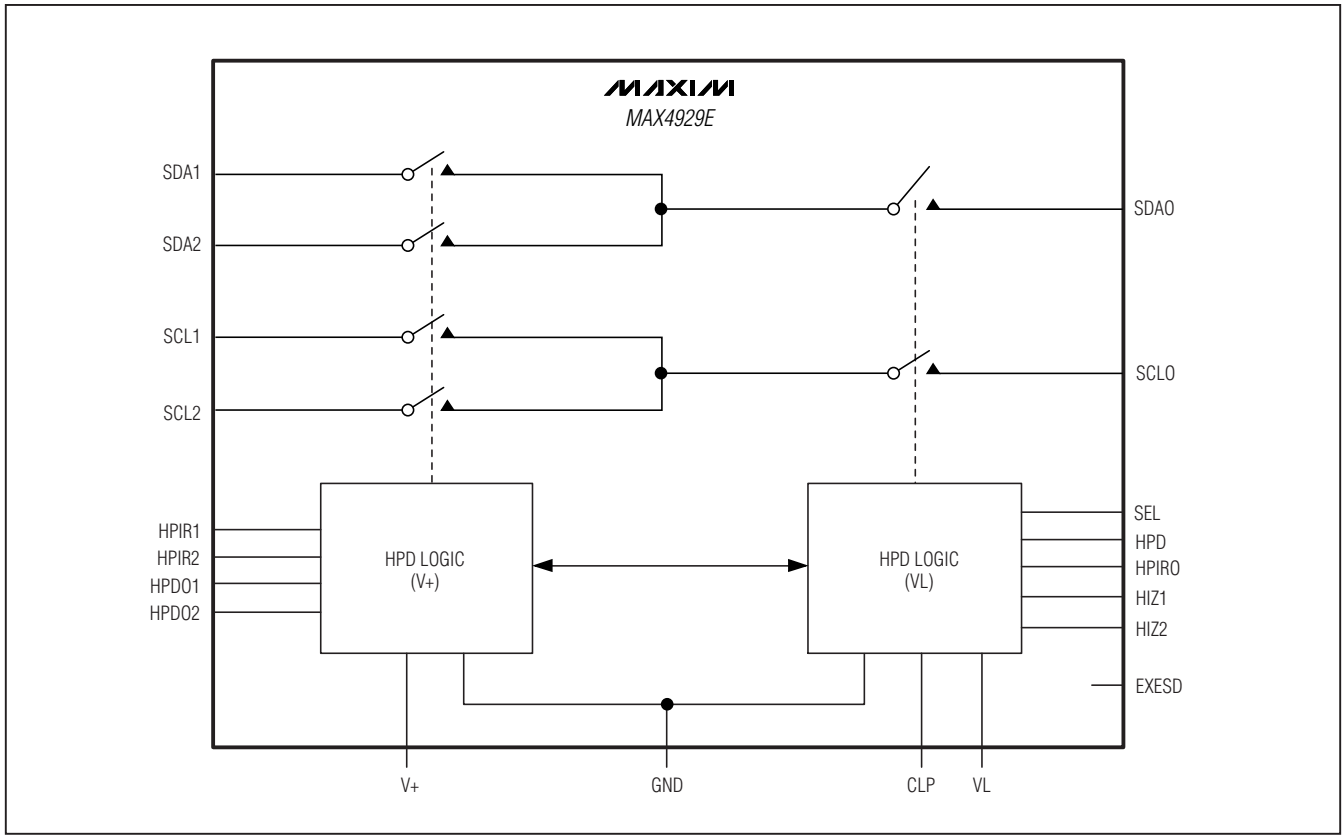


HDMI 2:1 Low-Frequency Translating Switch

Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1	19	HPDO2	Hot-Plug Detect Output 2. Translate logic level of HPD to V+ compatible (see Table 2).
2	20	HPIR2	Hot-Plug Interrupt Request 2
3	1	SDA2	Serial Data Input. SDA Mux Input 2.
4	2	SCL2	Serial Clock Input. SCL Mux Input 2.
5	3	HPDO1	Hot-Plug Detect Output 1. Translate logic level of HPD to V+ compatible (see Table 2).
6	4	HPIR1	Hot-Plug Interrupt Request 1
7	5	SDA1	Serial Data Input. SDA Mux Input 1.
8	6	SCL1	Serial Clock Input. SCL Mux Input 1.
9	7	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.1µF or greater ceramic capacitor.
10	8	CLP	Clamp-Voltage Reference. Clamp the maximum voltage of SCLO and SDAO. Bypass CLP to GND with a 0.1µF or greater ceramic capacitor (see Figure 6 and the *Typical Operating Circuit).*
11	9	VL	Logic Supply for HIZ_, SEL, HPD, HPIRO. Bypass VL to GND with a 0.1µF or greater ceramic capacitor. VL should have the same voltage level as any MCU interface.
12	10	SEL	Select Input. Logic input for Mux connection (see Table 1).
13	11	SCLO	SCL Mux Output. Connect SCLO to EDID EPROM.
14	12	SDAO	SDA Mux Output. Connect SDAO to EDID EPROM.
15	13	HPIRO	Hot-Plug Interrupt Request Output. Translate logic level of HPIR_ to VL compatible (see Table 3).
16	14	HPD	Hot-Plug Detect Input. Logic level on HPD is compatible with MCU.
17	15	HIZ2	Enable Input 2 (see Table 4).
18	16	HIZ1	Enable Input 1 (see Table 4).
19	17	GND	Ground
20	18	EXESD	External ESD Discharge. Connect 0.1µF capacitor from EXESD to GND.
—	EP	EP	Exposed Paddle. Connect EP to GND or leave EP unconnected.

Functional Diagram



Detailed Description

The MAX4929E low-frequency 2:1 switch is ideal for the low-frequency portion of HDMI/DVI switching applications. The device features three independent voltage inputs that allow the user to match any voltage level encountered in switching without additional components. The V+ range is from 4.5V to 5.5V to match the HDMI/DVI 5V requirements. CLP is set to match the EDID EPROM from 3.3V to 5.5V. VL is connected to the same supply as the system MCU. All pins going to the HDMI/DVI connectors are ESD-protected to ±6kV Human Body Model (HBM).

The MAX4929E has two enable inputs. The enable function allows the device to operate in normal mode or go into a high-Z state. It is possible to control two MAX4929Es with a single control bit, creating a 4:1 equivalent switch using a minimum of external components (see Figure 6).

Supply or signals sequencing are not required for the MAX4929E. Supply voltages V+, VL, and CLP can be applied in any order. Signals can be applied in any order as well.

Analog Switch

The MAX4929E features a voltage clamp function for the two 2:1 switch. Inputs to SCL_/SDA_ are V+ level compatible. Maximum output voltages of SCLO/SDAO are clamped to CLP. For optimum performance connect the EDID EPROM supply voltage to CLP (see Figure 6). For proper operation of the voltage clamp, connect SCLO/SDAO to CLP through the pullup resistors. For maximum output range, connect CLP to V+. The output of the switch is connected to the EDID EPROM, voltages from 3V to 5.5V are expected.

Logic Inputs

VL is the supply to input logic HIZ_, SEL, and HPD. Connect VL to the same supply as the system MCU for compatibility.

V+ is the supply to the input logic of the HPIR1 and HPIR2 inputs.

HDMI 2:1 Low-Frequency Translating Switch

Table 1. Inputs Selection for 2:1 Mux Truth Table

INPUTS			SWITCH CONNECTIONS
SEL	HIZ1	HIZ2	
0	0	1	SDAO to SDA1, SCLO to SCL1
0	1	0	SDAO to SDA1, SCLO to SCL1
1	0	1	SDAO to SDA2, SCLO to SCL2
1	1	0	SDAO to SDA2, SCLO to SCL2
X	0	0	High Impedance
X	1	1	High Impedance

Table 2. HPD Output Channel Selection

INPUTS				OUTPUTS	
SEL	HPD	HIZ1	HIZ2	HPDO1	HPDO2
X	0	0 1	1 0	0	0
0	1	0 1	1 0	1	0
1	1	0 1	1 0	0	1
X	X	1	1	High Impedance	High Impedance
X	X	0	0	High Impedance	High Impedance

Table 3. HPIRO Output Channel Selection

INPUTS					OUTPUT
SEL	HPIR1	HPIR2	HIZ1	HIZ2	HPIRO
X	0	0	0 1	1 0	0
X	1	1	0 1	1 0	1
0	0	X	0 1	1 0	0
0	1	X	0 1	1 0	1
1	X	0	0 1	1 0	0
1	X	1	0 1	1 0	1
X	X	X	0	0	High Impedance
X	X	X	1	1	High Impedance

Table 4. Mode of Operation

INPUTS		OUTPUTS
HIZ1	HIZ2	MODE OF OPERATION
0	0	High Impedance: SDAO, SDA1, SDA2, SCLO, SCL1, SCL2, HPDO1, HPDO2, HPIRO
0	1	Normal Operation
1	0	Normal Operation
1	1	High Impedance: SDAO, SDA1, SDA2, SCLO, SCL1, SCL2, HPDO1, HPDO2, HPIRO

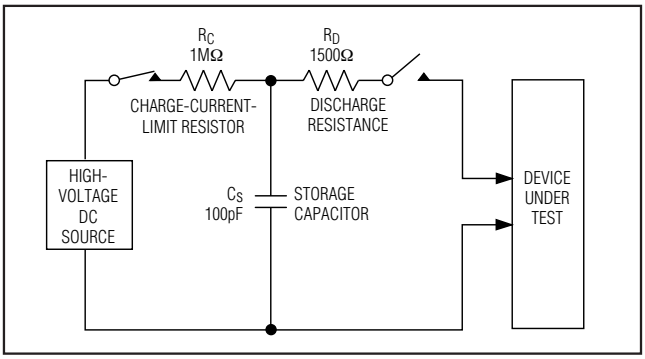


Figure 4. Human Body ESD Test Model

Logic Outputs

The HPDO_ signals are 5V TTL-compatible, per HDMI/DVI specifications. HPIRO is VL compatible.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. Additionally, the MAX4929E is protected to ±6kV (HBM) on SCL1, SCL2, SDA1, SDA2, HPDO1, HPDO2, HPIR1, and HPIR2 by the HBM.

Human Body Model

Several ESD testing standards exist for measuring the robustness against ESD events. The ESD protection of the MAX4929E is characterized with the HBM method. Figure 4 shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage, then discharged through a 1.5kΩ resistor. Figure 5 shows the current waveform when the storage capacitor is discharged into a lower impedance.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report documenting test setup, methodology, and results.

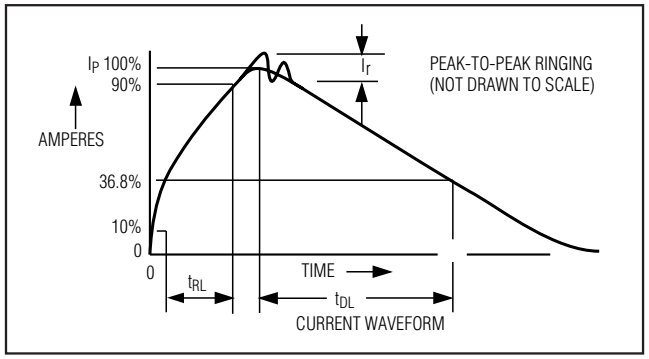


Figure 5. HBM Discharge Current Waveform

Applications Information

Power-Supply Bypassing and Sequencing

There is no power-supply sequencing required. Power can be applied to V+, CLP, or VL in any order. Bypass V+, VL, and CLP to GND using 0.1µF or larger ceramic capacitors as close to the device as possible.

Hot Plug

The MAX4929E is designed for HDMI/DVI switching. The MAX4929E permits hot-plugging to any inputs/outputs regardless of the power status of the device. A plug can be inserted, and thus connected to the MAX4929E whether the device is powered up or not. Therefore, sequencing of power supplies is not required; V+, CLP, and VL can be applied in any order.

Configure Two Devices to Form 4:1 Switch

Two MAX4929Es can be connected together to form a 4:1 switch (see Figure 6).

Exposed Paddle

The MAX4929EETP+ provides an EP to improve thermal performance in the TQFN package. Connect the EP to GND or leave EP unconnected.

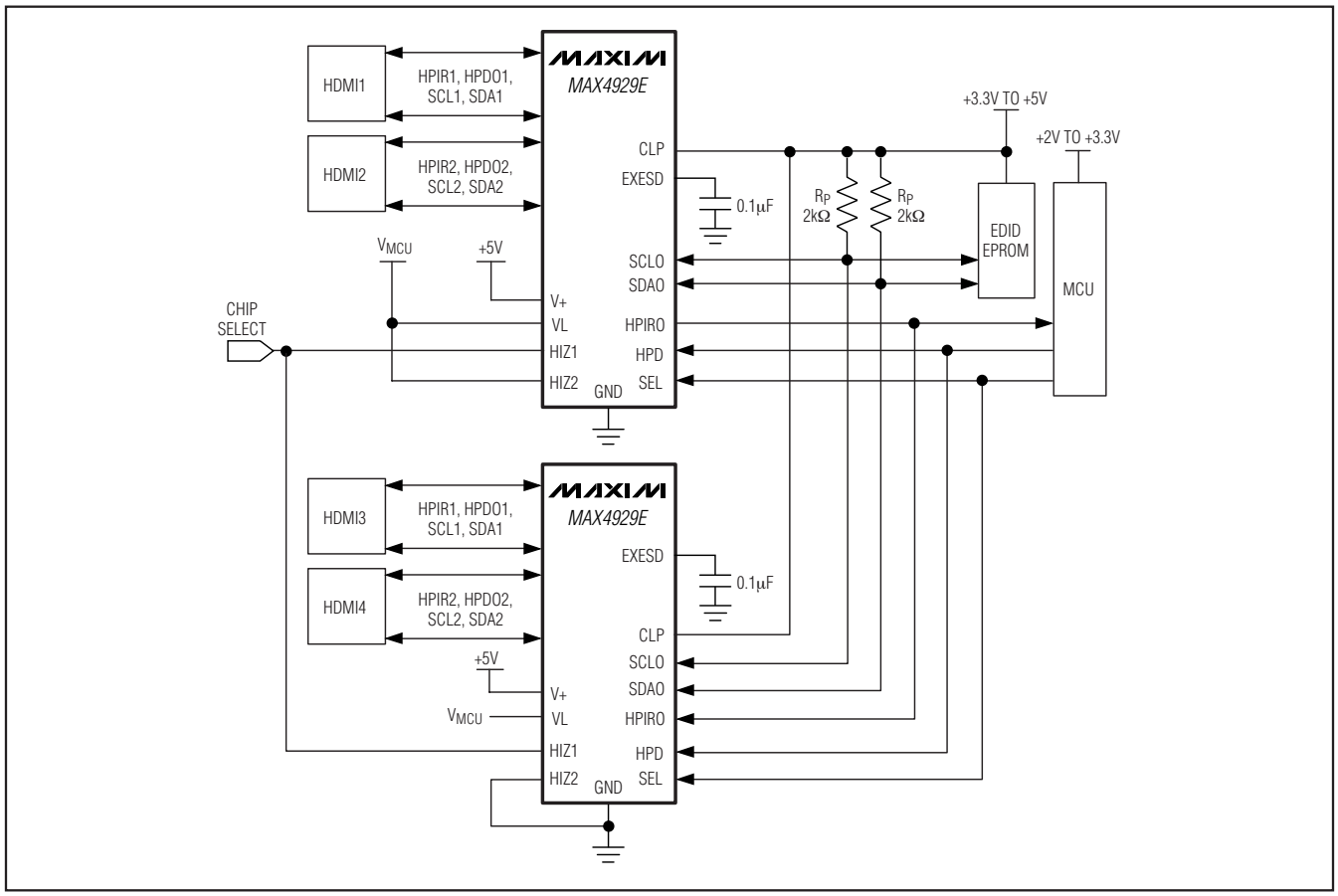
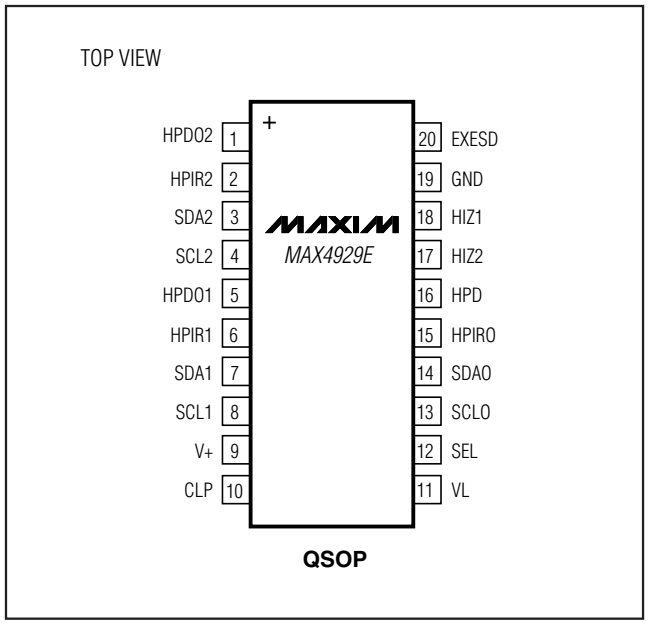


Figure 6. Two MAX4929Es Connected to Form a 4:1 Translating Switch

HDMI 2:1 Low-Frequency Translating Switch

Pin Configurations (continued)

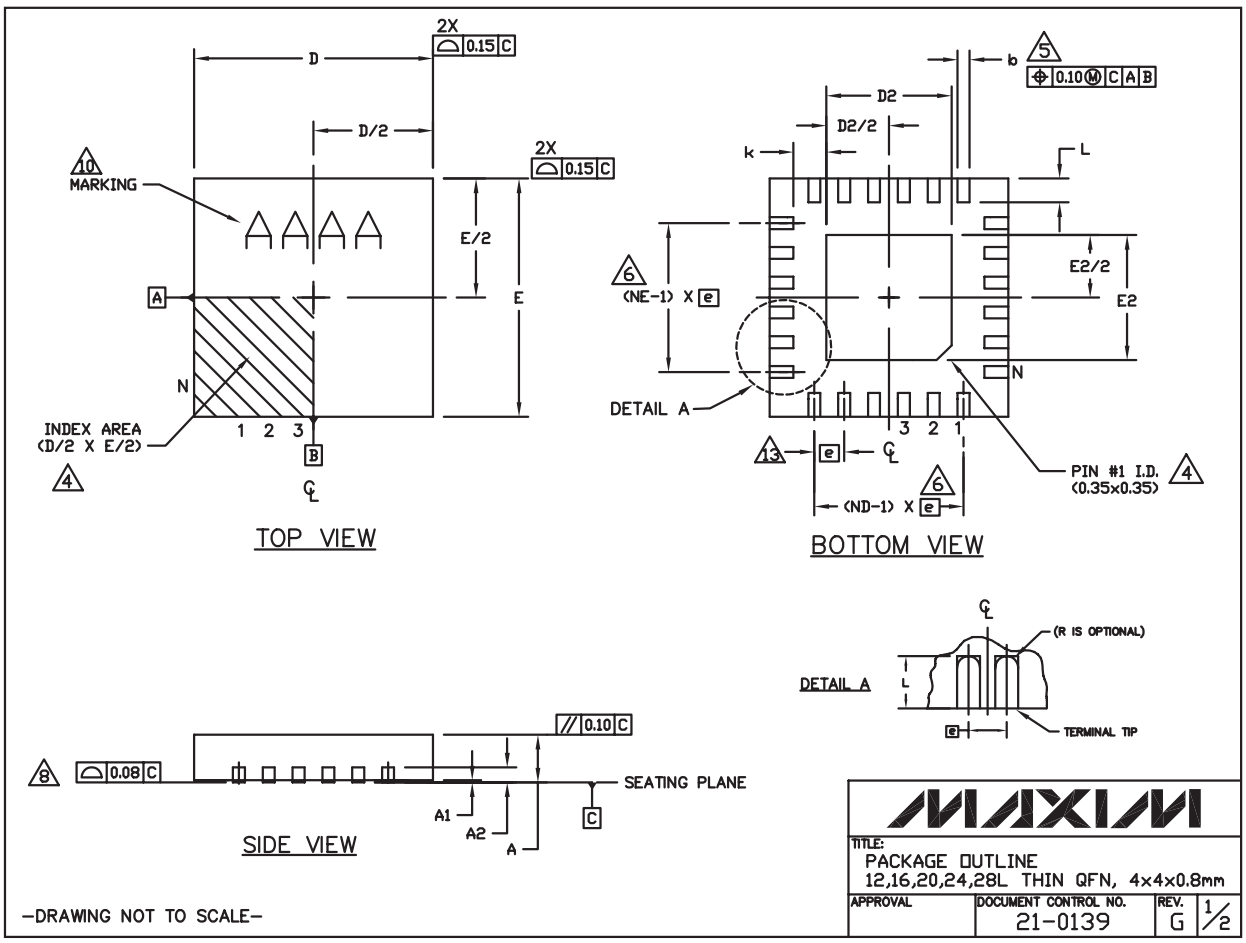


Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



HDMI 2:1 Low-Frequency Translating Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

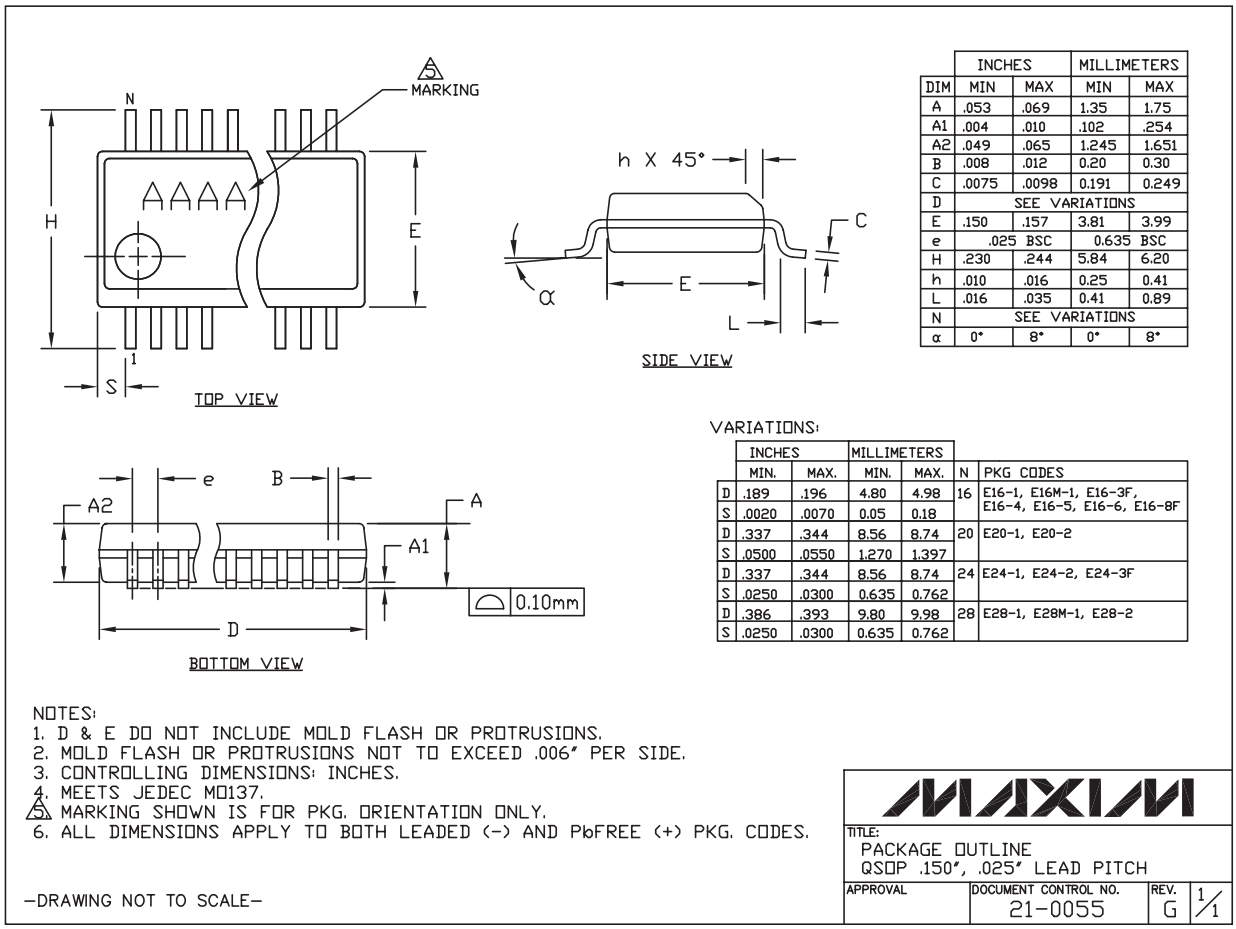
TITLE:
PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	G	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	PKG CODES
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-3F, E16-4, E16-5, E16-6, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2, E24-3F
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

MAXIM

TITLE:
PACKAGE OUTLINE
QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	G	1/1