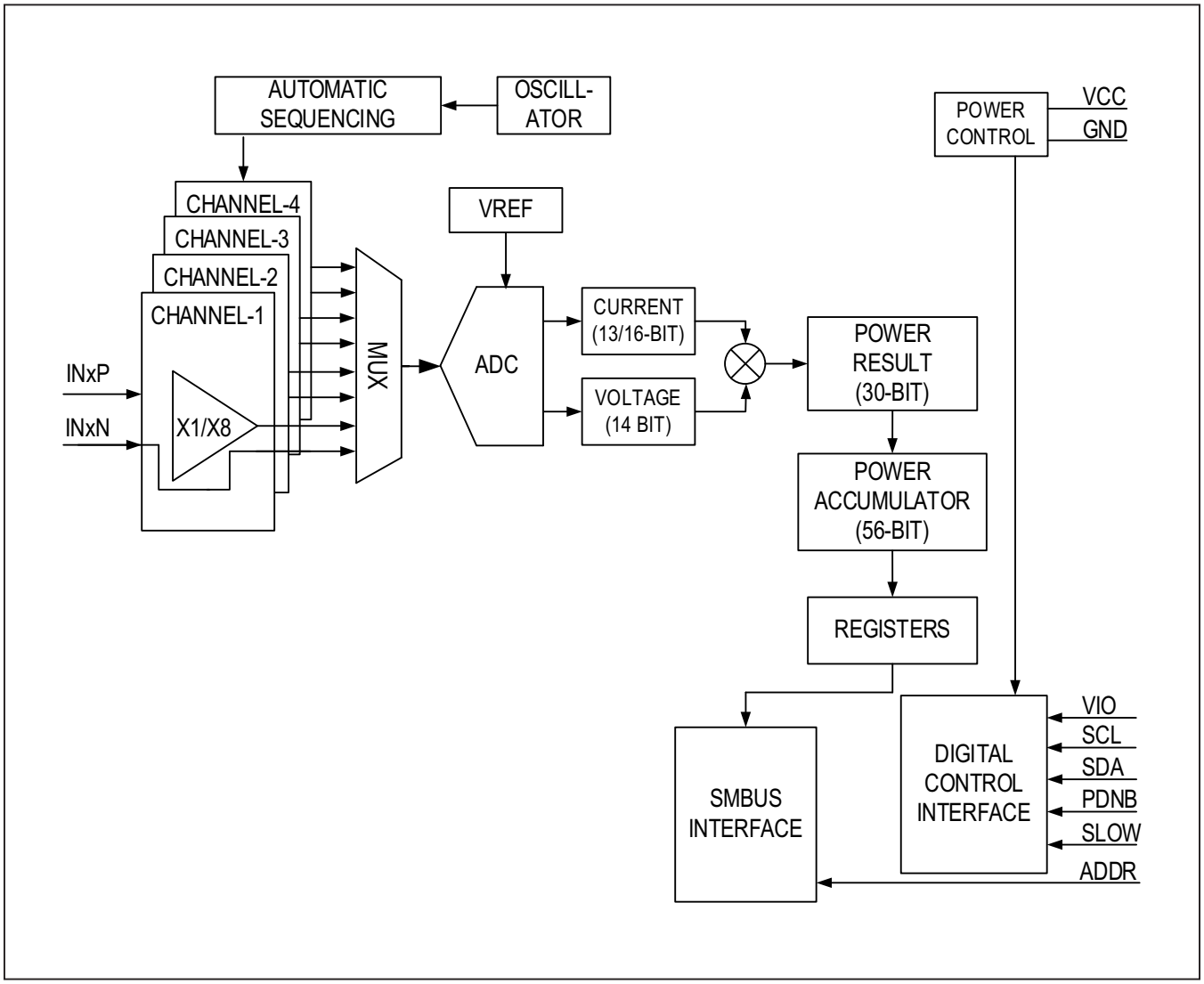
Simplified Block Diagram



Absolute Maximum Ratings

IN+ and IN- to GND .....-0.3V to +24V
Differential Input Voltage, IN+ to IN- .....±0.5V
V_{DD} or V_{IO} to GND .....-0.3V to +4V
SDA or SCL to GND .....-0.3V to +4V
All Other Pins ..... -0.3V to V_{IO} + 0.3 (not to exceed +4)V

Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Soldering Temperature .....See the IPC/JEDEC J-STD-020A Specification°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 WLP

PACKAGE CODE	N162A2+1
Outline Number	21-100184
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{DD} = 2.7V to 3.6V, V_{IO} = 1.6V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C. Limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_{DD} Operating Range			2.7		3.6	V
V_{DD} Average Supply Current (Note 1)	I_{DD}	PDNB = V_{IO} and SLOW = GND		774		µA
		PDNB = V_{IO} and SLOW = VIO		10		
		PDNB = GND		2		
V_{IO} Operating Range			1.6		3.6	V
V_{IO} Average Supply Current (Note 1)	I_{IO}	PDNB = V_{IO}		10		µA
		PDNB = GND		1		
SENSE INPUT/OUTPUT						
Minimum Input Common-Mode Voltage				0.5		V
Maximum Input Common-Mode Voltage				20		V
IN+ Input Bias Current				1		µA
IN- Average Input Bias Current (Note 2)		SLOW = V_{IO} or PDNB = GND		1		µA
		SLOW = GND (V_{SENSE} = 0mV)		5		
		SLOW = GND (V_{SENSE} = 100mV)		5		

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 3.6V, V_{IO} = 1.6V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C. Limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Per Channel Current and Voltage Sample Rate (Note 5)		SLOW = GND		1024		sps
Per Channel Current and Voltage Sample Rate		SLOW = V_{IO}		8		sps
Per Channel Power Calculation Rate (Note 5)		SLOW = GND		1024		sps
Per Channel Power Calculation Rate		SLOW = V_{IO}		8		sps
Power Measurement Accumulation Accuracy (1 Sigma Error Range with > 2500 Accumulations) (Note 3, Note 4)		V_{SENSE} = 5µV		±25		%
Input Bandwidth (Note 3)				400		kHz
Power-Up Time		Measured from V_{DD} > 2.6V and V_{IO} > 1.5V and PDNB deasserted to SMBus port active		4		ms
ACCURACY						
Current Sample Resolution		V_{SENSE} < 10mV		16		Bits
Voltage Sample Resolution				14		Bits
Current-Sense Full Scale Voltage				100		mV
Voltage-Sense Full Scale				24		V
Power Measurement Accumulation Accuracy (1 Sigma Error Range with > 1000 Accumulations) (Note 3, Note 4)		V_{SENSE} = 97mV		±0.8		%
		V_{SENSE} = 10mV		±1		
		V_{SENSE} = 1mV		±1.5		
		V_{SENSE} = 100µV		±2.2		
		V_{SENSE} = 50µV		±3.5		
LOGIC INPUT/OUTPUT						
Input Logic-High (SCL/SDA/PDNB/SLOW)	V_{IH}		0.7 x VIO			V
Input Logic-Low (SCL/SDA/PDNB/SLOW)	V_{IL}				0.3 x V_{IO}	V
SDA Output Logic-Low	V_{OL}	I_{OL} = 4mA			0.4	V
SDA Output Leakage					±1	µA
SCL, SDA Leakage					±5	µA
SLOW, PDNB Leakage					±1	µA
I^2C/SMBUS INTERFACE (V_{IO} = 3.3V)						
SCL Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		500			ns

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 3.6V, V_{IO} = 1.6V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C. Limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time (Repeated) START Condition	$t_{HD:STA}$		260			ns
Low Period of SCL	t_{LOW}		500			ns
High Period of SCL	t_{HIGH}		260			ns
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	0		150	
Data Setup Time	$t_{SU:DAT}$		50			ns
Start Setup Time	$t_{SU:STA}$		260			ns
SDA and SCL Rise Time	t_R				120	ns
SDA and SCL Fall Time	t_F		3		120	ns
Stop Setup Time	$t_{SU:STO}$		260			ns
Noise Spike Reject	t_{SP}			25		ns

Note 1: SMBus not active.
Note 2: Input bias current varies with V_{SENSE} (IN+ - IN-) voltage. See the *Typical Operating Characteristics* section for details.
Note 3: Estimated from simulation, not production tested.
Note 4: Includes gain error, offset error, and quantization error.
Note 5: For control byte (6) = 0, the sample rate is 1ksps. For control byte (6) = 1, the sample rate is 1.5ksps.

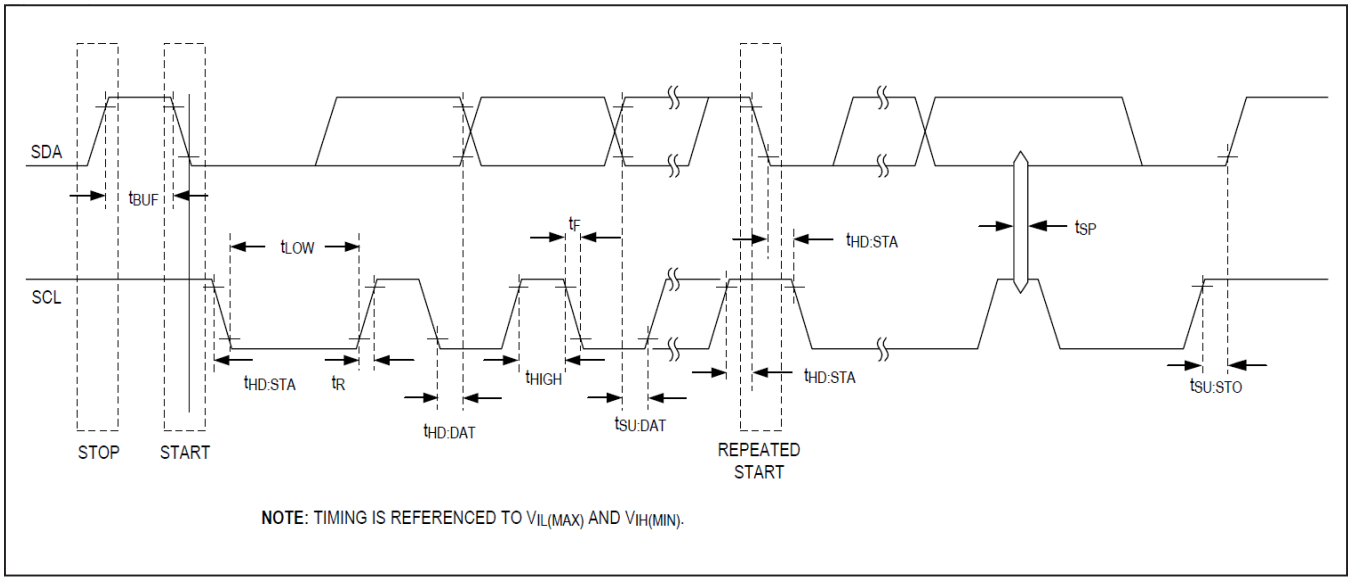
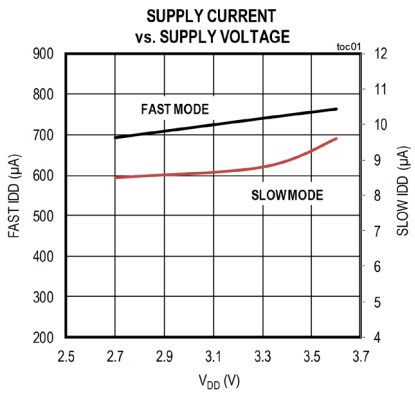
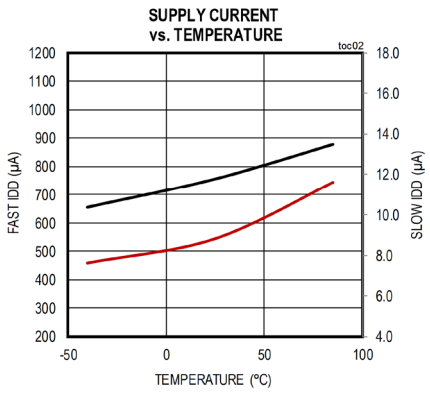


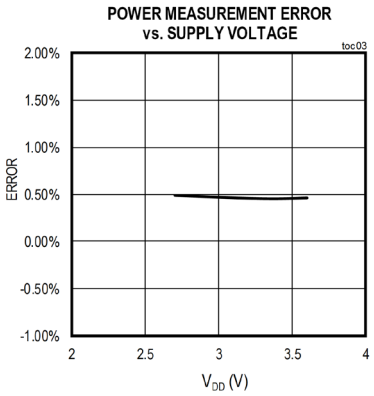
Figure 1. I²C/SMBus Timing Diagram

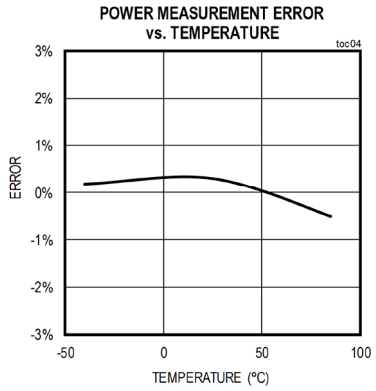
Typical Operating Characteristics

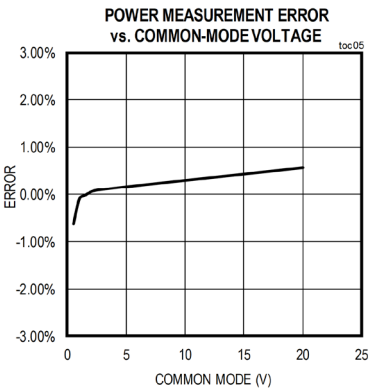
V_{DD} = V_{IO} =3.3V, T_A = +25C, V_{CM} = 3.8V, V_{SENSE} = 1mV

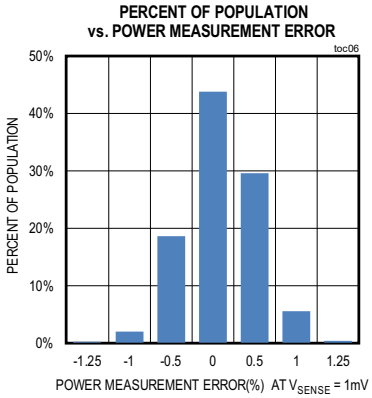


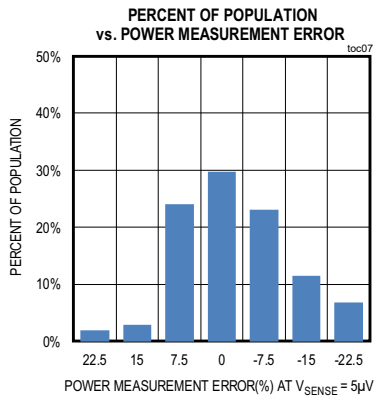


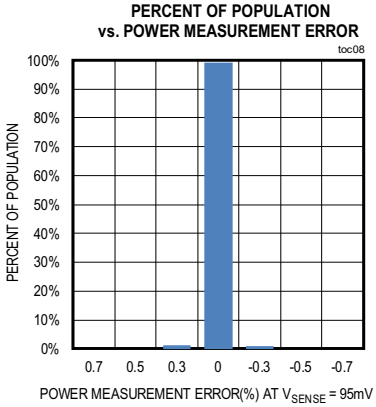


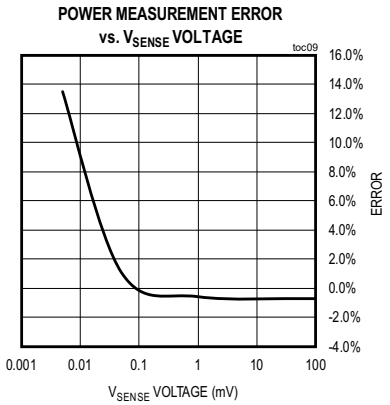






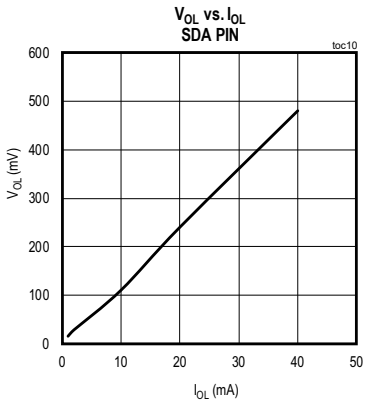


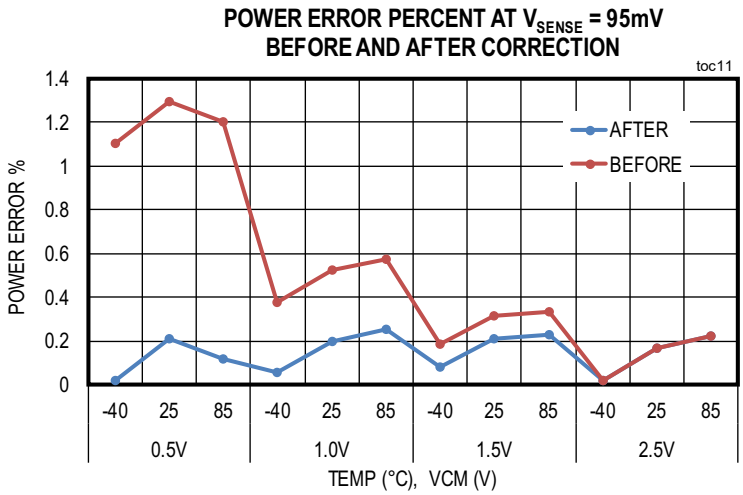


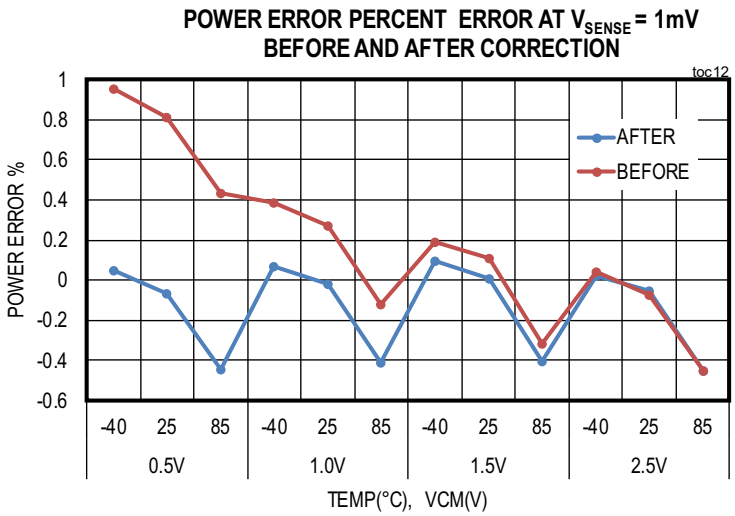


Typical Operating Characteristics

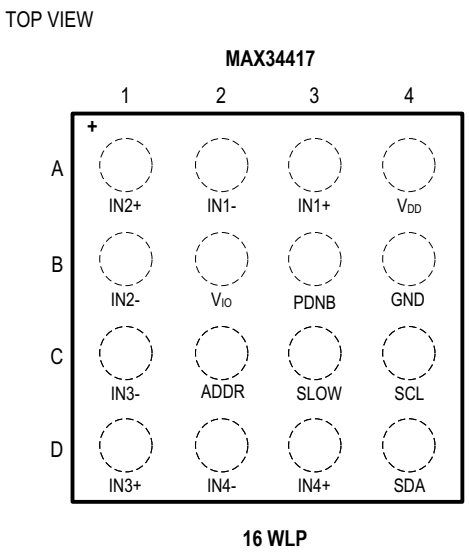
V_{DD} = V_{IO} =3.3V, T_A = +25C, V_{CM} = 3.8V, V_{SENSE} = 1mV







Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	IN2+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 2. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
A2	IN1-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 1. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
A3	IN1+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 1. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
A4	V_{DD}	Supply Voltage for Current-Sense Amplifiers. +2.7V to +3.6V supply. This pin should be decoupled to GND with a minimum 100nF ceramic capacitor. Power can be applied to V_{DD} either before or after or in the absence of V_{IO}.
B1	IN2-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 2. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
B2	V_{IO}	Supply Voltage for Digital Interface. +1.6V to +3.6V supply. This pin should be decoupled to GND with a minimum 100nF ceramic capacitor. Power can be applied to V_{IO} either before or after or in the absence of V_{DD}.
B3	PDNB	Power-Down Mode Input. When this pin is tied low, the device is completely powered down including the I^2C/SMBus interface.
B4	GND	Ground Connection

Pin Description (continued)

PIN	NAME	FUNCTION
C1	IN3-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 3. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
C2	ADDR	I²C/SMBus-Compatible Address Select Input. A resistor tied to GND from this pin selects the SMBus slave address. See the Addressing section for more details.
C3	SLOW	Slow Accumulate Mode Input. When this pin is tied high, the power accumulation is slowed to reduce overall device power consumption.
C4	SCL	I²C/SMBus-Compatible Clock Input. SCL does not load the SMBus when either V_{DD} or V_{IO} is not present.
D1	IN3+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 3. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
D2	IN4-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 4. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
D3	IN4+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 4. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
D4	SDA	I²C/SMBus-Compatible Data Input/Output. Output is open drain. SDA does not load the SMBus when either V_{DD} or V_{IO} is not present.

Detailed Description

The MAX34417 automatically sequences through the channels to collect samples from the common-mode voltage and the current-sense amplifiers. The 16-bit current value and the 14-bit voltage value are then multiplied to create a 30-bit power value that is then written to the power accumulator.The MAX34417 contains a 56-bit power accumulator for each channel. This accumulator is updated 1024 times per second. When the host is ready to pull the latest accumulation data, it first sends the update command that causes the MAX34417 to load the latest accumulation data and accumulation count into the internal MAX34417 registers so the host can read them at any time. This type of operation allows the host to control the accumulation period. The only constraint is that the host should access the data before the accumulators can overflow. If the accumulators overflow, they do not roll over.

The MAX34417 contains a 14-bit ADC for voltage and a 13-bit ADC for current. During each sample time, a 14-bit voltage sample and a 16-bit current sample are resolved. To create a 16-bit current value from the 13-bit ADC, the device takes two current samples; one with the current sense amplifier in a high-gain mode and another with the amplifier in a low-gain mode. The high gain setting is 8 times the low-gain setting. Based on the two current-sense ADC results, the device determines which result provides the best accuracy and fills the 16-bit current sample accordingly.

SMBus operation

The MAX34417 uses the SMBus command/response format as described in the System Management Bus Specification Version 2.0. The structure of the data flow between the host and the slave is shown below for several different types of transactions. Data is sent MSB first. The fixed slave address of the MAX34417 is determined on device power-up by sampling the resistor tied to the ADDR pin. See the *Slave Address Setting* section for details. On device power-up, the device defaults to the control command code (01h). If the host sends an invalid command code, the device does not acknowledge (NACK) the command code. If the host attempts to read the device with an invalid command code, all ones (FFh) are returned in the data byte.

Table 1. Read Byte Format

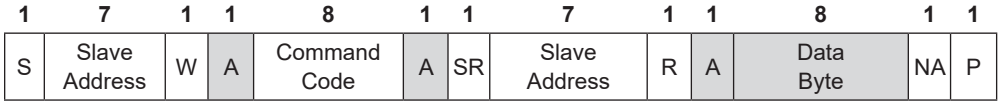


Table 2. Write Byte Format

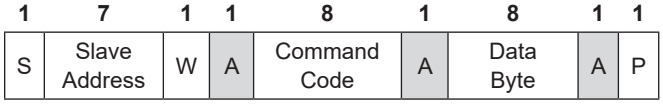


Table 3. Send Byte Format

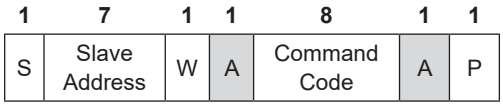


Table 4. Block Read Format

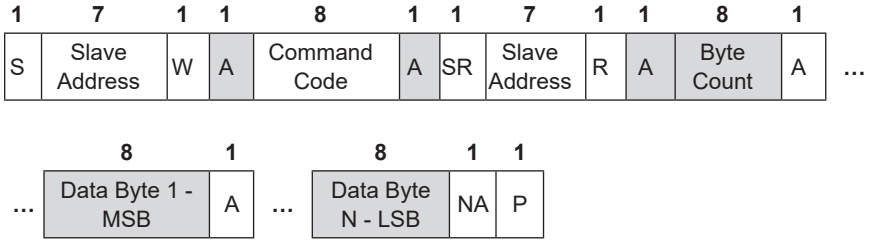
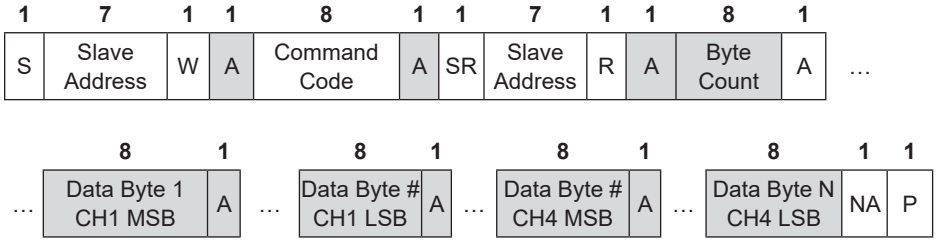


Table 5. Bulk Read Format



Note: In multibyte reads, the most significant byte is the first Data Byte read.

Key:	N = Number of bytes from Table 7
S = Start	R = Read Bit (1)
SR = Repeated Start	A = Acknowledge (0)
P = Stop	NA = Not Acknowledge (1)
W = Write Bit (0)	Shaded Block = Slave Transaction

Slave Address Setting

The MAX34417 responds to receiving it's fixed slave address by asserting an ACK on the bus. The fixed slave address of the MAX34417 is determined on device power up by sampling the voltage across a resistor tied to the ADDR pin after V_{DD} rises to a valid value. See the table below for more details. The device will not respond to a general call address. It will be activated only when receiving its fixed slave address or the broadcasting address, 2Ch, for Global Update. Upon sending "00" to slave address 2Ch, all MAX34417 ICs connecting to the I^2C will be updated.

On power up or when PDNB toggles from low to high, a current of 100µA is applied to the RADDR and the voltage is measured. The binary slicing value is compared to the ADC result. An ADC value that is below the slicing value but not below the adjacent lower slicing value selects the Slave Address. The selected values will tolerate a total error of ±30% in the measurement to account for errors in the current value, resistor value, ADC gain error, etc.. As shown, the 3 LSB of the ADC value are not needed for the comparison.

Table 6. SMBUS Slave Address Select

RADDR (±1%) (Ω)	SLAVE ADDRESS	SLICING VOLTAGE	SLICING ADC VALUE	VOLTAGE RANGE (MV)
Tie to ground	001 0000 (10h)			0 – 35
499	001 0010 (12h)	35mV	'000001001000	35 – 65
931	001 0100 (14h)	65mV	'000010000000	65 – 120
1740	001 0110 (16h)	120mV	'000011111000	120 – 224
3160	001 1000 (18h)	224mV	'000111001000	224 – 416
5900	001 1010 (1Ah)	416mV	'001101010000	416 – 772
11000	001 1100 (1Ch)	772mV	'011000110000	772 – 1433
20500	001 1110 (1Eh)	1433mV	'101101111000	1433 – V_{DD}

Command Codes

Table 7. Command Codes

COMMAND CODE	NAME	DETAILED DESCRIPTION	TYPE	NUMBER OF BYTES	POR (NOTE 1)
00h	UPDATE	Request Accumulator Update	Send Byte	0	-
01h	CONTROL	Device Configuration and Status	R/W Byte	1	00h
02h	ACC_COUNT	Accumulator Counter	Block Read	3	Note 2
03h	PWR_ACC_1	Power Accumulator for Channel 1	Block Read	7	Note 2
04h	PWR_ACC_2	Power Accumulator for Channel 2	Block Read	7	Note 2
05h	PWR_ACC_3	Power Accumulator for Channel 3	Block Read	7	Note 2
06h	PWR_ACC_4	Power Accumulator for Channel 4	Block Read	7	Note 2
07h	V_CH1	Voltage for Channel 1	Block Read	2	Note 2
08h	V_CH2	Voltage for Channel 2	Block Read	2	Note 2
09h	V_CH3	Voltage for Channel 3	Block Read	2	Note 2
0Ah	V_CH4	Voltage for Channel 4	Block Read	2	Note 2
0Fh	DID	Device ID and Revision	Read Byte	1	Note 3
00h	BULK UPDATE	Slave address = 2Ch followed by command code = 00h	Send Byte	0	Note 4
10h	Bulk Power Readout	Read all accumulators in bulk mode starting with channel 1	Bulk Read	28	Note 5
11h	Bulk Voltage Readout	Read all voltages in bulk mode starting with channel 1	Bulk Read	8	

Notes:

1) The acronym POR means Power-On Reset and this is the default value when power is applied to the device.
2) These registers are set to all zeros upon POR.
3) The Device ID is factory set and will vary based on the die revision.
4) Slave Address 2Ch is a broadcast address for Global Update to all MAX34417.
5) 28 bytes if Control[7] = 1, else, 24 byte

Command Codes Bit Description

Update (00h) – Send Byte

The update send byte command does not contain any data. The UPDATE command must be sent to the device before reading any of the other commands, and it must be sent after writing to the CONTROL command. After sending the UPDATE command, the host should wait at least 1msec before reading any command. Each time the device receives this command, it completes an accumulation cycle for the four channels (if not already complete) and then it transfers all of the accumulation data in the power accumulators and the accumulator counter to a set of registers that can be read with the SMBus interface and it resets all of the counters/accumulation registers. An update command does not clear the OVF bit.

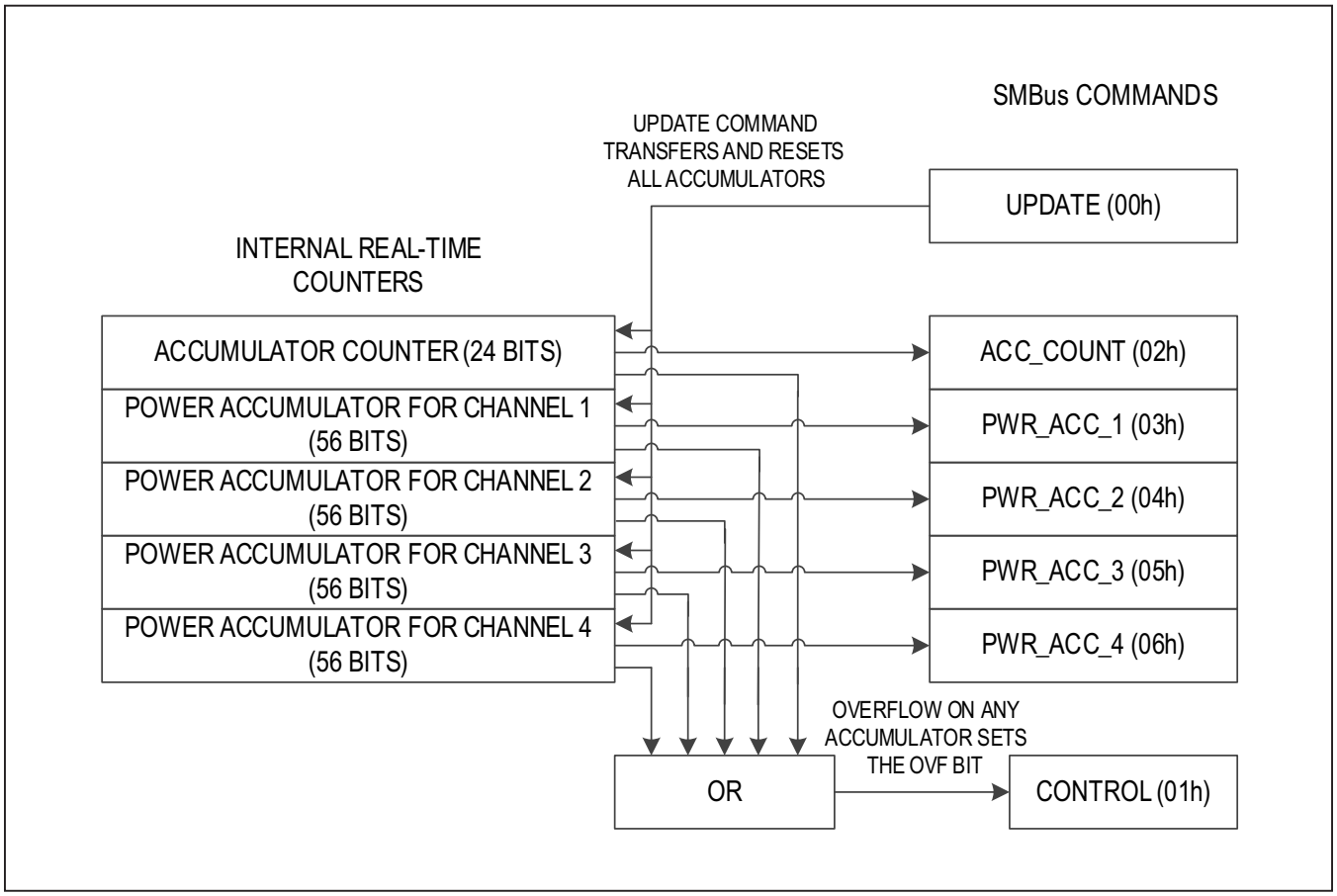


Figure 2. MAX34417 SMBus Register Structure

Control (01h) – R/W Byte

Table 8. Control (01h)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	Mode	CAM	SMM	PARK_EN	PARK1	PARK0	SLOW	OVF
POR:	0	0	0	0	0	0	0	0

Bit 7: MAX34407/MAX34417

When this bit is at 0, the accumulators are 48-bits wide and the voltage readout is 12-bit left-justified to a 16-bit field. The power calculated is still 30-bit wide. When the bit is set, the accumulators are 56 wide and the voltage readout is 14 bit left-justified to a 16-bit field.

0 = MAX34407

1 = MAX34417

Bit 6: CAM

Continuous Accumulate Mode. When this bit is set, the inputs are measured and accumulated continuously without idle periods. After setting this bit, an UPDATE command must be issued to start the accumulation cycles. The subsequent UPDATE command will move the data to the SMBus registers, reset the accumulators, and start the continuous accumulation cycle process. SMM and CAM modes should not be enabled at the same time.

0 = CAM mode not active.

1 = CAM Mode enabled.

Note that changing any Control byte settings while CAM bit is enabled is disallowed. If CAM mode must be set, the Control byte must be set to desired values with CAM = 0, then followed by an UPDATE. After this, the CAM mode bit can be set and another UPDATE must be sent.

Bit 5: SMM

Single Measure Mode. When this bit is set, the device will perform only one measure and accumulation cycle for the four input channels (normal scan mode) or four samples of one channel in Park mode in response to an UPDATE command. The data can be read by issuing another UPDATE command which moves the previous UPDATE data into the SMBus read registers and starts another measurement cycle. Data should be read between UPDATE commands. UPDATE commands should be no less than 1msec apart for reliable measurements. The power accumulators remain at 56-bits even though the single calculated power is a 30-bit value. After the SMM bit is changed, the UPDATE command should be sent to reset the accumulators and perform the selected scan operation. SMM and CAM modes should not be enabled at the same time.

0 = Normal scan and accumulate operation.

1 = SMM Mode enabled.

Bit 4: PARK_EN

This bit enables the channel park feature. If this bit is set, only one channel will be enabled and the device will sample the selected channel four times faster than the normal round-robin rate. The channel to monitor is selected with the PARK0 and PARK1 bits. After the PARK_EN bit is changed, the UPDATE command should be sent to clear out the accumulators and start a new accumulation period. When the channel park feature is enabled, the minimum time before the power accumulators can overflow reduces by a factor of four since the selected channel is being updated four times faster. Also, the power accumulators for the disabled channels do not contain any meaningful data.

0 = Round Robin Sampling of All Four Channels.

1 = One Channel Selected (with the PARK0/1 bits).

Bits 3 to 2: PARK1 to PARK0

If the PARK_EN (Park Enable) bit is set, then these bits select which channel is to be monitored at the exclusion of the other channels.

Table 9. PARK Channel Selectiion

PARK1	PARK0	SELECTED CHANNEL
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

Bit 1: SLOW

This bit is logically OR'ed with the SLOW input pin. If either this bit is set or the SLOW pin is high, then the power accumulation calculation rate is slowed in order to lower the power consumption of the device.

Bit 0: OVF

This status bit will be set to a one if any of the power accumulators or the accumulator counter reach overflow. When the accumulators or counter overflow, they will not rollover. Any active sequencing or accumulation mode will stop and the device will halt in the idle state. A UPDATE command will clear the accumulators and the accumulation counter, thus clearing the OVF condition, as well as resuming the selected accumulation mode sequence. The OVF bit in the control register is not cleared by an UPDATE command. This status bit must be cleared by writing a 0.

Accumulator Counter (02h) – Block Read

Table 10. Accumulator Counter (02h)

	BIT 23	**BIT 22**	**BIT 21**	**BIT 20**	**BIT 19**	**BIT 18**	**BIT 17**	**BIT 16**
NAME:	CNT23	CNT22	CNT21	CNT20	CNT19	CNT18	CNT17	CNT16
POR:	0	0	0	0	0	0	0	0
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
NAME:	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8
POR:	0	0	0	0	0	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
NAME:	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
POR:	0	0	0	0	0	0	0	0

Bits 23 to 0: CNT23 to CNT0

These bits report the number of accumulations since the last UPDATE command. The UPDATE command copies the count into this I2C data register. By dividing the total accumulated power reported in each power accumulator by this count, the average power can be determined. The accumulator counter does not rollover.

Power Accumulator for Channel 1 (03h) – Block Read

Power Accumulator for Channel 2 (04h) – Block Read

Power Accumulator for Channel 3 (05h) – Block Read

Power Accumulator for Channel 4 (06h) – Block Read

Table 11. Power Accumulator

NAME:	BIT 55	BIT 54	BIT 53	BIT 52	BIT 51	BIT 50	BIT 49	BIT 48
POR:	ACC55	ACC54	ACC53	ACC52	ACC51	ACC50	ACC49	ACC48
	0	0	0	0	0	0	0	0
	Bit 47	**Bit 46**	**Bit 45**	**Bit 44**	**Bit 43**	**Bit 42**	**Bit 41**	**Bit 40**
NAME:	ACC47	ACC46	ACC45	ACC44	ACC43	ACC42	ACC41	ACC40
POR:	0	0	0	0	0	0	0	0
	Bit 39	**Bit 38**	**Bit 37**	**Bit 36**	**Bit 35**	**Bit 34**	**Bit 33**	**Bit 32**
NAME:	ACC39	ACC38	ACC37	ACC36	ACC35	ACC34	ACC33	ACC32
POR:	0	0	0	0	0	0	0	0
	Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
NAME:	ACC31	ACC30	ACC29	ACC28	ACC27	ACC26	ACC25	ACC24
POR:	0	0	0	0	0	0	0	0
	Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
NAME:	ACC23	ACC22	ACC21	ACC20	ACC19	ACC18	ACC17	ACC16
POR:	0	0	0	0	0	0	0	0
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
NAME:	ACC15	ACC14	ACC13	ACC12	ACC11	ACC10	ACC9	ACC8
POR:	0	0	0	0	0	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
NAME:	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
POR:	0	0	0	0	0	0	0	0

Bits 55 to 0: ACC55 to ACC0

These bits report the total power accumulated by each channel. The UPDATE command moves the data in the accumulators into these registers in the I^2C logic from where they are read. The power accumulators will not rollover. This is an unsigned, binary number. If the value in the accumulator is negative, this register will read 000000000000h.

Voltage for Channel 1 (07h) – Block Read

Voltage for Channel 2 (08h) – Block Read

Voltage for Channel 3 (09h) – Block Read

Voltage for Channel 4 (0Ah) – Block Read

Table 12. Voltage Read

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
NAME:	V13	V12	V11	V10	V9	V8	V7	V6
POR:	0	0	0	0	0	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
NAME:	V5	V4	V3	V2	V1	V0	0	0
POR:	0	0	0	0	0	0	0	0

Bits 15 to 2: V13 to V0

These bits report the voltage on the IN- pin of each channel at the approximate time of the last UPDATE command. It is an unsigned, binary value. The 14-bit value is in bits 15:2.

Device ID and Revision Register (0Fh) – Read Byte

Table 13. Device ID and Revision

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	ID4	ID3	ID2	ID1	ID0	REV2	REV1	REV0
POR:	0	0	1	1	1	Factory set		

Device ID and Revision Register (0Fh)

Bits 7 to 3: ID4 to ID0

These bits report the device identification (ID). The ID is fixed at 07h.

Bits 2 to 0: REV2 to REV0

These bits report the device revision. The device revision is factory set.

Bulk Update (00h)

When sending 00 to slave address 2Ch, all devices on the I2C bus will be updated.

Bulk Power Readout (10h)

Read accumulated power data for all four channels, 7bytes for each channel with channel 1 MSB first and channel 4 LSB last, total 28bytes.

Bulk Power Readout (11h)

Read all voltage data for four channels, 2 bytes each for each channel with channel 1 MSB first and channel 4 LSB last, total 8 bytes.

Applications Information

Average Power Calculation Example

The average power can be derived in an external calculation, as shown below, if the current sense resistor value is known.

Power accumulator (56 bit) = 000001CEFBD314h (7767577364 decimal)

Accumulator counter (24 bit) = 0005DEh (1502 decimal)

Current-sense resistor = 10mΩ

Step 1

Calculate the unscaled average power by dividing the power accumulator value with the accumulator count value:

000001CEFBD314h/0005DEh = 4EE921h (5171489 decimal)

Step 2

Calculate the ratio of the Step 1 result to the calculated power full-scale value which is a 30-bit value:

$5171489/2^{30} = 0.004816324$

Step 3

Multiply the result from Step 2 by the correction factor listed in Table 14 that matches the current-sense resistor value:

0.004816324 x 240 = 1.156W

Perr_Verr Correction

When the $V_{CM} \leq 2.0V$, a correction can be applied to improve power accuracy. The correction must be used only when greater than or equal to 1000 samples are accumulated to avoid truncation errors from integer math if done on a microcontroller platform.

ACCUMULATOR = Accumulator reading for a channel

ACCUM_COUNT = Accumulator count reading from the device

VOLTAGE = Voltage reading for a channel.

The steps include

1) Power = ACCUMULATOR/ACCUM_COUNT
2) Current = Power/(VOLTAGE/4)
3) Adjusted Voltage, V_{ADJ} = VOLTAGE/4 – V_{ERR}, where V_{ERR} is as shown below.
   a. $V_{ERR} = 3$ if $0.5 \leq V_{CM} < 1.0$
   b. $V_{ERR} = 2$ if $1.0 \leq V_{CM} < 1.5$
   c. $V_{ERR} = 1$ if $1.5 \leq V_{CM} < 2.0$
4) Adjusted Power, P_{ADJ} = Current x V_{ADJ}
5) Adjusted Accumulator = P_{ADJ} x ACCUM_COUNT

If there is a residue from operation ‘2’ above, it may be added to P_{ADJ} in step 5.

Table 14. Correction Factors for Various Current-Sense Resistor Values

CURRENT-SENSE RESISTOR VALUE (MΩ)	FULL-SCALE CURRENT (A)	FULL-SCALE VOLTAGE (V)	POWER SCALE CORRECTION CALCULATION	POWER SCALE CORRECTION FACTOR (W)
100	1	24	1 x 24	24
50	2	24	2 x 24	48
40	2.5	24	2.5 x 24	60
25	4	24	4 x 24	96
20	5	24	5 x 24	120
15	6.66667	24	6.667 x 24	160
10	10	24	10 x 24	240
5	20	24	20 x 24	480
4	25	24	25 x 24	600
2	50	24	50 x 24	1200
1	100	24	100 x 24	2400

Kelvin Sense

For best performance, a Kelvin sense arrangement is recommended (see Figure 2). In a Kelvin sense arrangement, the voltage-sensing nodes across the sense element are placed so that they measure the true voltage drop across the sense element and not any additional excess voltage drop that can occur in the copper PCB traces or the solder mounting of the sense element. Routing the differential sense lines along the same path to the MAX34417 and keeping the path short also improve the system performance.

Minimizing Trace Resistance

PCB trace resistance from the sense resistor (RSENSE) to the IN- inputs can affect the MAX34417 power measurement accuracy. Every 1Ω of PCB trace resistance in the IN- path will add about 25µV of offset error. It is recommended to place the sense resistors as close as possible to the MAX34417 and not to use minimum width PCB traces. When placing an RC filter at the input, the resistor must be placed in the IN+ input path to reduce DC errors from the trace resistance.

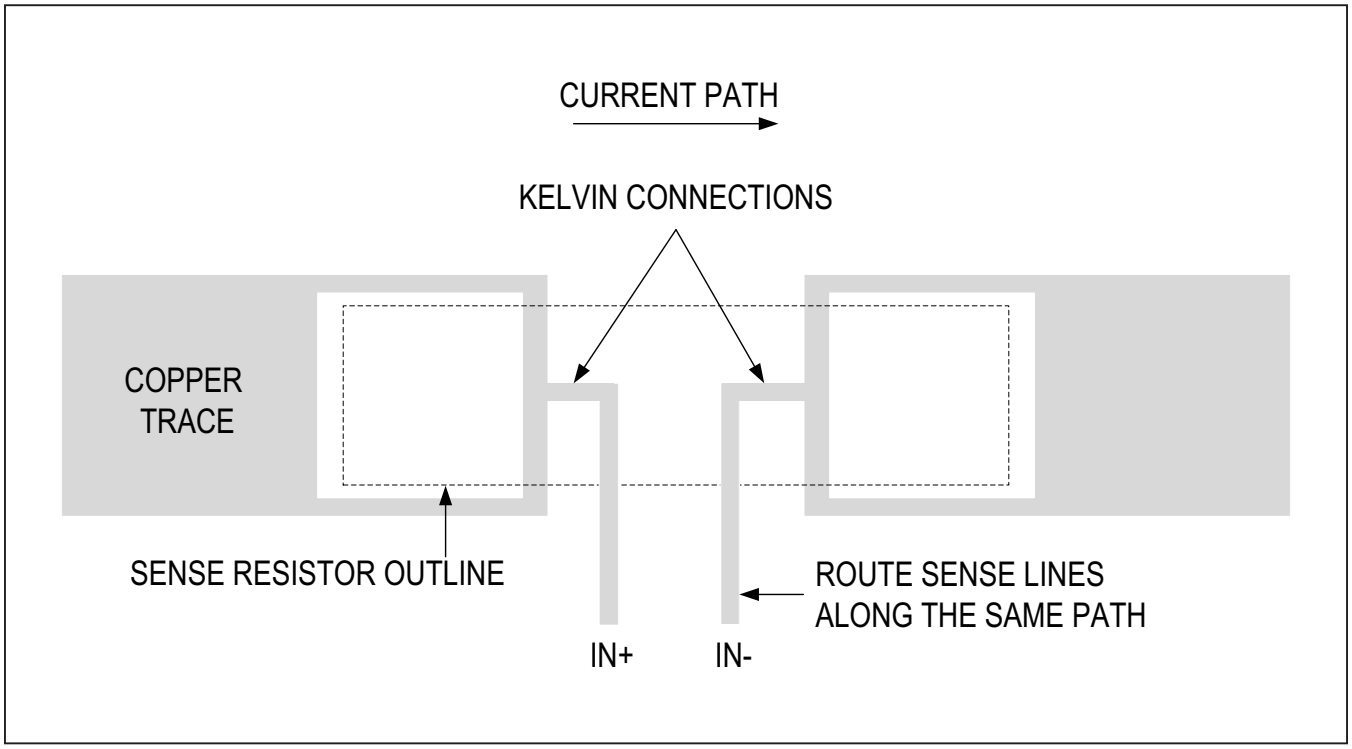


Figure 3. Kelvin Sense Connection Layout Example

Top Marking

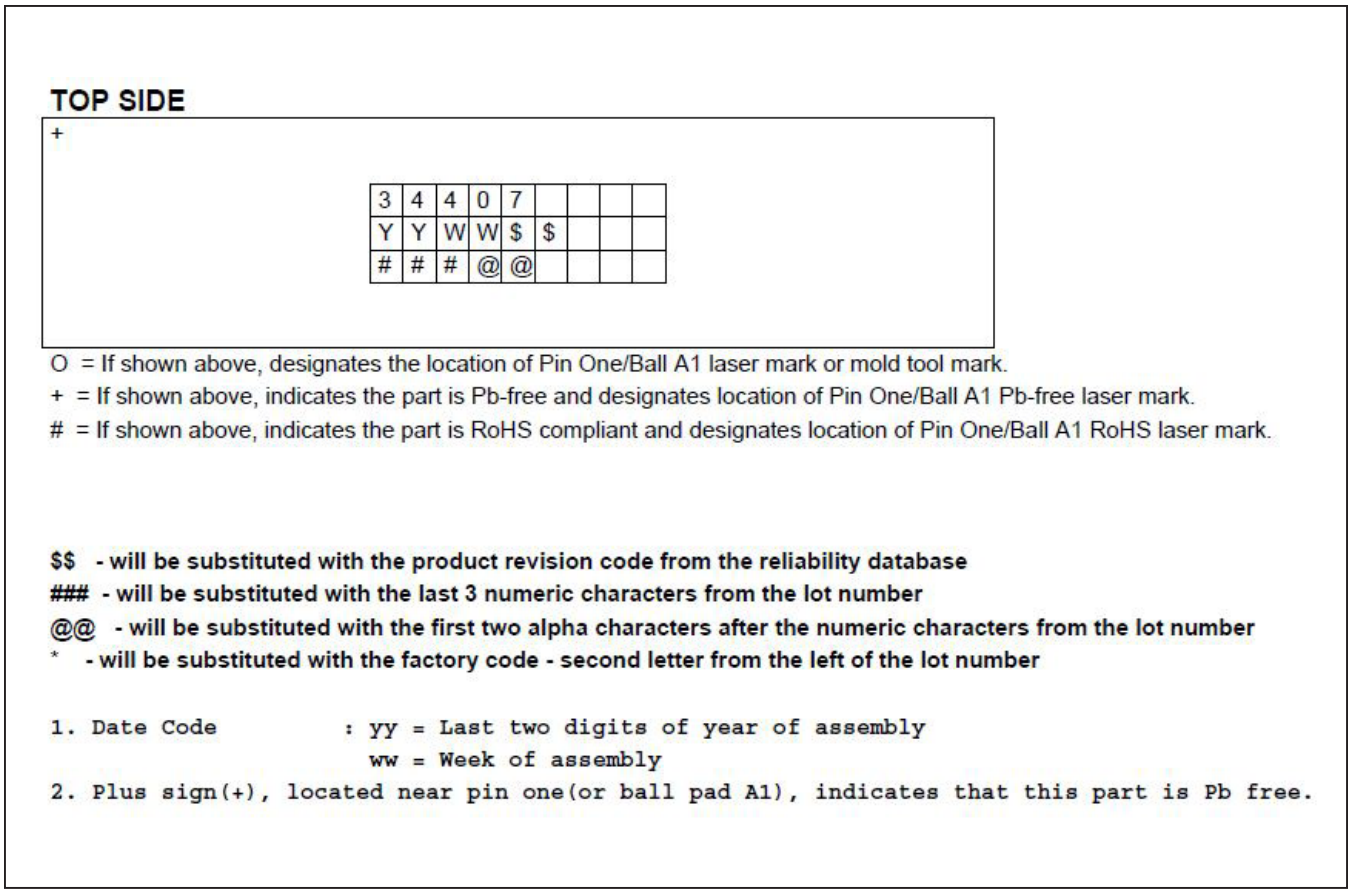
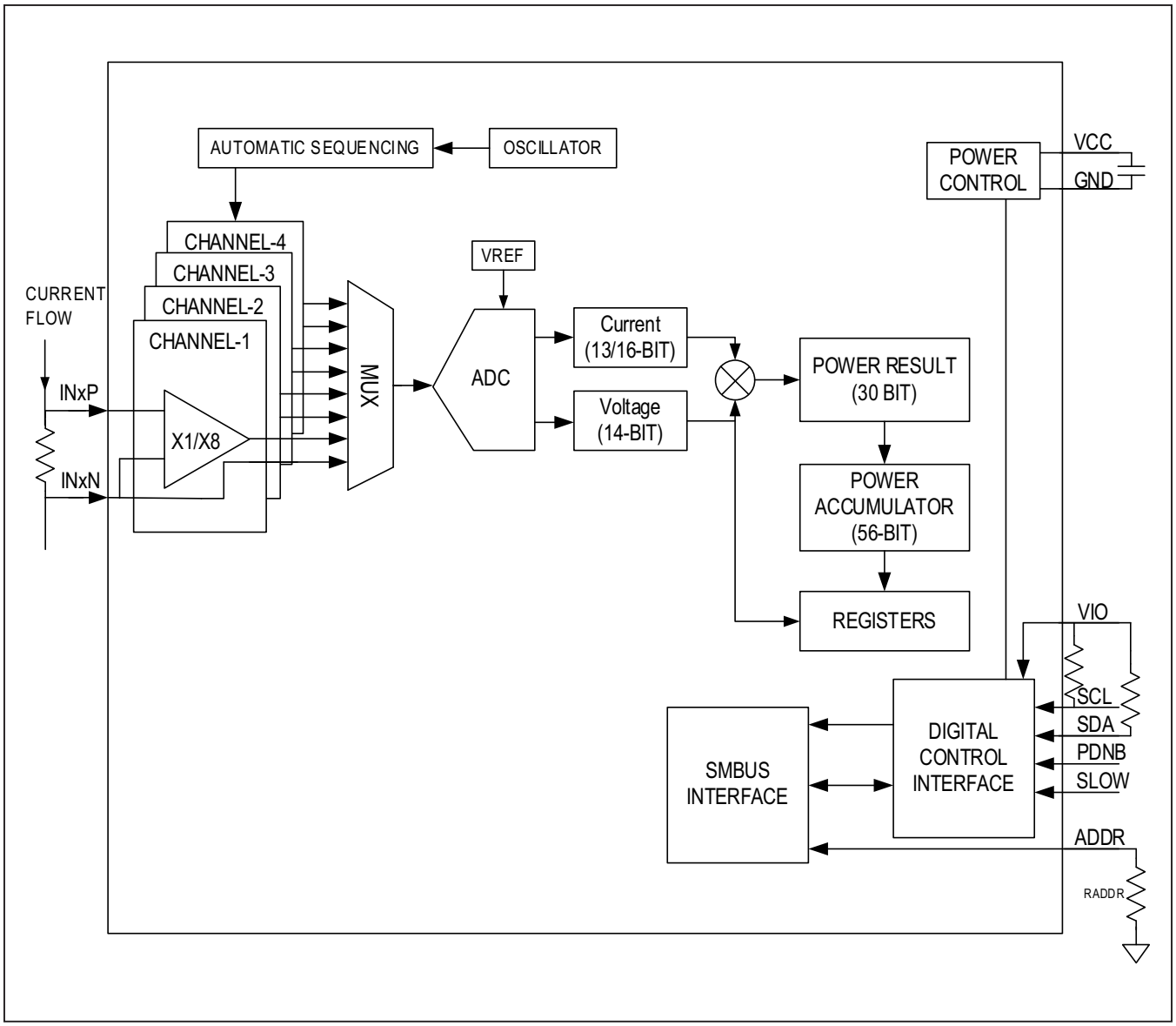


Figure 4. Top Mark

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX34417ENE+	-40°C to +85°C	16 Thin-WLP with 0.4mm Pitch
MAX34417ENE+T	-40°C to +85°C	16 Thin-WLP with 0.4mm Pitch

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—
1	6/18	Updated *Electrical Characteristics* table, *Typical Operating Characteristics*, Table 5, Table 7, *Command Codes Bit Description*, Table 12, Table 13, and *Applications Information* section	5–7, 10, 13, 17, 18
2	9/18	Updated *Typical Operating Characteristics*	6, 7

