

# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

## ABSOLUTE MAXIMUM RATINGS

BATT, PWM, POK, COMP,  $\overline{\text{SHDN}}$  to GND .....-0.3V to +6V  
 PGND to GND .....-0.3V to +0.3V  
 LX, REF, FB to GND .....-0.3V to ( $V_{\text{BATT}} + 0.3\text{V}$ )  
 Continuous Power Dissipation ( $T_{\text{A}} = +70^{\circ}\text{C}$ )  
 10-Pin  $\mu\text{MAX}$  (derate 5.6mW/ $^{\circ}\text{C}$  above  $+70^{\circ}\text{C}$ ) .....444mW

Operating Temperature Range .....-40 $^{\circ}\text{C}$  to +85 $^{\circ}\text{C}$   
 Junction Temperature .....+150 $^{\circ}\text{C}$   
 Storage Temperature Range .....-65 $^{\circ}\text{C}$  to +150 $^{\circ}\text{C}$   
 Lead Temperature (soldering, 10s) .....+300 $^{\circ}\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{\text{BATT}} = 3.6\text{V}$ ,  $\overline{\text{SHDN}} = \text{BATT}$ ,  $C_{\text{REF}} = 0.1\mu\text{F}$ ,  $T_{\text{A}} = 0^{\circ}\text{C}$  to +85 $^{\circ}\text{C}$ , unless otherwise noted. Typical values are at  $T_{\text{A}} = +25^{\circ}\text{C}$ .)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Input Voltage		2.6		5.5	V
Undervoltage Lockout Threshold	$V_{\text{BATT}}$ rising or falling (35mV hysteresis)	2.15	2.35	2.55	V
Quiescent Current	No load, pulse skipping, PWM = GND		140	240	$\mu\text{A}$
	1MHz switching		2		mA
Quiescent Current in Dropout			190	340	$\mu\text{A}$
Shutdown Supply Current	$\overline{\text{SHDN}} = \text{GND}$		0.1	10	$\mu\text{A}$
<b>REFERENCE AND ERROR AMP</b>					
FB Voltage Accuracy	MAX1927R	0.738	0.75	0.762	V
	MAX1928-15	1.477	1.5	1.523	
	MAX1928-18	1.773	1.8	1.827	
	MAX1928-25	2.462	2.5	2.538	
FB Input Current	MAX1928	5	10	15	$\mu\text{A}$
	MAX1927R		10	150	nA
Transconductance ( $g_m$ )	MAX1927R		250		$\mu\text{S}$
	MAX1928-15		210		
	MAX1928-18		175		
	MAX1928-25		125		
Reference Voltage Accuracy		1.231	1.25	1.269	V
Reference Supply Rejection	$2.6\text{V} < V_{\text{BATT}} < 5.5\text{V}$		0.5	2	mV
<b>PWM CONTROLLER</b>					
P-Channel On-Resistance	$V_{\text{BATT}} = 3.6\text{V}$		0.25	0.4	$\Omega$
	$V_{\text{BATT}} = 2.6\text{V}$		0.3	0.5	
N-Channel On-Resistance	$V_{\text{BATT}} = 3.6\text{V}$		0.17	0.3	$\Omega$
	$V_{\text{BATT}} = 2.6\text{V}$		0.2	0.35	
Current-Sense Transresistance ( $R_{\text{CS}}$ )			0.48		V/A
P-Channel Current-Limit Threshold		1.1	1.3	1.6	A
P-Channel Pulse-Skipping Current Threshold		0.11	0.13	0.15	A
N-Channel Negative Current-Limit Threshold			-0.55		A

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MAX1927/MAX1928

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{BATT} = 3.6V$ ,  $\overline{SHDN} = BATT$ ,  $C_{REF} = 0.1\mu F$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
N-Channel Synchronous Rectifier Turn-Off Threshold			20		mA
LX Leakage Current	$V_{BATT} = 5.5V$ , LX = GND or BATT	-20	0.1	+20	$\mu A$
Maximum Duty Cycle		100			%
Minimum Duty Cycle	PWM = GND			0	%
	PWM = BATT		15		
Internal Oscillator Frequency		0.85	1	1.15	MHz
Thermal Shutdown Threshold	15°C hysteresis		160		Degrees
<b>POK COMPARATOR</b>					
BATT Operating Voltage Range	$I_{POK} = 0.1 mA$	1		5.5	V
Output Low Voltage	$V_{FB} = 0.5V$ , $I_{POK} = 1mA$		0.01	0.1	V
Output High Leakage Current	$V_{POK} = 5.5V$			1	$\mu A$
POK Threshold	MAX1927R	0.650	0.675	0.700	V
	MAX1928-15	1.305	1.350	1.395	
	MAX1928-18	1.566	1.620	1.674	
	MAX1928-25	2.175	2.250	2.325	
Output Valid to POK Release Delay	POK transitions to high impedance 20ms after $V_{FB} > V_{POK}$	15	20	25	ms
<b>LOGIC INPUTS (<math>\overline{SHDN}</math>, PWM)</b>					
Logic Input High	$2.6V < V_{BATT} < 5.5V$	1.6			V
Logic Input Low	$2.6V < V_{BATT} < 5.5V$			0.6	V
Logic Input Current	$V_{BATT} = 5.5V$		0.1	1	$\mu A$

## ELECTRICAL CHARACTERISTICS

( $V_{BATT} = 3.6V$ ,  $\overline{SHDN} = BATT$ ,  $C_{REF} = 0.1\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
BATT Input Voltage		2.6	5.5	V
Undervoltage Lockout Threshold	$V_{BATT}$ rising or falling (35mV hysteresis)	2.15	2.55	V
Quiescent Current	No load, pulse skipping, PWM = GND		240	$\mu A$
Quiescent Current in Dropout			340	$\mu A$
Shutdown Supply Current	$\overline{SHDN} = GND$		10	$\mu A$
<b>REFERENCE AND ERROR AMP</b>				
FB Voltage Accuracy	MAX1927R	0.732	0.768	V
	MAX1928-15	1.47	1.53	
	MAX1928-18	1.764	1.836	
	MAX1928-25	2.45	2.55	
FB Input Current	MAX1928	5	15	$\mu A$

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{BATT} = 3.6V$ ,  $\overline{SHDN} = BATT$ ,  $C_{REF} = 0.1\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

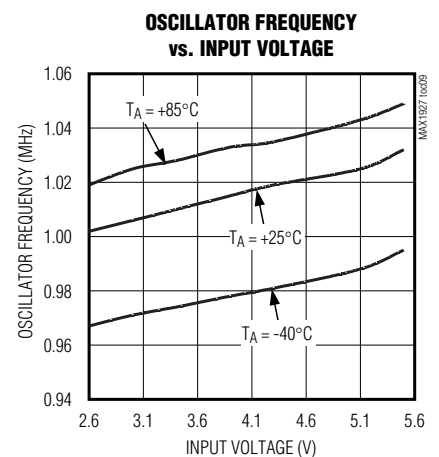
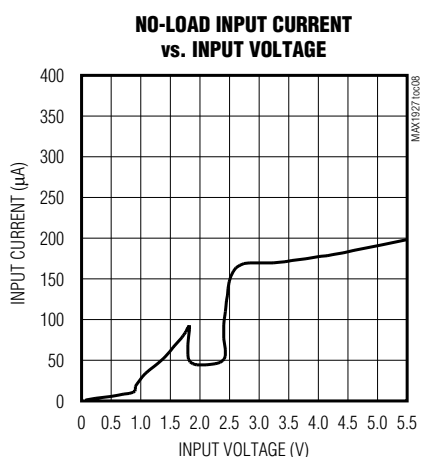
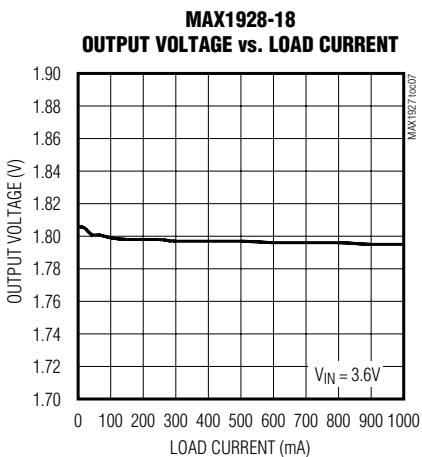
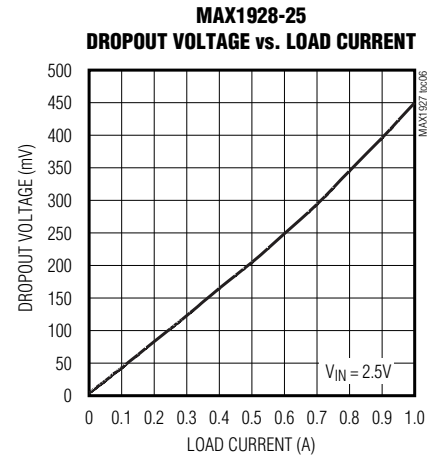
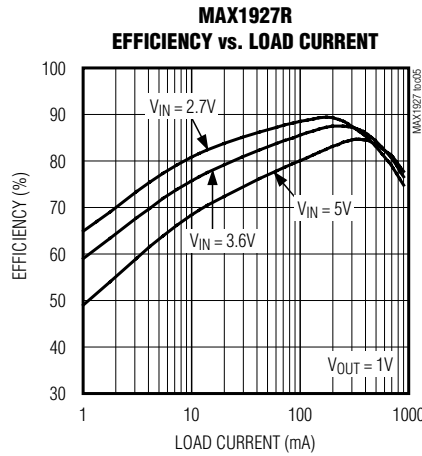
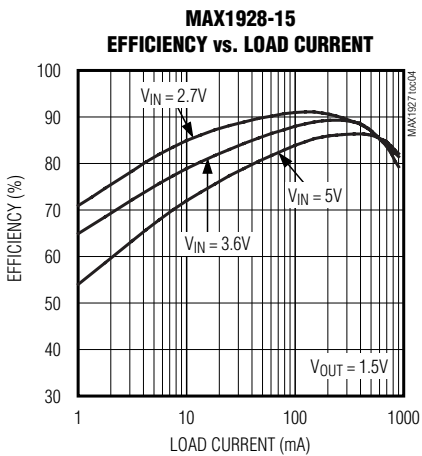
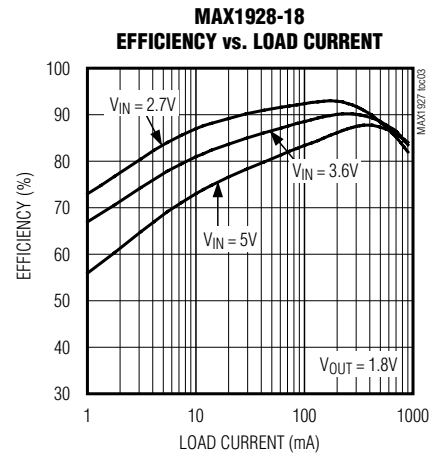
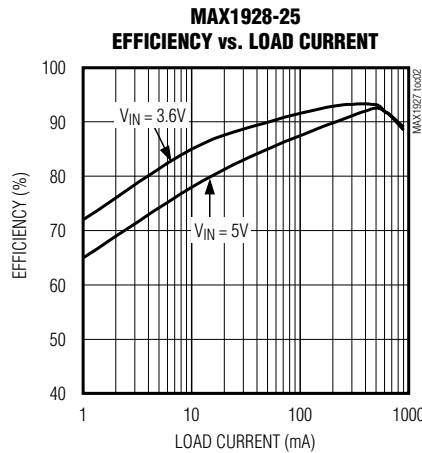
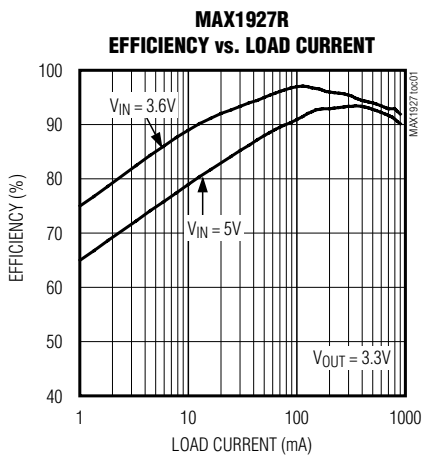
PARAMETER	CONDITIONS	MIN	MAX	UNITS
FB Input Current	MAX1927R		150	nA
Reference Voltage Accuracy		1.22	1.269	V
Reference-Supply Rejection	$2.6V < V_{BATT} < 5.5V$		2	mV
<b>PWM CONTROLLER</b>				
P-Channel On-Resistance	$V_{BATT} = 3.6V$		0.4	$\Omega$
	$V_{BATT} = 2.6V$		0.5	
N-Channel On-Resistance	$V_{BATT} = 3.6V$		0.30	$\Omega$
	$V_{BATT} = 2.6V$		0.35	
P-Channel Current-Limit Threshold		1.1	0.10 1.6	A
P-Channel Pulse-Skipping Current Threshold		0.10	0.16	A
LX Leakage Current	$V_{BATT} = 5.5V$ , LX = GND or BATT	-20	+20	$\mu A$
Maximum Duty Cycle		100		%
Minimum Duty Cycle	PWM = GND		0	%
Internal Oscillator Frequency		0.8	1.2	MHz
<b>POK COMPARATOR</b>				
BATT Operating Voltage Range	$I_{POK} = 0.1 mA$	1	5.5	V
Output Low Voltage	$V_{FB} = 0.5V$ , $I_{POK} = 1mA$		0.1	V
Output High Leakage Current	$V_{POK} = 5.5V$		1	$\mu A$
POK Threshold	MAX1927R	0.650	0.700	V
	MAX1928-15	1.305	1.395	
	MAX1928-18	1.566	1.674	
	MAX1928-25	2.175	2.325	
Output Valid to POK Release Delay	POK transitions to high impedance 20ms after $V_{FB} > V_{POK}$	15	25	ms
<b>LOGIC INPUTS (<math>\overline{SHDN}</math>, PWM)</b>				
Logic Input High	$2.6V < V_{BATT} < 5.5V$	1.6		V
Logic Input Low	$2.6V < V_{BATT} < 5.5V$		0.6	V
Logic Input Current	$V_{BATT} = 5.5V$		1	$\mu A$

# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

## Typical Operating Characteristics

(Circuits of Figure 3 and 4,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

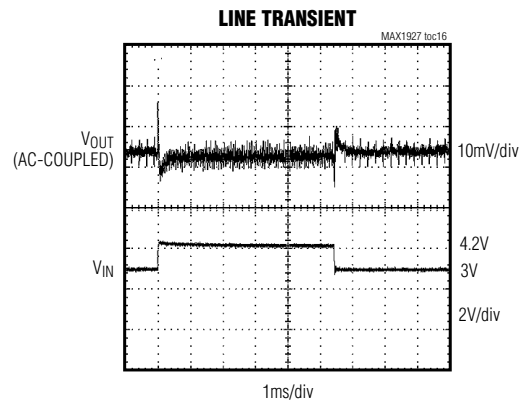
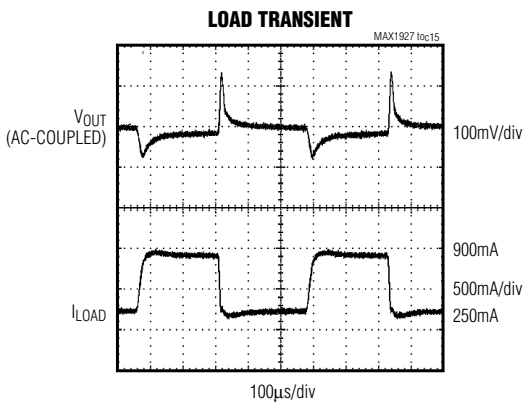
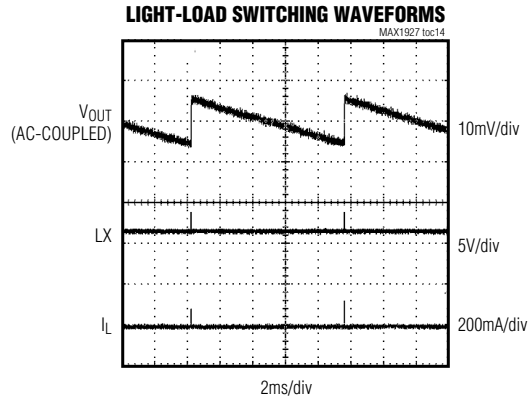
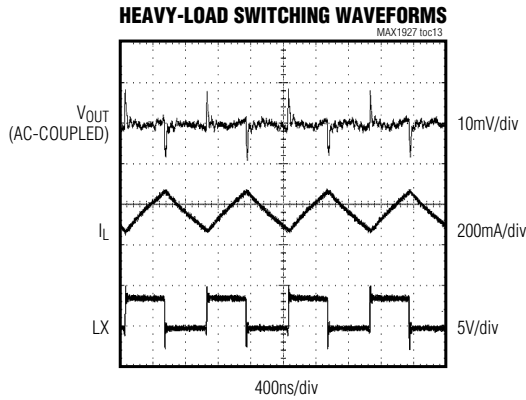
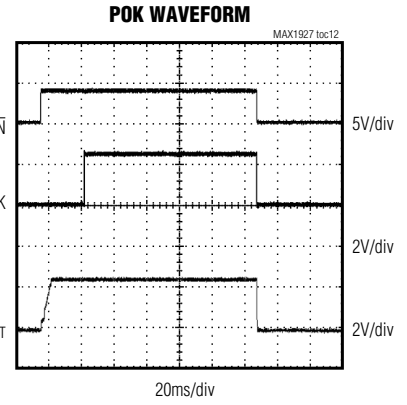
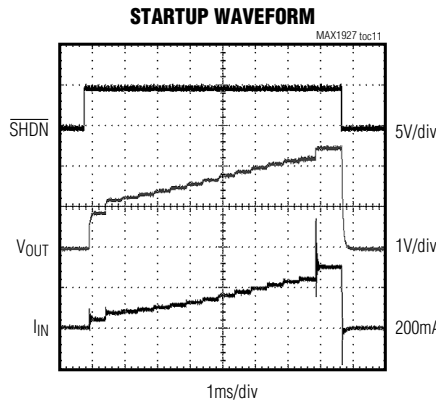
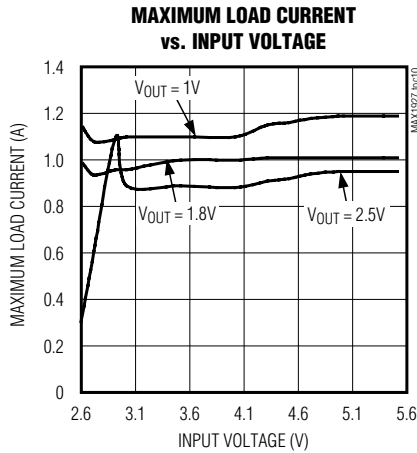
MAX1927/MAX1928



# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

## Typical Operating Characteristics (continued)

(Circuits of Figure 3 and 4,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

## Pin Description

MAX1927/MAX1928

PIN	NAME	FUNCTION
1	PWM	Forced-PWM Input. Drive to GND to use PWM at medium to heavy loads and pulse-skipping at light loads. Drive to BATT to force PWM operation at all loads.
2	GND	Ground
3	REF	Internal 1.25V Reference. Bypass to GND with a 0.1 $\mu$ F capacitor.
4	FB	Output Feedback Sense Input. To set the output voltage to the preset voltage (MAX1928), connect FB directly to the output. To adjust the output voltage (MAX1927R), connect FB to the center of an external resistor-divider between the output and GND. FB regulation voltage is 0.75V.
5	COMP	Compensation Input. See the <i>Compensation, Stability, and Output Capacitor</i> section for compensation component selection.
6	$\overline{\text{SHDN}}$	Shutdown Control Input. Drive low to shut down the converter. Drive high for normal operation.
7	PGND	Power Ground
8	LX	Inductor Connection to the drains of the internal power MOSFETs.
9	BATT	Supply Voltage Input. Connect to a 2.6V to 5.5V source. Bypass to GND with a low-ESR 10 $\mu$ F capacitor.
10	POK	Power-OK Open-Drain Output. Once the soft-start routine has completed, POK goes high impedance 20ms after FB exceeds 90% of its expected final value.

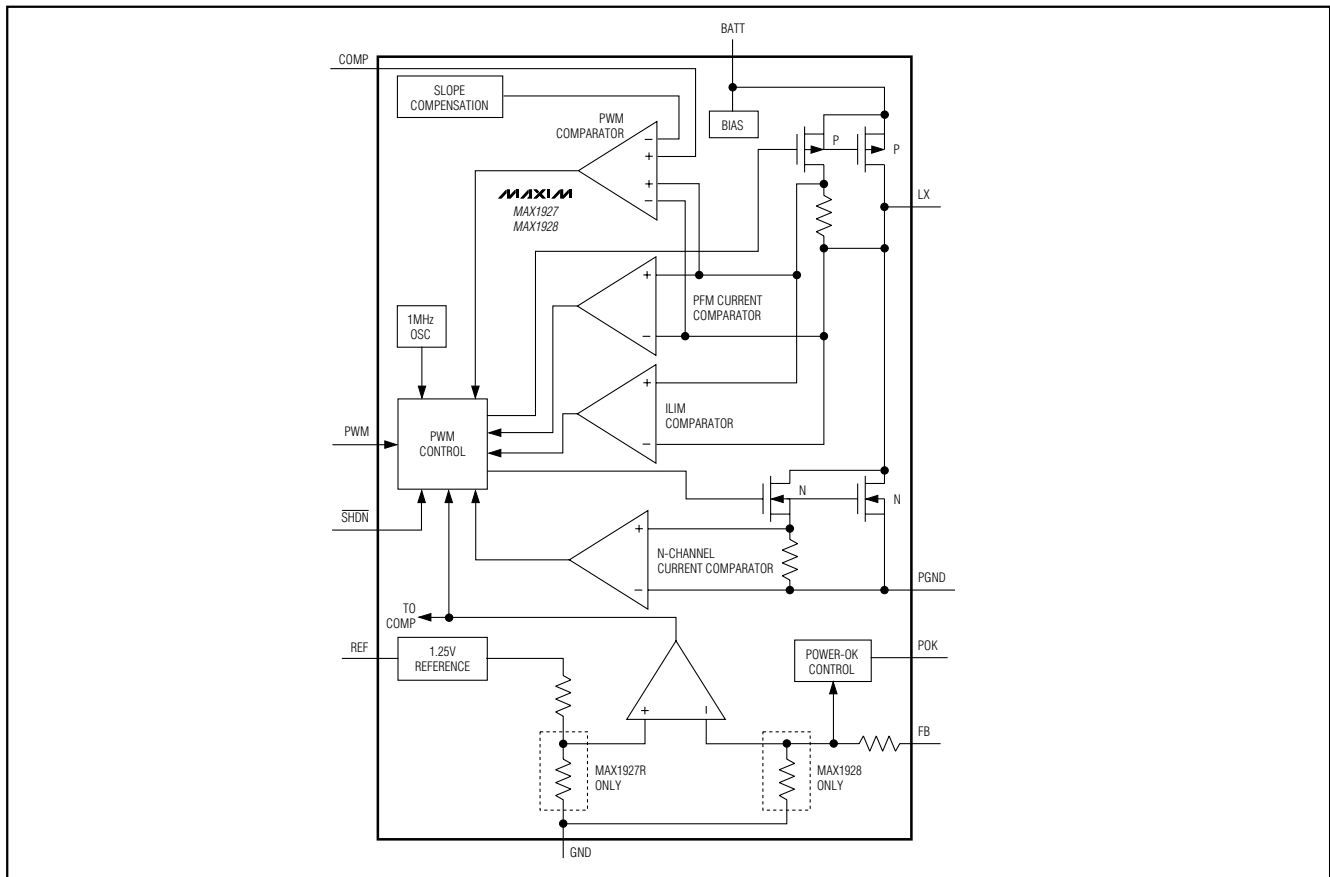


Figure 1. Simplified Functional Diagram

# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

## Detailed Description

The MAX1927/MAX1928 PWM step-down DC-DC converters accept inputs as low as 2.6V, while delivering 800mA to output voltages as low as 0.75V. These devices operate in one of two modes to optimize noise and quiescent current. Under heavy loads, MAX1927/MAX1928 operate in pulse-width modulation (PWM) mode and switch at a fixed 1MHz frequency. Under light loads, they operate in PFM mode to reduce power consumption. In addition, both devices provide selectable forced PWM operation for minimum noise at all load currents.

### PFM Operation and PWM Control Scheme

The PFM mode improves efficiency and reduces quiescent current to 140 $\mu$ A at light loads. The MAX1927/MAX1928 initiate pulse-skipping PFM operation when the peak inductor current drops below 130mA. During PFM operation, the MAX1927/MAX1928 switch only as necessary to service the load, reducing the switching frequency and associated losses in the internal switch, synchronous rectifier, and inductor.

During PFM mode, a switching cycle initiates when the error amplifier senses that the output voltage has dropped below the regulation point. If the output voltage is low, the P-channel MOSFET switch turns on and conducts current to the output filter capacitor and load. The PMOS switch turns off when the PWM comparator is satisfied. The MAX1927/MAX1928 then wait until the error amplifier senses a low output voltage to start again. Some jitter is normal during the transition from PFM to PWM with loads around 100mA. This has no adverse impact on regulation.

At loads greater than 130mA, the MAX1927/MAX1928 use a fixed-frequency, current-mode, PWM controller capable of achieving 100% duty cycle. Current-mode feedback provides cycle-by-cycle current limiting, superior load and line response, as well as overcurrent protection for the internal MOSFET and synchronous rectifier. A comparator at the P-channel MOSFET switch detects overcurrent conditions exceeding 1.1A.

During PWM operation, the MAX1927/MAX1928 regulate output voltage by switching at a constant frequency and then modulating the power transferred to the load using the PWM comparator (Figure 1). The error-amp output, the main switch current-sense signal, and the slope compensation ramp are all summed at the PWM comparator. The comparator modulates the output power by adjusting the peak inductor current during the first half of each cycle based on the output-error voltage. The MAX1927/MAX1928 have relatively low AC-loop gain coupled with a high-gain integrator to enable

the use of a small, low-valued, output filter capacitor. The resulting load regulation is 0.3% (typ) from 0 to 800mA.

### Forced PWM Operation

To force PWM-only operation, connect PWM to BATT. Forced PWM operation is desirable in sensitive RF and data-acquisition applications to ensure that switching noise does not interfere with sensitive IF and data sampling frequencies. A minimum load is not required during forced PWM operation because the synchronous rectifier passes reverse inductor current as needed to allow constant frequency operation with no load. Forced PWM operation has higher quiescent current than PFM (2mA typ compared to 140 $\mu$ A) due to continuous switching.

### 100% Duty-Cycle Operation

The maximum on-time can exceed one internal oscillator cycle, which permits operation at 100% duty cycle. As the input voltage drops, the duty cycle increases until the internal P-channel MOSFET stays on continuously. Dropout voltage at 100% duty cycle is the output current multiplied by the sum of the internal PMOS on-resistance (typically 0.25 $\Omega$ ) and the inductor resistance. Near dropout, switching cycles can be skipped, reducing switching frequency. However, voltage ripple remains small because the current ripple is still low.

### Synchronous Rectification

An N-channel synchronous rectifier eliminates the need for an external Schottky diode and improves efficiency. The synchronous rectifier turns on during the second half of each cycle (off-time). During this time, the voltage across the inductor is reversed, and the inductor current falls. In normal mode, the synchronous rectifier is turned off when either the output falls out of regulation (and another on-time begins) or when the inductor current approaches zero. In forced PWM mode, the synchronous rectifier remains active until the beginning of a new cycle.

### Shutdown Mode

Driving  $\overline{\text{SHDN}}$  to GND places the MAX1927/MAX1928 in shutdown mode. In shutdown, the reference, control circuitry, internal switching MOSFET, and synchronous rectifier turn off and the output becomes high impedance. Drive  $\overline{\text{SHDN}}$  high for normal operation. Input current falls to 0.1 $\mu$ A (typ) during shutdown mode.

### POK Output

POK is an open-drain output that goes high impedance 20ms after the soft-start ramp has concluded and  $V_{FB}$  is within 90% of the threshold. POK is low impedance when in shutdown.

# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

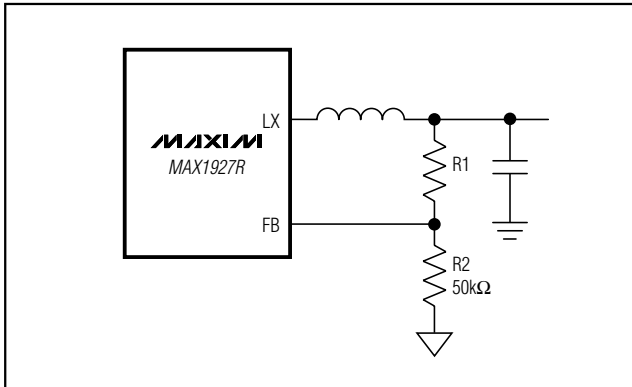


Figure 2. Setting the Adjustable Output Voltage

## Applications Information

### Output Voltage Selection

The MAX1927/MAX1928 have preset output voltages. In addition, the MAX1927R has an adjustable output. To set the output voltage at the preset voltage, connect FB to the output. See Table 1 for a list of the preset voltages and their corresponding part numbers.

The output voltage for the MAX1927R is adjustable from 0.75V to the input voltage by connecting FB to a resistor-divider between the output and GND (Figure 2). To determine the values of the resistor-divider, first select a value for feedback resistor R2 between 5kΩ to 50kΩ. R1 is then given by:

$$R1 = R2 \times \left( \frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where  $V_{FB}$  is 0.75V.

### Input Capacitor Selection

Capacitor equivalent series resistance (ESR) is a major contributor to input ripple in high-frequency DC-DC converters. Ordinary aluminum-electrolytic capacitors have high ESR and should be avoided. Low-ESR aluminum electrolytic capacitors are acceptable and relatively inexpensive. Low-ESR tantalum capacitors or polymer capacitors are better and provide a compact solution for space-constrained surface-mount designs. Ceramic capacitors have the lowest ESR overall.

The input filter capacitor reduces peak currents and noise at the input voltage source. Connect a low-ESR bulk capacitor ( $\geq 10\mu\text{F}$  typ) to the input. Select this bulk capacitor to meet the input ripple requirements and voltage rating rather than capacitance value. Use the

Table 1. FB Regulation Voltages

PART	PRESET OUTPUT VOLTAGE
MAX1927R	0.75V, Adjustable
MAX1928-15	1.5 V
MAX1928-18	1.8 V
MAX1928-25	2.5 V

following equation to calculate the maximum RMS input current:

$$I_{RMS} = \frac{I_{OUT}}{V_{IN}} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}$$

### Compensation, Stability, and Output Capacitor

The MAX1927/MAX1928 are externally compensated with a resistor and a capacitor (see Figure 3,  $R_C$  and  $C_C$ ) in series from COMP to GND. An additional capacitor ( $C_f$ ) may be required from COMP to GND if high-ESR output capacitors are used. The capacitor integrates the current from the transimpedance amplifier, averaging output capacitor ripple. This sets the device speed for transient response and allows the use of small ceramic output capacitors because the phase-shifted capacitor ripple does not disturb the current regulation loop. The resistor sets the proportional gain of the output error voltage by a factor  $g_m \times R_C$ . Increasing this resistor also increases the sensitivity of the control loop to output ripple.

The resistor and capacitor set a compensation zero that defines the system's transient response. The load creates a dynamic pole, shifting in frequency with changes in load. As the load decreases, the pole frequency decreases. System stability requires that the compensation zero must be placed to ensure adequate phase margin (at least  $30^\circ$  at unity gain). The following is a design procedure for the compensation network:

- 1) Select an appropriate converter bandwidth ( $f_C$ ) to stabilize the system while maximizing transient response. This bandwidth should not exceed 1/10 of the switching frequency.
- 2) Calculate the compensation capacitor,  $C_C$ , based on this bandwidth:

For the MAX1927:

$$C_C = \left( \frac{V_{OUT}}{I_{OUT(MAX)}} \right) \times \left( \frac{1}{R_{CS}} \right) \times \left( g_m \times \frac{R_2}{R_1 + R_2} \right) \times \left( \frac{1}{2\pi f_C} \right)$$



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For the MAX1928:

$$C_C = \left( \frac{V_{OUT}}{I_{OUT(MAX)}} \right) \times \left( \frac{1}{R_{CS}} \right) \times (g_m) \times \left( \frac{1}{2\pi f_C} \right)$$

Resistors R1 and R2 are external to the MAX1927 (see the *Setting the Output Voltage* section).  $I_{OUT(MAX)}$  is the maximum output current,  $R_{CS} = 0.48V/A$ , and  $g_m = 250\mu S$  for the MAX1927. See the *Electrical Characteristics* table for MAX1928  $g_m$  values. Select the closest standard  $C_C$  value that gives an acceptable bandwidth.

3) Calculate the equivalent load impedance,  $R_L$ , by:

$$R_L = \frac{V_{OUT}}{I_{OUT(MAX)}}$$

4) Calculate the compensation resistance ( $R_C$ ) to can-

cel out the dominant pole created by the output load and the output capacitance:

$$\frac{1}{2\pi \times R_L \times C_{OUT}} = \frac{1}{2\pi \times R_C \times C_C}$$

Solving for  $R_C$  gives:

$$R_C = \frac{R_L \times C_{OUT}}{C_C}$$

5) Calculate the high-frequency compensation pole to cancel the zero created by the output capacitor's ESR:

$$\frac{1}{2\pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2\pi \times R_C \times C_f}$$

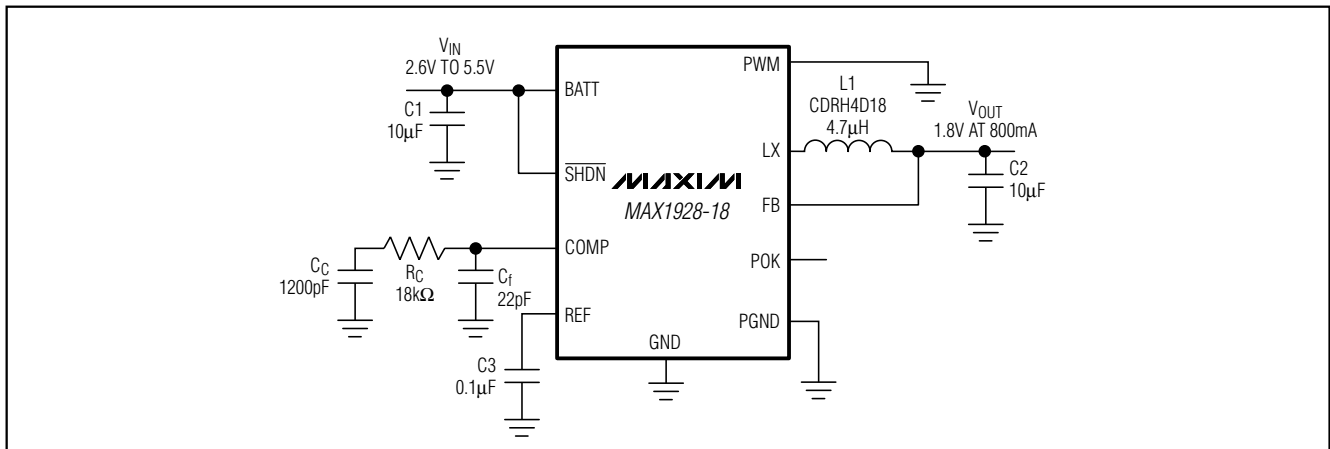


Figure 3. Applications Circuit for the MAX1928

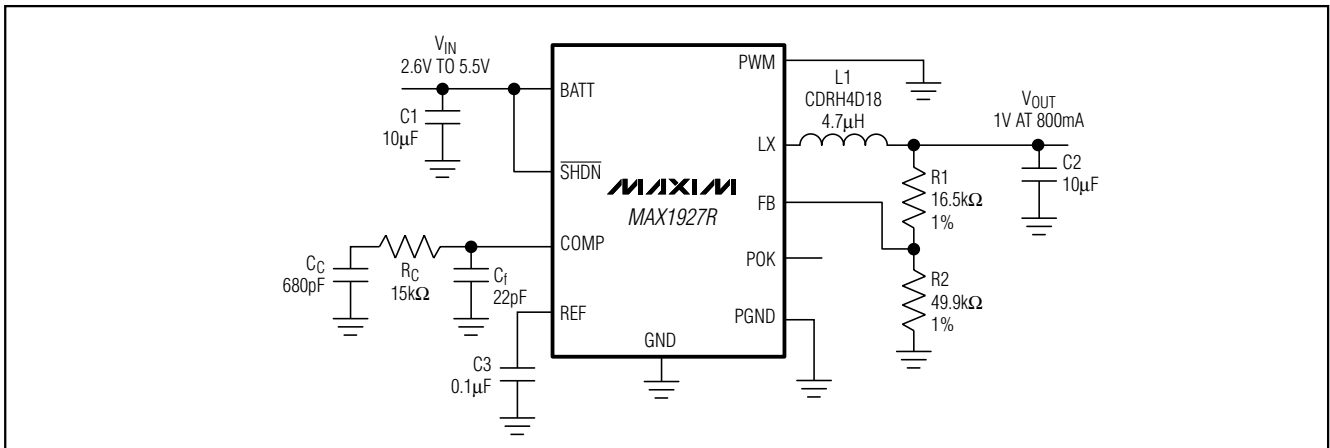


Figure 4. Applications Circuit for the MAX1927

# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

**MAX1927/MAX1928**

Solving for  $C_f$  gives:

$$C_f = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

or 22pF, whichever is greater.

## Standard Application Circuits

Figures 3 and 4 are standard applications circuits for the MAX1927/MAX1928. Figure 3 illustrates the preset output voltages (MAX1928), while Figure 4 shows the adjustable configuration (MAX1927). Table 2 lists part numbers and suppliers for the components used in these circuits.

## PC Board Layout and Routing

High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes EMI, noise on the feedback paths, and voltage gradients in the ground plane, all of which can result in instability or regulation errors. Connect the inductor, input filter capacitor, and output filter capacitor as close together as possible and keep their traces short, direct, and wide. Connect their

ground pins at a single common node in a star ground configuration. The external voltage feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces, such as those from the LX pin, away from the voltage feedback network. Position the bypass capacitors as close as possible to their respective pins to minimize noise coupling. For optimum performance, place input and output capacitors as close to the device as possible. Connect GND and PGND to the highest quality system ground. The MAX1928 evaluation kit illustrates an example PC board layout and routing scheme.

## Chip Information

TRANSISTORS: 3282

PROCESS: BiCMOS

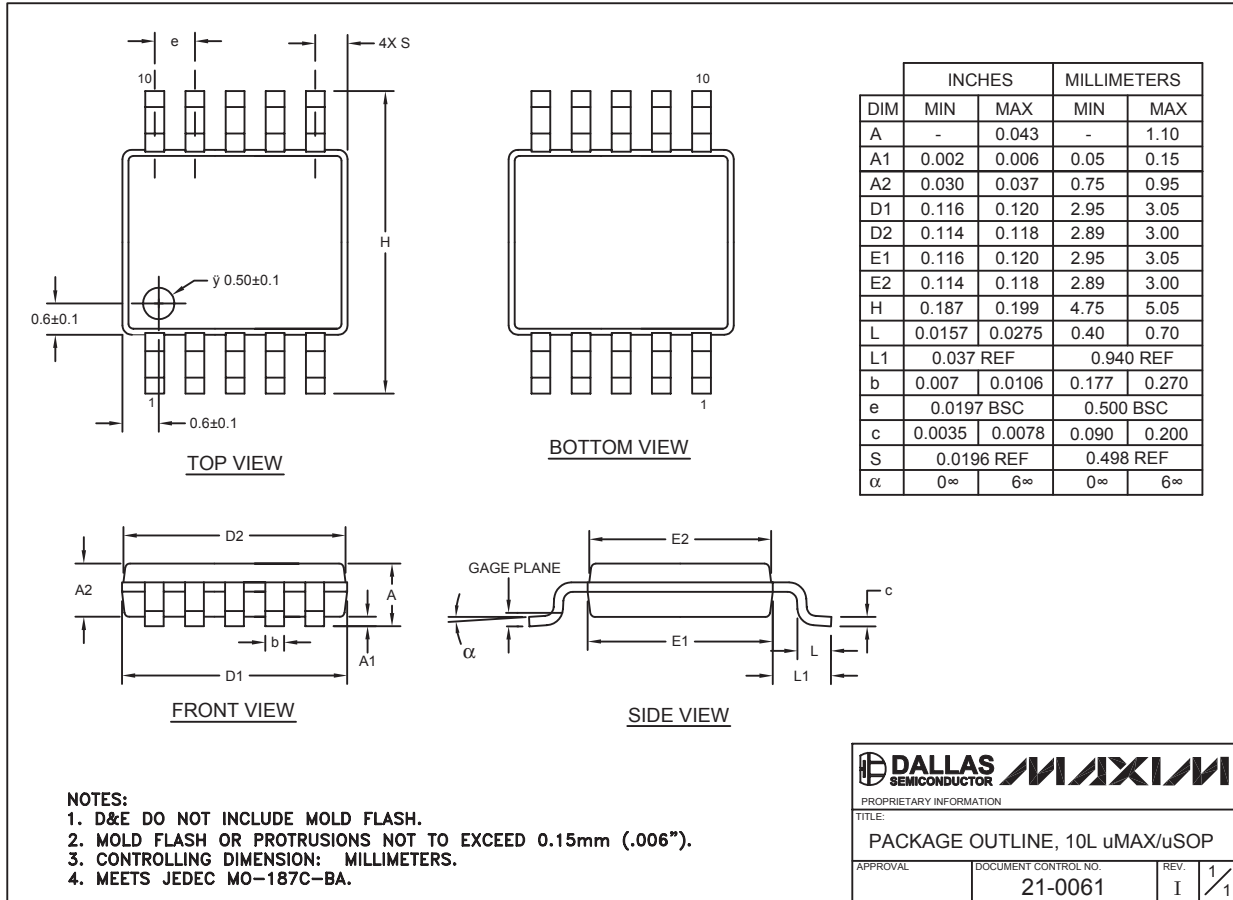
**Table 2. Suggested Parts/Suppliers**

PART	PART NUMBER	MANUFACTURER	PHONE	WEBSITE
Inductor	CDRH3D16-4R7	Sumida	USA 847-956-0666 Japan 81-3-3607-5111	www.sumida.com
Input/Output Capacitors	JMK212BJ106MG	Taiyo Yuden	408-573-4150	www.t-yuden.com
COMP Capacitor	GRM1881X1H561J	Murata	770-436-1300	www.murata.com
REF Capacitor	EMK107BJ104KA	Taiyo Yuden	408-573-4150	www.t-yuden.com

# Low-Output-Voltage, 800mA, PWM Step-Down DC-DC Converters

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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