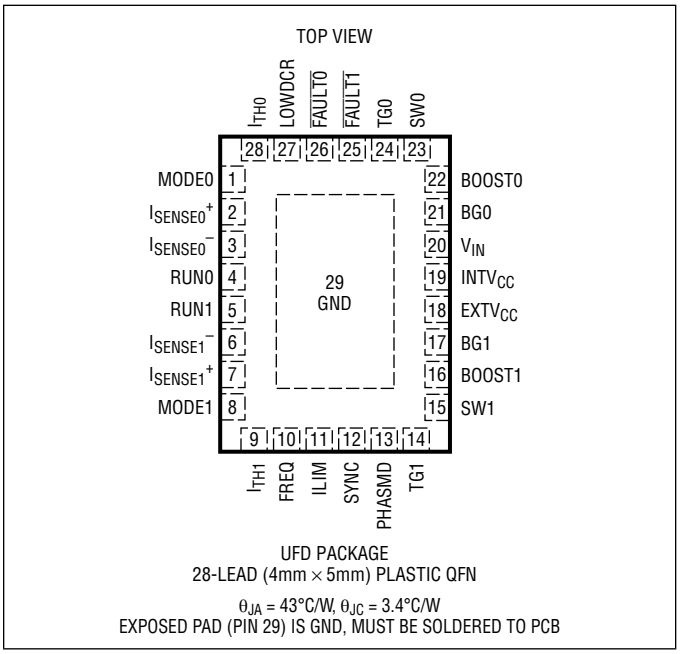
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 40V
BOOST0, BOOST1 ..... –0.3V to 46V
SW0, SW1 ..... –5V to 40V
(BOOST0-SW0), (BOOST1-SW1) ..... –0.3V to 6V
I_{SENSE0}^+, I_{SENSE0}^-, I_{SENSE1}^+, I_{SENSE1}^- ... –0.3V to $INTV_{CC}$
$EXTV_{CC}$, $INTV_{CC}$, RUN0, RUN1 ..... –0.3V to 6V
MODE0, MODE1, ILIM, LOWDCR,
PHASMD, FREQ ..... –0.3V to INTVcc
SYNC, $\overline{FAULT0}$, $\overline{FAULT1}$, I_{TH0}, I_{TH1} ..... –0.3V to INTVcc
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3874EUFD#PBF	LTC3874EUFD#TRPBF	3874	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3874IUFD#PBF	LTC3874IUFD#TRPBF	3874	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage							
V_{IN}	Input Voltage Range			4.5		38	V
V_{OUT}	Output Voltage Range	LOWDCR = $INTV_{CC}$ (Note 3) LOWDCR = 0V				3.5 5.5	V V
I_Q	Input DC Supply Current Normal Operation Shutdown	(Note 4) $V_{RUN0,1}$ = 3.3V $V_{RUN0,1}$ = 0V			4.6 1.8		 mA mA
V_{UVLO}	Undervoltage Lockout Threshold	V_{INTVCC} Falling V_{INTVCC} Rising			3.5 3.8		V V
Control Loop							
$I_{ISENSE0,1}$	I_{SENSE} Pins Bias Current	$V_{ISENSE0,1}$ < (V_{INTVCC} – 3.3V) $V_{ISENSE0,1}$ > (V_{INTVCC} – 3.3V)	● ●		±0.15 ±1	±0.4 ±3	µA µA
$V_{ISENSE(MAX)}$	Maximum Current Sense Threshold	(Table 3) ILIM = $INTV_{CC}$, LOWDCR = $INTV_{CC}$, $V_{ISENSE0,1}$ = 1.2V, V_{ITH} = 2.18V	●	26.8	28.8	30.8	mV
		ILIM = 0V, LOWDCR = $INTV_{CC}$, $V_{ISENSE0,1}$ = 1.2V, V_{ITH} = 2.18V	●	14.5	16	17.5	mV
		ILIM = $INTV_{CC}$, LOWDCR = 0V, $V_{ISENSE0,1}$ = 1.2V, V_{ITH} = 2.18V	●	65	72	79	mV
		ILIM = 0V, LOWDCR = 0V, $V_{ISENSE0,1}$ = 1.2V, V_{ITH} = 2.18V	●	33	40	47	mV
Gate Drivers							
TG R_{UP}	TG Pull-Up $R_{DS(ON)}$	TG High			2.6		Ω
TG R_{DOWN}	TG Pull-Down $R_{DS(ON)}$	TG Low			1.5		Ω
BG R_{UP}	BG Pull-Up $R_{DS(ON)}$	BG High			2.4		Ω
BG R_{DOWN}	BG Pull-Down $R_{DS(ON)}$	BG Low			1.1		Ω
TG0,1 t_r t_f	TG Transition Time: Rise Time Fall Time	(Note 5) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
BG0,1 t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 5) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate on Delay Time	C_{LOAD} = 3300pF Each Driver (Note 5)			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 5)			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 6)			60		ns
$INTV_{CC}$ Regulator							
V_{INTVCC}	Internal V_{CC} Voltage No Load	6V < V_{IN} < 38V		5.25	5.5	5.75	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA			0.5	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive (Note 7)	●	4.5	4.7		V
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				300		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
f_{RANGE}	PLL SYNC Range		●	250		1000	kHz
f_{NOM}	Nominal Frequency	V_{FREQ} = 0.9V			500		kHz
I_{FREQ}	Frequency Setting Current			9	10	11	µA
$\theta_{SYNC-\theta0}$	SYNC to Ch0 Phase Relationship Based on the Falling Edge of SYNC and Rising Edge of TG0	PHASMD = 0 PHASMD = 1/3 • $INTV_{CC}$ PHASMD = 2/3 • $INTV_{CC}$ PHASMD = $INTV_{CC}$			180 60 120 90		Deg Deg Deg Deg
$\theta_{SYNC-\theta1}$	SYNC to Ch1 Phase Relationship Based on the Falling Edge of SYNC and Rising Edge of TG1	PHASMD = 0 PHASMD = 1/3 • $INTV_{CC}$ PHASMD = 2/3 • $INTV_{CC}$ PHASMD = $INTV_{CC}$			0 300 240 270		Deg Deg Deg Deg
Digital Inputs RUN0, RUN1, MODE0, MODE1, $\overline{FAULT0}$, $\overline{FAULT1}$, LOWDCR							
V_{IH}	Input High Threshold Voltage		●			2.0	V
V_{IL}	Input Low Threshold Voltage		●	1.4			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3874 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3874E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3874I is guaranteed over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 43^{\circ}C/W)$

Note 3: Output voltage is set and controlled by master controller in multiphase operations.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Application Information.

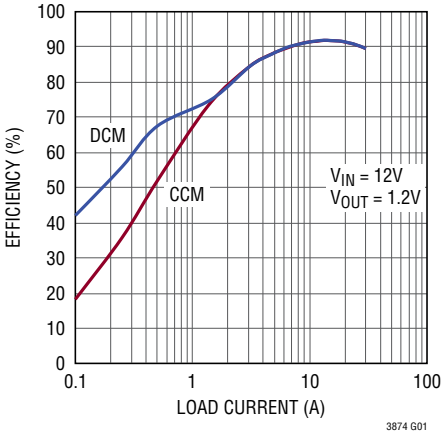
Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 6: The minimum on-time condition corresponds to an inductor peak-to-peak ripple current ≥ 40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

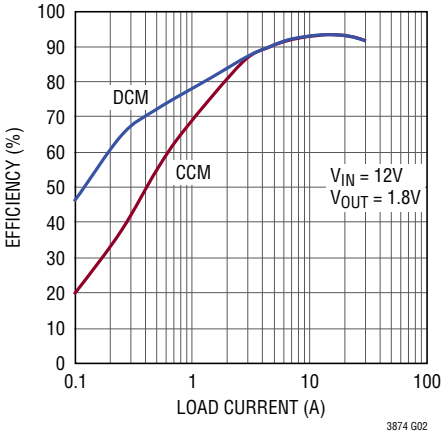
Note 7: $EXTV_{CC}$ is enabled only if V_{IN} is higher than 7V.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

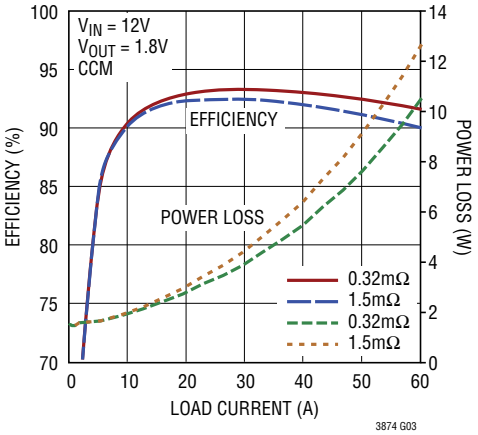
Efficiency vs Output Current and Mode



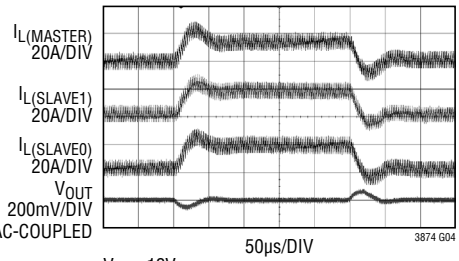
Efficiency vs Output Current and Mode



Dual Phase Efficiency and Power Loss vs Output Current

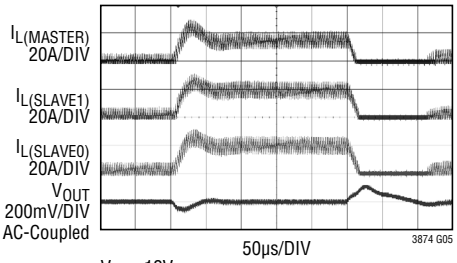


Load Step (Forced Continuous Mode) 3-Phase with Master Controller LTC3866



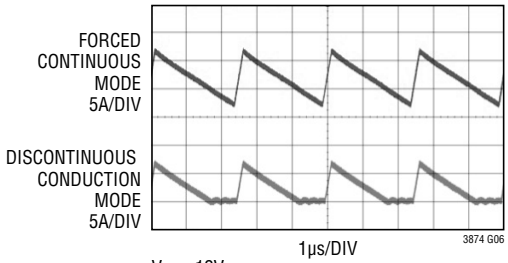
VIN = 12V
VOUT = 1.2V
ILOAD 5A TO 50A

Load Step (Discontinuous Conduction Mode) 3-Phase with Master Controller LTC3866



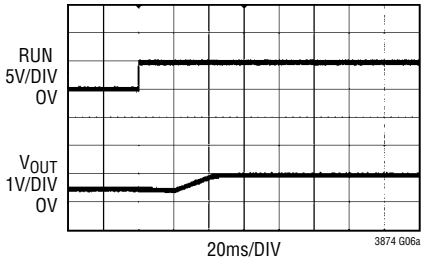
VIN = 12V
VOUT = 1.2V
ILOAD 5A TO 50A

Inductor Current at Light Load



VIN = 12V
VOUT = 1.2V
ILOAD = 2A

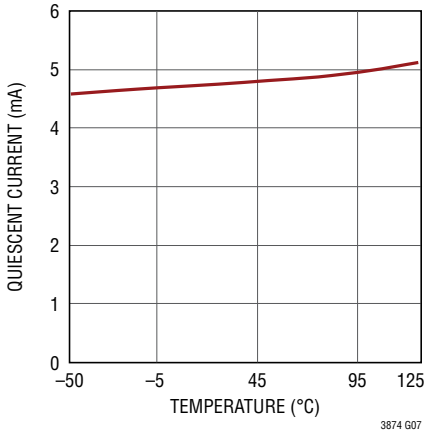
Start-Up Into a Pre-Biased Output with Master Controller LTC3875



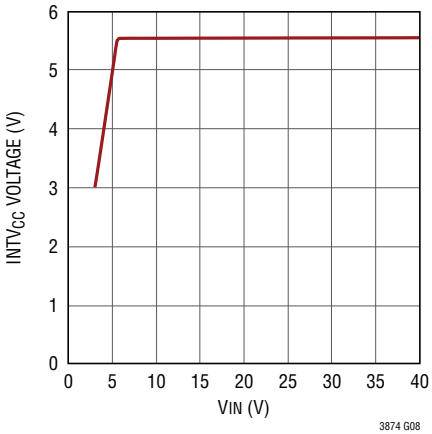
VIN = 12V
VOUT = 1.0V

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

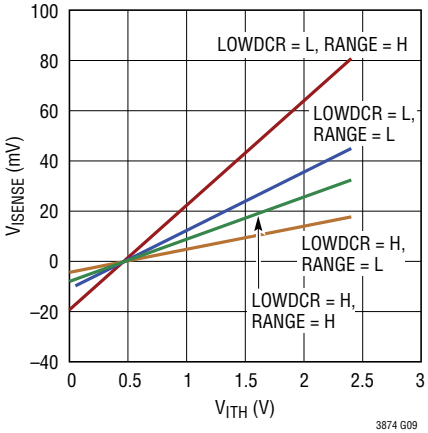
Quiescent Current vs Temperature without $EXTV_{CC}$



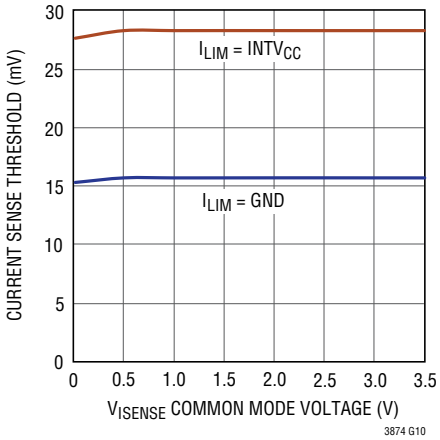
$INTV_{CC}$ Line Regulation



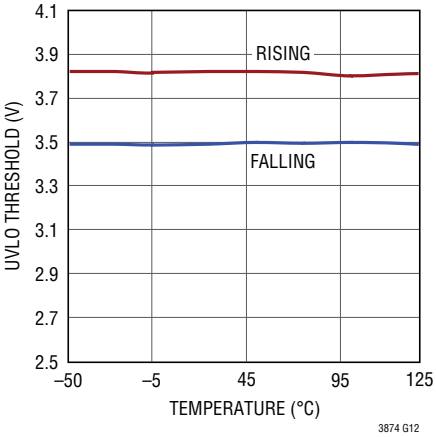
Current Sense Threshold vs I_{TH} Voltage



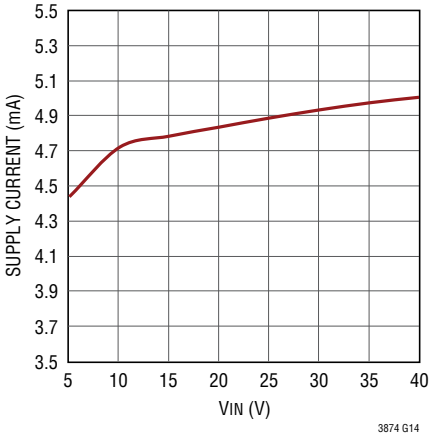
Maximum Current Sense Threshold vs Common Mode Voltage (LOWDCR = $INTV_{CC}$, V_{ITH} = 2.18V)



Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



Quiescent Current vs Input Voltage without $EXTV_{CC}$



PIN FUNCTIONS

MODE0/MODE1 (PIN 1/Pin 8): DCM/CCM Mode Control pins. Each channel runs in forced continuous mode if the Mode pin is logic high. There is an internal 500k pull-down resistor on Mode pin. To select discontinuous conduction mode, float or pull down the MODE pin.

$I_{SENSE0}^+/I_{SENSE1}^+$ (Pin 2/Pin 7): Current Sense Comparator Inputs. The (+) inputs to the current comparators are normally connected to DCR sensing networks.

$I_{SENSE0}^-/I_{SENSE1}^-$ (Pin 3/Pin 6): Current Sense Comparator Inputs. The (–) inputs to the current comparators are connected to the outputs.

RUN0/RUN1 (Pin 4/Pin 5): Enable Run Inputs. Logic high on RUN pin enables the corresponding channel.

I_{TH0}/I_{TH1} (Pin 28/Pin 9): Current Control Threshold. Each associated channel's current comparator tripping threshold increases with its I_{TH} voltage. These pins must be connected to the master controller's I_{TH} pins.

FREQ (Pin 10): Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. This pin sets the default switching frequency when there is no external clock on the SYNC pin. See the application section for detailed information.

ILIM (Pin 11): Current Comparators Sense Voltage Limit. Program a DC voltage at this pin to set the maximum current sense threshold for the current comparators.

SYNC (Pin 12): External Clock Synchronization Input. If an external clock is present at this pin, the switching frequency will be synchronized to the **falling edge** of external clock. Tie this pin to GND if not used.

PHASMD (Pin 13): Phase Set Pin. This pin determines the relative phases between the external clock on pin SYNC and the internal controllers. See Table 1 in the Operation section for details.

TG0/TG1 (Pin 24/Pin 14): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltages.

SW0/SW1 (Pin 23/Pin 15): Switch Node Connections. Connect these pins to the output filter inductor, bottom N-channel MOSFET drain and top N-channel MOSFET source. Voltage swing at the pins are from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST0/BOOST1 (Pin 22/Pin 16): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

BG0/BG1 (Pin 21/Pin 17): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-channel MOSFETs between GND and $INTV_{CC}$.

$EXTV_{CC}$ (Pin 18): External Power Input to an Internal Switch Connected to $INTV_{CC}$. The switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever $EXTV_{CC}$ is higher than 4.7V and V_{IN} is greater than 7V. Do not exceed 6V on this pin.

$INTV_{CC}$ (Pin 19): Internal 5.5V Regulator Output. The control circuits are powered from this voltage. Decouple this pin to GND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

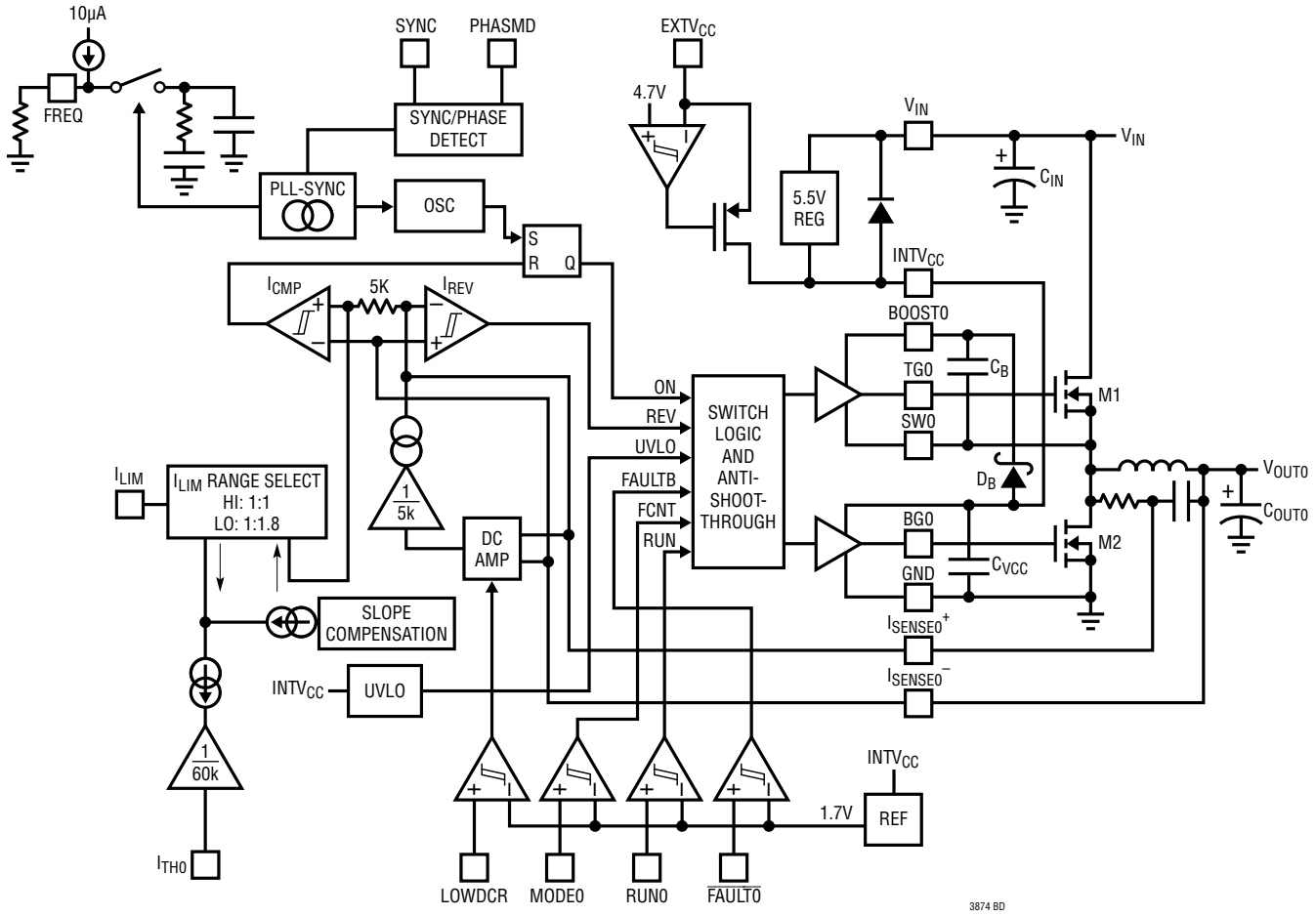
V_{IN} (Pin 20): Main Input Supply. Decouple this pin to GND with a capacitor (0.1µF to 1µF).

$\overline{FAULT0}$, $\overline{FAULT1}$ (Pin 26/Pin 25): Master Controller Fault Inputs. Connect these pins to the master chip fault indicator pins to respond to the fault signals from the master controller. When a $\overline{FAULT}$ pin is floating or low, both TG and BG pins are pulled down in the corresponding channel. There is an internal 500k pull-down resistor on each $\overline{FAULT}$ pin.

LOWDCR (Pin 27): Sub-milliohm DCR Current Sensing Enable Pin. There is an internal 500k pull-up resistor between LOWDCR pin and $INTV_{CC}$. Floating or pulling this pin logic high will enable the sub-milliohm DCR current sensing. Puling this pin logic low will disable the sub-milliohm DCR current sensing.

GND (Exposed Pad Pin 29): Ground. Connect this pad, through vias, to a solid ground plane under the circuit. The sources of the bottom N-channel MOSFETs, the (–) terminal of C_{INTVCC}, and the (–) terminal of C_{IN} should connect to this ground plane as closely as possible to the IC. All small-signal components and compensation components should also connect to this ground plane.

FUNCTIONAL BLOCK DIAGRAM One of Two Channels (CH0) Shown



OPERATION

Main Control Loop

The LTC3874 is a constant frequency, LTC proprietary current mode step-down slave controller for parallel operation with master controllers. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the master controller. When the load current increases, the master controller increases the I_{TH} voltage, which in turn causes the peak current in the corresponding slave channels to increase, until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until the beginning of the next cycle in Continuous Conduction Mode (CCM) or until the inductor current starts to reverse, as indicated by the reverse current comparator I_{REV}, in Discontinuous Conduction Mode (DCM). The LTC3874 slave controllers *DO NOT* regulate the output voltage but regulate the current in each channel for current sharing with the master controllers. Output voltage regulation is achieved through the voltage feedback control loop in the master controllers.

Sub-Milliohm DCR Current Sensing

The LTC3874 employs a unique architecture to enhance the signal-to-noise ratio that enables it to operate with a small sense signal of a sub-milliohm value inductor DCR to improve power efficiency and reduce jitter due to switching noise.

Floating or pulling the LOWDCR pin high will enable sub-milliohm DCR current sensing. The LTC3874 can sense a DCR value as low as 0.2mΩ with careful PCB layout. The proprietary signal processing circuit provides a 14dB signal-to-noise ratio improvement. As with conventional current mode architectures, the current limit threshold is still a function of the inductor peak current and the DCR value, and can be accurately set with the ILIM and I_{TH} pins.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, an internal 5.5V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V and V_{IN} is higher than 7V, the 5.5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$. $EXTV_{CC}$ can be applied before V_{IN}. Using the $EXTV_{CC}$ allows the $INTV_{CC}$ power to be drawn from an external source.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. A dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every three cycles to allow C_B to recharge.

Start-Up and Shutdown (RUN0, RUN1)

The two channels of the LTC3874 can be independently shut down using the RUN0 and RUN1 pins. Pulling either of these pins below 1.4V shuts down the main control circuits for that channel. During shutdown, both TG and BG are pulled down to turn off the external power MOSFETs. Pulling either of these pins above 2V enables the controller. The RUN0/1 pins are actively pulled down until the $INTV_{CC}$ voltage passes the undervoltage lockout threshold of 3.8V. For multiphase operation, the RUN0/1 pins must be connected together and driven by the RUN pins on the master controller. Because a large RC filter in the LTC3874 needs to settle during initialization, the RUN pins can only be pulled up 4ms after V_{IN} is ready. Do not exceed the Absolute Maximum Rating of 6V on these pins.

OPERATION

The start-up of each channel's output voltage V_{OUT} is controlled by the master controller. After the RUN pins are released, the master controller drives the output based on the programmed delay time and rise time. The slave controller LTC3874 follows the I_{TH} voltage set by the master to supply the same current to the output during startup.

Light Load Current Operation (Discontinuous Conduction Mode, Continuous Conduction Mode)

The LTC3874 can operate either in discontinuous conduction mode or forced continuous conduction mode. To select forced continuous mode, tie the MODE pin to a DC voltage above 2V (e.g., $INTV_{CC}$). To select discontinuous conduction mode, tie the MODE pin to a DC voltage below 1.4V (e.g., GND).In forced continuous mode, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in discontinuous mode. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry. When the MODE pin is connected to GND, the LTC3874 operates in discontinuous mode at light loads. At very light loads, the current comparator I_{CMP} may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). This mode provides higher light load efficiency than forced continuous mode and the inductor current is not allowed to reverse. There is a 500k pull-down resistor internally connected to the MODE pin. If the MODE0/1 pins are left floating, both channels are in discontinuous conduction mode by default.

Multichip Operations (PHASMD and SYNC Pins)

The PHASMD pin determines the relative phases between the internal channels as well as the external clock signal on SYNC pin as shown in Table 1. The phases tabulated are relative to zero degree phase being defined as the **falling** edge of the clock on SYNC pin.

Table 1

PHASMD	CHANNEL 0 PHASE	CHANNEL 1 PHASE
GND	180°	0°
1/3 $INTV_{CC}$	60°	300°
2/3 $INTV_{CC}$ or Float	120°	240°
$INTV_{CC}$	90°	270°

The SYNC pin is used to synchronize switching frequency between the master and slave controllers. Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

Single Output Multiphase Operation

The LTC3874 is configured for single output multiphase converters with a master controller by making these connections

- Tie all the I_{TH} pins of paralleled channels together for current sharing between masters and slaves;
- Tie all SYNC or PLLIN pins of paralleled channels together or tie the master chip's CLKOUT pin to the slave chip's SYNC pin for switching frequency synchronization among channels.
- Tie all the RUN pins of paralleled channels together for startup and shutdown at the same time.
- Tie the fault indictor pin of the master controller if available to the $\overline{FAULT}$ pin of the slave controller for fault protection.
- The LTC3874 MODE pin can be tied to the master chip PGOOD pin for start-up control. During soft-start, the LTC3874 operates in DCM mode. When the soft-start interval is done, the LTC3874 operates in CCM mode.

Examples of single output multiphase converters are shown in Figure 1.

OPERATION

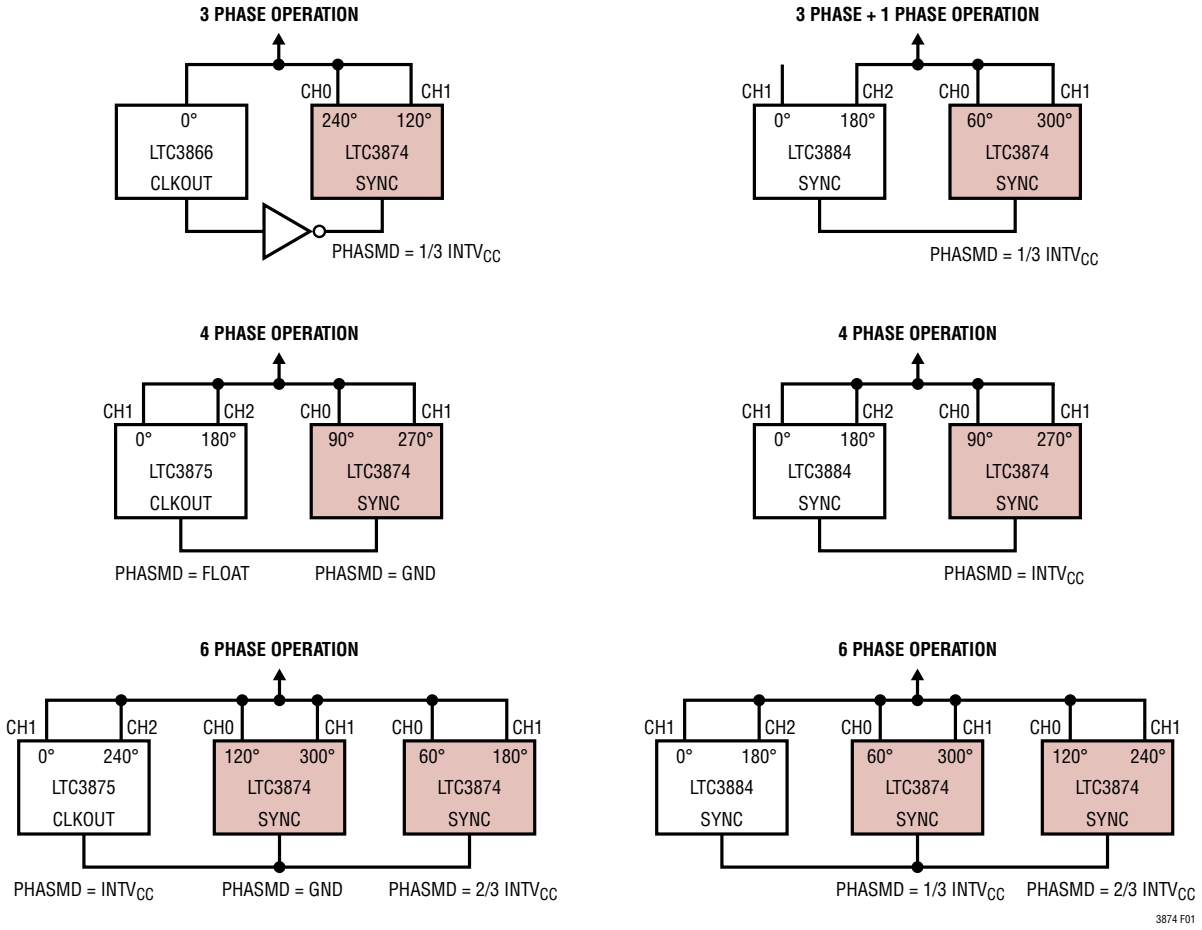


Figure 1. Multiphase Operation

Frequency Selection and Phase-Locked Loop (FREQ and SYNC Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3874 controllers can be selected using the FREQ pin. If the SYNC pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 250kHz to 1MHz. There is a precision 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to GND. A curve is provided later in the application section showing the relationship between the voltage on the FREQ pin and switching frequency (Figure 5). A phase-locked loop (PLL) is integrated in the LTC3874 to synchronize the internal oscillator to an external clock source on the SYNC pin. The PLL loop filter network is integrated inside the LTC3874. The phase-locked loop is capable of locking to any frequency within the range of 250kHz to 1MHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

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The Typical Application on the first page of this data sheet is a basic LTC3874 application circuit configured as a slave controller. In paralleled operation, the current sensing scheme and circuit parameters in the LTC3874 have to be the same as the master controller to achieve balanced current sharing between masters and slaves. Input and output capacitors are selected based on RMS current rating, ripple and transient specs.

Current Limit Programming

To match the master controller current limit, each channel of the LTC3874 can be programmed separately with the ILIM and LOWDCR pins. The 4-level logic input pin ILIM setup summary is shown in Table 2. When ILIM is grounded, both channels are set to be low current range. When ILIM is tied to $INTV_{CC}$, both channels are set to be high current range.

Which setting should be used? For balanced load current sharing, use the same current range setting as in the master controller. Note, the LTC3874 does not have active clamping circuit on I_{TH} pin for peak current limit and over current protection. Over current protection relies on the master controller to drive the I_{TH} pin not to exceed the clamped voltage. The relationship between the current sense threshold and I_{TH} voltage can be found in Table 3.

Table 2. ILIM vs Range

ILIM	CHANNEL 0 CURRENT LIMIT	CHANNEL 1 CURRENT LIMIT
GND	Range Low	Range Low
1/3 $INTV_{CC}$	Range High	Range Low
2/3 $INTV_{CC}$ or Float	Range Low	Range High
INTVcc	Range High	Range High

Table 3. Current Sense Threshold vs I_{TH} Voltage

	CURRENT SENSE THRESHOLD (mV)			
	LOWDCR = H		LOWDCR = L	
I_{TH} (V)	RANGE = H	RANGE = L	RANGE = H	RANGE = L
2.40	32.5	18.1	81.3	45.1
2.33	31.4	17.4	78.4	43.6
2.26	30.2	16.8	75.6	42.0
2.20	29.1	16.2	72.7	40.4
2.18	28.8	16.0	72.0	40.0
2.13	28.0	15.5	69.9	38.8
2.06	26.8	14.9	67.1	37.3
1.99	25.7	14.3	64.2	35.7
1.92	24.6	13.6	61.4	34.1
1.85	23.4	13.0	58.5	32.5
1.79	22.3	12.4	55.7	30.9
1.72	21.1	11.7	52.8	29.4
1.68	20.4	11.3	51.0	28.4
1.58	18.9	10.5	47.2	26.2
1.51	17.7	9.9	44.3	24.6
1.45	16.6	9.2	41.5	23.0
1.38	15.5	8.6	38.6	21.4

I_{SENSE}^+ and I_{SENSE}^- Pins

I_{SENSE}^+ and I_{SENSE}^- are the inputs to the current comparators. When the LOWDCR pin is high, their common mode input voltage range is 0V to 3.5V. I_{SENSE}^- should be connected directly to V_{OUT} of the master controller. I_{SENSE}^+ is connected to an R • C filter with time constant one-fifth of L/DCR of the output inductor. Care must be taken not to float these pins during normal operation. Filter components, especially capacitors, must be placed close to the LTC3874, and the sense lines should run close

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together to a Kelvin connection underneath the current sense element. The LTC3874 is designed to be used with a sub-milliohm DCR value; without proper care, parasitic resistance, capacitance and inductance will degrade the current sense signal integrity, making the programmed current limit unpredictable. In Figure 2, resistor R must be placed close to the output inductor and capacitor C close to the IC pins to prevent noise coupling to the sense signal.

The LTC3874 can also be used like any conventional current mode controller by disabling the LOWDCR pin, connecting it to ground. An RC filter can be used to sense the output inductor signal and connects to the I_{SENSE}^+ pin. Its time constant, R • C, should equal to L/DCR of the output inductor. By pulling down the LOWDCR pin, the current limit increases by 2.5 times. See Table 3 for details. In these applications, the common mode operating voltage range of I_{SENSE}^+, I_{SENSE}^- is from 0V to 5.5V.

Table 4. Output Voltage Range vs LOWDCR Pin

LOWDCR	OUTPUT VOLTAGE
Low	0V to 5.5V
High	0V to 3.5V

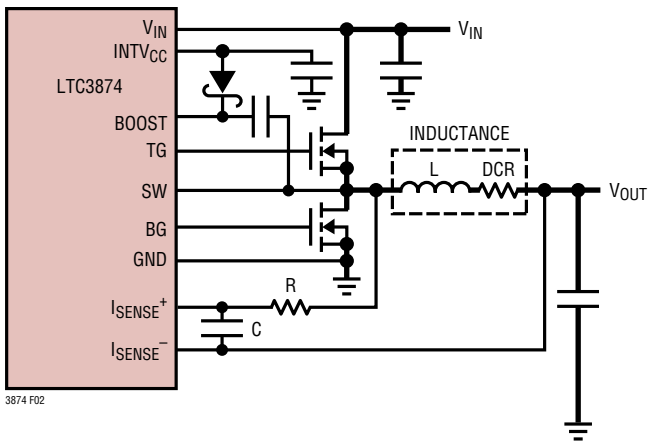

Figure 2 Inductor DCR Current Sensing

Inductor DCR Current Sensing

The LTC3874 is specifically designed for high load current applications requiring the highest possible efficiency; it is capable of sensing the signal of an inductor DCR in the sub-milliohm range (Figure 2). The DCR is the DC winding resistance of the inductor's copper, which is often less than 1mΩ for high current inductors. In high current and low output voltage applications, conduction loss of a high DCR or a sense resistor will cause a significant reduction in power efficiency. For a specific output requirement, choose the inductor with the DCR that satisfies the maximum desirable sense voltage, and use the relationship of the sense pin filters to output inductor characteristics as depicted below.

$$DCR = \frac{V_{ISENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

RC = L/(5 • DCR) when the LOWDCR pin is high

RC = L/DCR when the LOWDCR pin is low

where:

$V_{ISENSE(MAX)}$: Maximum sense voltage for a given I_{TH} voltage

I_{MAX}: Maximum load current

ΔI_L: Inductor ripple current

L, DCR: Output inductor characteristics

R, C: Filter time constant

To ensure that the load current will be delivered over the full operating temperature range, the temperature coefficient of the DCR resistance, approximately 0.4%/°C, should be taken into consideration.

Typically, C is selected in the range of 0.047µF to 0.47µF. This forces R to around 2kΩ, reducing error that might have been caused by the I_{SENSE} pins' ±1uA current.

There will be some power loss in R that relates to the duty cycle. It will be highest in continuous mode at maximum input voltage:

$$P_{LOSS}(R) = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R}$$

Ensure that R has a power rating higher than this value. However, DCR sensing eliminates the conduction loss of a sense resistor; it will provide a better efficiency at heavy loads. To maintain a good signal-to-noise ratio for the current sense signal, using a minimum ΔV_{ISENSE} of

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2mV for duty cycles less than 40% is desirable when the LOWDCR pin is high; use a minimum ΔV_{ISENSE} of 10mV for duty cycles less than 40% when the LOWDCR pin is low. The actual ripple voltage will be determined by the following equation:

$$\Delta V_{ISENSE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{R\,C \bullet f_{OSC}}\right)$$

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

At least two external power MOSFETs need to be selected: One N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than one-third of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the internal regulator voltage, V_{INTVCC}, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less. Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, input capacitance, input voltage and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical *gate charge* curve included on most data sheets (Figure 3). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time.

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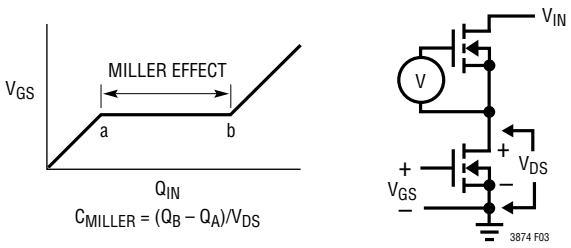

Figure 3. Gate Charge Characteristic

The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturer's data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included. When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

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An optional Schottky diode across the synchronous MOSFET conducts during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse-recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

$INTV_{CC}$ Regulators and $EXTV_{CC}$

The LTC3874 features a PMOS LDO that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and most of the LTC3874's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 5.5V when V_{IN} is greater than 6V. $EXTV_{CC}$ connects to $INTV_{CC}$ through another P-channel MOSFET and can supply the needed power when its voltage is higher than 4.7V and V_{IN} is higher than 7V. Each of these can supply a peak current of 100mA and must be bypassed to ground with a minimum value of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and GND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3874 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5.5V linear regulator from V_{IN} or $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.4V, the linear regulator is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC3874 $INTV_{CC}$ current is limited to less than 34mA from a 38V supply in the UFD package and not using the $EXTV_{CC}$ supply:

$$T_J = 70°C + (34mA)(38V)(43°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 4.7V and V_{IN} above 7V, the $INTV_{CC}$ linear regulator is turned off and the $EXTV_{CC}$ is connected to $INTV_{CC}$. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from other high efficiency sources such as +5V rails in the system. Do not apply more than 6V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from $EXTV_{CC}$. Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (34mA)(5V)(43°C/W) = 77°C$$

However, for low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal LDO resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected to an external supply. If a 5V external supply is available, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.
3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V.

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For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 4 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET, which is typically 4.5V for logic-level devices.

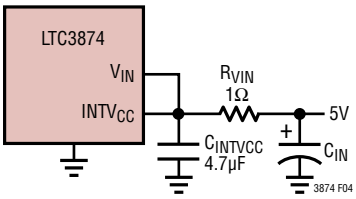

Figure 4. Setup for a 5V Input

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitor, C_B, connected to the BOOST pin, supplies the gate drive voltages for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC} – V_{DB}$$

The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Undervoltage Lockout

The LTC3874 has a precision UVLO comparator constantly monitoring the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action and pulls down RUN pins when $INTV_{CC}$ is below 3.5V. In multiphase operation, when the LTC3874 is in undervoltage lockout, the RUN pin is pulled down to disable the master's switching action. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 300mV of precision hysteresis.

Phase-Locked Loop and Frequency Synchronization

The LTC3874 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the internal clock to be locked to the falling edge of an external clock signal applied to the SYNC pin. The turn-on of the top MOSFET is synchronized or out-of-phase with the **falling** edge of external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 10µA of current flowing out of the FREQ pin. This allows the user to use a single resistor to GND to set the switching frequency when no external clock is applied to the SYNC pin. The internal switch between the FREQ pin and the integrated PLL filter network is ON, allowing the filter network to be precharged to the same voltage potential as the FREQ pin. The relationship between the voltage on the FREQ pin and the operating frequency is shown in Figure 5 and specified in the Electrical Characteristic table. If an external clock is detected on the SYNC pin, the internal switch mentioned above will turn off and isolate the influence of the FREQ pin. Note that the LTC3874 can only be synchronized to an external clock whose frequency is within the range of the LTC3874's internal VCO. This is guaranteed to be between 250kHz and 1MHz. A simplified block diagram is shown in Figure 6.

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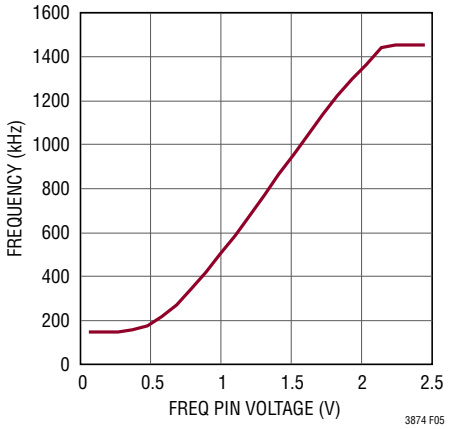

Figure 5. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

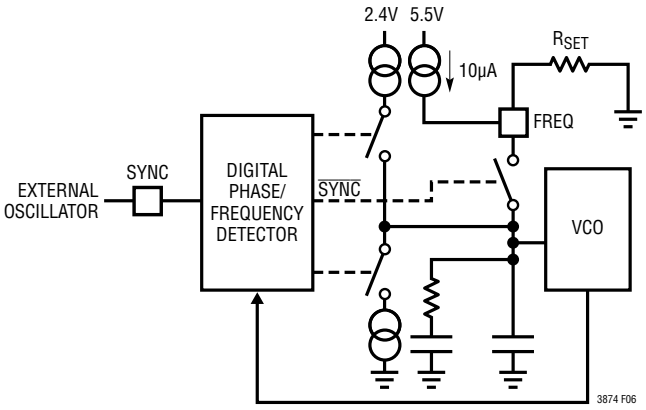

Figure 6. Phase-Locked Loop Block Diagram

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

Typically, the external clock (on the SYNC pin) input high threshold is 2V, while the input low threshold is 1.4V.

Fault Protection and Response

Master controllers monitor system voltage, current, temperature and provide many protection features during all kinds of fault conditions. The LTC3874 slave controllers do not provide as many fault protections as master controllers but respond to the fault signal from the master controller. $\overline{\text{FAULT0}}$ and $\overline{\text{FAULT1}}$ pins are designed to share the fault signal between masters and slaves. In a typical parallel application, connect the fault pins on LTC3874 to the master fault indictor pins, so that the slave controller can respond to all fault signals from the master. When the $\overline{\text{FAULT}}$ pin is pulled below 1.4V, both TG and BG in the corresponding channel are pulled down and external MOSFETs are turned off. When the $\overline{\text{FAULT}}$ pin voltage is above 2V, the corresponding channel is back to normal operation. During fault conditions, all internal circuits in the LTC3874 are still running so the slave controllers can immediately return to normal operation when the $\overline{\text{FAULT}}$ pin is released.

The LTC3874 has internal thermal shutdown protection which pulls all TG and BG pins low when the junction temperature is higher than 160°C. The thermal shutdown has 10°C of hysteresis. In thermal shutdown, the $\overline{\text{FAULT0}}$ and $\overline{\text{FAULT1}}$ pins are also pulled low. The RUN pins are not internally pulled low. There is a 500k pull-down resistor on each $\overline{\text{FAULT}}$ pin which sets the default voltage on the $\overline{\text{FAULT}}$ pins low if the $\overline{\text{FAULT}}$ pins are floating.

Transient Response and Loop Stability

In a typical parallel operation, the LTC3874 cooperates with master controllers to supply more current. To achieve balanced current sharing between master and slave, it is recommended that each slave channel copies the power stage design from the master channel. Select the same inductors, same power MOSFETs, and same output capacitors between the master and slave channels. Control loop and compensation design on the I_{TH} pin should start with the single phase operation of the master controller. The multiphase transient response and loop stability is almost the same as the single phase operation of the master by tying the I_{TH} pins together between master and slaves. For example, design the compensation for a single phase 1.8V/20A output using LTC3866 with a 0.33µH inductor

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and 530µF output capacitors. To extend the output to 1.8V/40A, simply parallel one channel of LTC3874 with the same inductor and output capacitors (total output capacitors are 1060µF) and tie the I_{TH} pin of LTC3874 to the master I_{TH}. The loop stability and transient responses of the two phase converter are very similar to the single phase design without any extra compensator on the I_{TH} pin of the slave controller. Furthermore, LTpowerCAD is provided on the LTC website as a free download for transient and stability analysis.

To minimize the high frequency noise on the I_{TH} trace between master and slave I_{TH} pins, a small filter capacitor in the range of tens of pF can be placed closely at each I_{TH} pin of the slave controller. This small capacitor normally does not significantly affect the closed-loop bandwidth but increases the gain margin at high frequency.

Mode Selection and Pre-Biased Startup

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging the output capacitors. The LTC3874 can be configured to operate in DCM mode for pre-biased start-up. The master chip's PGOOD pin can be connected to the MODE pins of the LTC3874 to ensure the DCM operation at startup and CCM operation in steady state.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3874 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase. The minimum on-time for the LTC3874 is approximately 90ns, with reasonably good PCB layout, minimum 30% inductor current ripple and at least 2mV – 3mV (10mV – 15mV when the LOWDCR pin is low) ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the current loop. As the peak sense voltage decreases the minimum on-time gradually increases to 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 7. Figure 8 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in the PC layout:

1. Are the top N-channel MOSFETs M1 and M3 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The I_{TH} traces should be as short as possible. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

APPLICATIONS INFORMATION

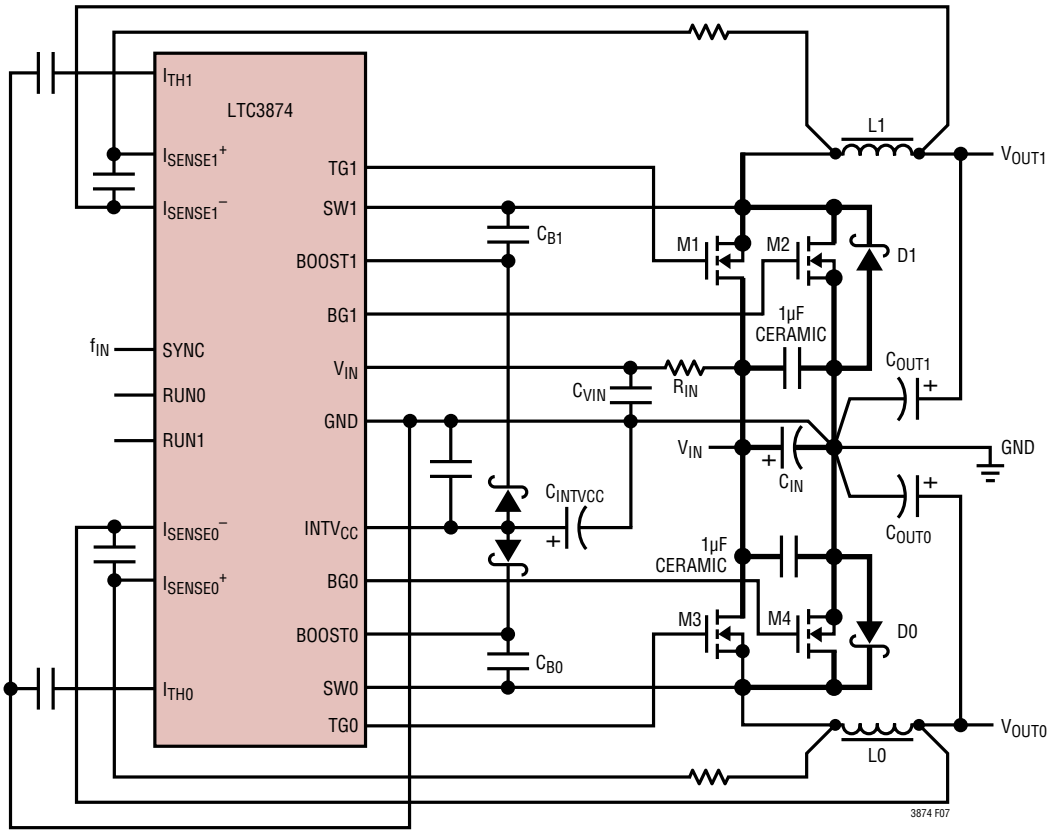


Figure 7. Recommended Printed Circuit Layout Diagram

3. Are the I_{SENSE}^+ and I_{SENSE}^- leads routed together with minimum PC trace spacing? The filter capacitor between I_{SENSE}^+ and I_{SENSE}^- should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor or inductor, whichever is used for current sensing.

4. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially.

5. Keep the switching nodes (SW1, SW0), top gate nodes (TG1, TG0), and boost nodes (BOOST1, BOOST0) away from sensitive small-signal nodes, especially from the opposite channel's current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC3874 and occupy minimum PC trace area. If DCR sensing is used, place the resistor (Figure 2, "R") close to the switching node.

6. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

APPLICATIONS INFORMATION

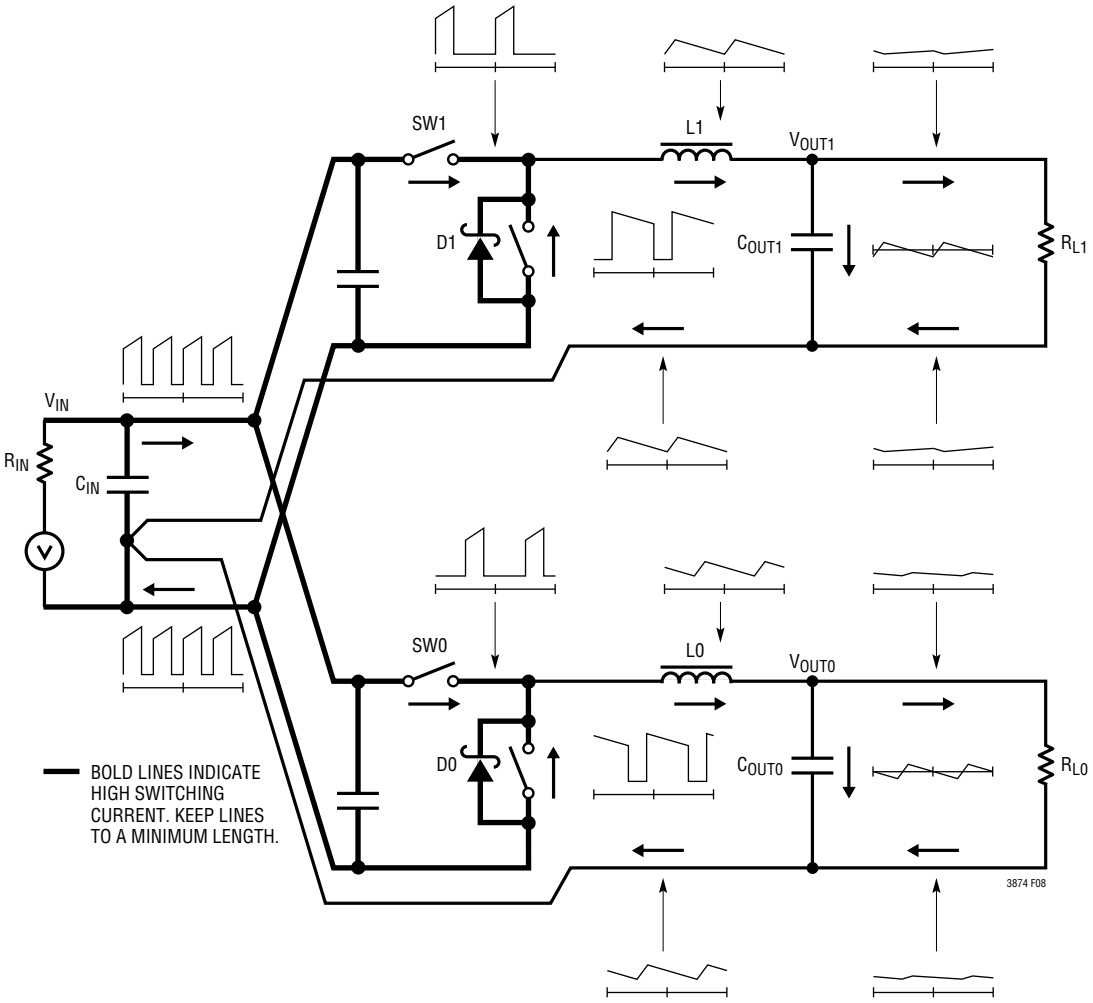


Figure 8. Branch Current Waveforms

APPLICATIONS INFORMATION

PC Board Layout Debugging

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

Design Example

As a design example using master controller LTC3866 and slave controller LTC3874 for a 3-phase high current regulator, assume V_{IN} = 12V (nominal), V_{IN} = 20V (maximum), V_{OUT} = 1.5V, I_{MAX} = 90A, and f = 400kHz (see Figure 9).

The master controller LTC3866 design can be found in the LTC3866 data sheet Design Example section.

The regulated output voltage is determined by the LTC3866:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

Using a 20k 1% resistor from the V_{FB} node to ground, the top feedback resistor is (to the nearest 1% standard value) 30.1k.

The frequency is set by biasing the LTC3866 FREQ pin to 1V. The LTC3866 CLKOUT pin is connected to the LTC3874 SYNC pin through an inverter. The LTC3874 PHASMD pin is connected to 1/3 • $INTV_{CC}$.

The inductance value is based on a 35% maximum ripple current assumption per phase (10.5A). The highest value of ripple current occurs at the maximum input voltage:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

This design will require 0.33µH. The Würth 744301033,0.33µH inductor is chosen for both the LTC3866 and the LTC3874. At the nominal input voltage (12V), the ripple current will be:

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

It will have 10A (33%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 35A.

APPLICATIONS INFORMATION

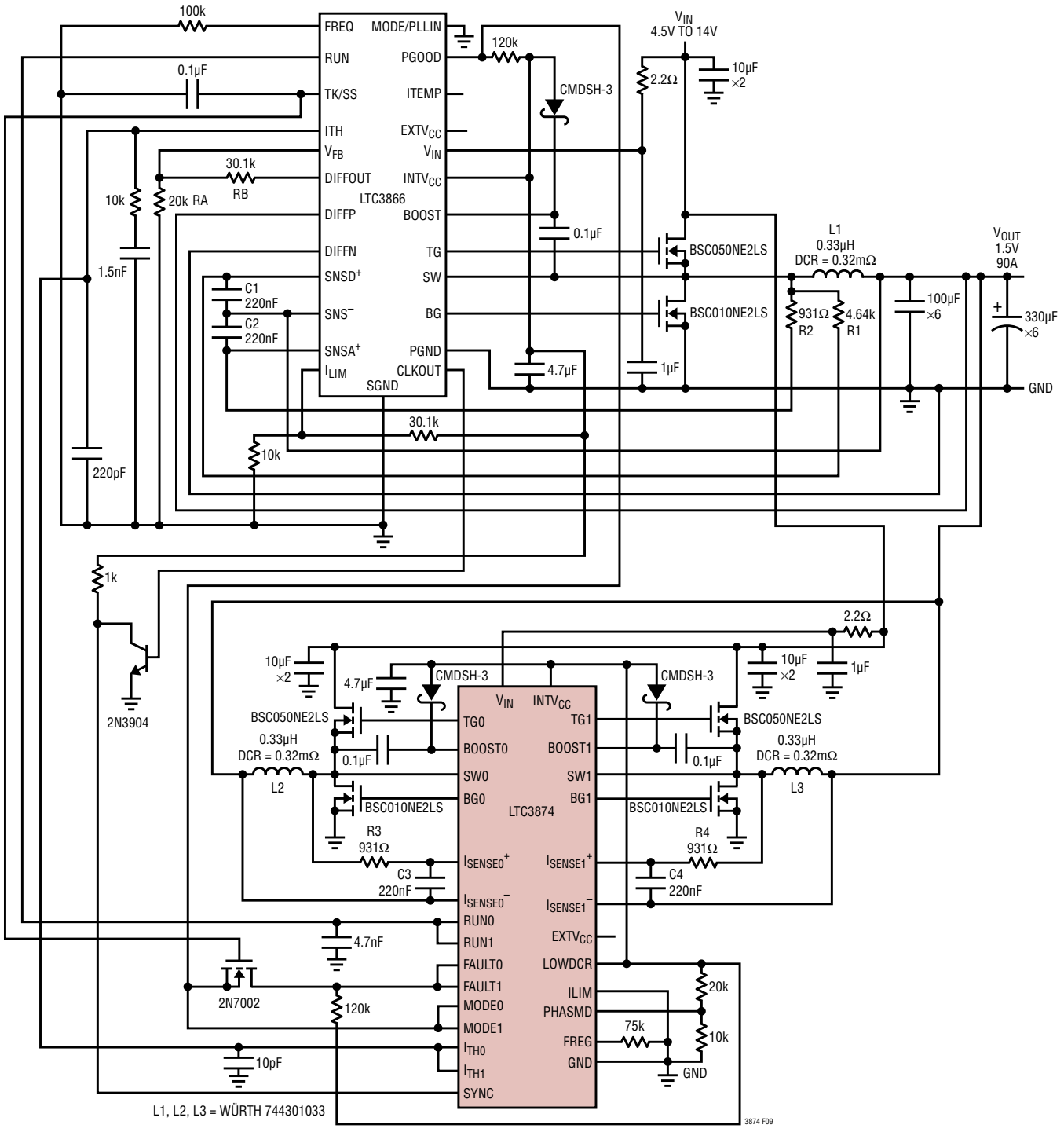


Figure 9. High Efficiency, Triple Phase Sub-Milliohm DCR Sensing 1.5V/90A Step-Down Supply

APPLICATIONS INFORMATION

The minimum on-time occurs at the maximum V_{IN}, and should not be less than 90ns:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f} = \frac{1.5V}{20V(400kHz)} = 187ns$$

DCR current sensing is used in this circuit. For the LTC3866, if C1 and C2 are chosen to be 220nF, based on the chosen 0.33µH inductor with 0.32mΩ DCR, R1 and R2 can be calculated as:

$$R1 = \frac{L}{DCR \bullet C1} = 4.69k$$

$$R2 = \frac{L}{DCR \bullet C2 \bullet 5} = 937\Omega$$

Choose R1 = 4.64k and R2 = 931Ω.

For the LTC3874, if C3 and C4 are chosen to be 220nF, based on the chosen 0.33µH inductor with 0.32mΩ DCR, R3 and R4 can be calculated as:

$$R3 = \frac{L}{DCR \bullet C3 \bullet 5} = 937\Omega$$

$$R4 = \frac{L}{DCR \bullet C4 \bullet 5} = 937\Omega$$

Choose R3 = 931 Ω and R4 = 931Ω.

The maximum DCR of the inductor is 0.34mΩ. The $V_{SENSE(MAX)}$ is calculated as:

$$V_{SENSE(MAX)} = I_{PEAK} \bullet DCR_{MAX} = 12mV$$

The current limit is chosen to be 15mV for the LTC3866. When the current limit is 15mV for the LTC3866, the I_{TH} pin voltage is 2V. Based on Table 3, the LTC3874 LOWDCR pin is pulled high and the ILIM pin is pulled low to choose both channels' current limit to be 14.4mV when the I_{TH} pin voltage is 2V.

Both ICs' RUN pins are connected together. During start-up, the LTC3866 has 1µA current to pull up the RUN pins. A 4.7nF capacitor is connected to the RUN pins to ensure the LTC3874 RUN pins have 4mS delay after V_{IN} is ready.

The LTC3866 PGOOD pin is connected to the LTC3874 $\overline{FAULT}$ pins through a NMOS switch. The switch is controlled by the LTC3866 TK/SS pin. During the soft-start, the switch is off. The LTC3874 $\overline{FAULT}$ pins are pulled up by a 120k resistor. When the soft-start interval is done, the NMOS switch is turned on. The LTC3874 $\overline{FAULT}$ pins are controlled by the LTC3866 PGOOD pin.

The LTC3874 Mode pins are tied to the LTC3866 PGOOD pin for start-up control.

The LTC3866 and LTC3874 choose the same power MOSFET, C_{IN}, and C_{OUT}.

The power dissipation on the topside MOSFET can be easily estimated. Choosing an Infineon BSC050NE2LS MOSFET results in: $R_{DS(ON)}$ = 7.1mΩ (max), V_{MILLER} = 2.8V, $C_{MILLER} \cong$ 35pF. At maximum input voltage with TJ (estimated) = 75°C:

$$P_{MAIN} = \frac{1.5V}{20V}(30A)^2[1+(0.005)(75°C-25°C)] \bullet (0.0071\Omega) + (20V)^2\left(\frac{30A}{2}\right)(2\Omega)(35pF) \bullet \left[\frac{1}{5.5V-2.8V} + \frac{1}{2.8V}\right](400kHz)$$

$$= 599mW + 122mW$$

$$= 721mW$$

An Infineon BSC010NE2LS, $R_{DS(ON)}$ = 1.1mΩ, is chosen for the bottom FET. The resulting power loss is:

$$P_{SYNC} = \frac{20V-1.5V}{20V}(30A)^2[1+(0.005)(75°C-25°C)] \bullet (0.001\ 1\Omega) = 1.14W$$

APPLICATIONS INFORMATION

Design Example 2

Using master controller LTC3884 and slave controller LTC3874 for a dual-output, 3 + 1 phase high current regulator, assume V_{IN} = 12V (nominal), and V_{IN} = 15V (maximum). LTC3884 channel 0 provides V_{OUT0} of 1.5V and 30A output current, and channel 1 together with channel 0 and channel 1 in the LTC3874 provides V_{OUT1} of 1.0V, with 90A output current (see Figure 11).

The master chip LTC3884 design can be found in the LTC3884 data sheet (Design Example section).

The LTC3884 SYNC pin is connected to the LTC3874 SYNC pin for switching frequency synchronization. The LTC3874 PHASMD pin is forced to 1/3 $INTV_{CC}$ to form a PolyPhase configuration.

The slave chip LTC3874 should use the same inductor, power MOSFET, C_{IN}, and C_{OUT} as the master chip. DCR sensing is also used for the slave chip.

The LTC3884 I_{TH1}, the LTC3874 I_{TH0} and the LTC3874 I_{TH1} pins are connected together. The LTC3874 LOWDCR pin is pulled high and the ILIM pin is forced to 0V to obtain the same current limit as LTC3884 CH1.

The LTC3884 RUN1, the LTC3874 RUN0 and the LTC3874 RUN1 pins are connected together. The LTC3884 $\overline{FAULT}$ pins are connected to LTC3874's $\overline{FAULT}$ pins so the LTC3874 will be disabled if the LTC3884 is under any fault event.

The LTC3874 MODE pins are tied to the LTC3884 PGOOD1 pin for start-up control. During soft-start, the LTC3874 operates in DCM mode. When the soft-start interval is done, the LTC3874 operates in CCM mode.

APPLICATIONS INFORMATION

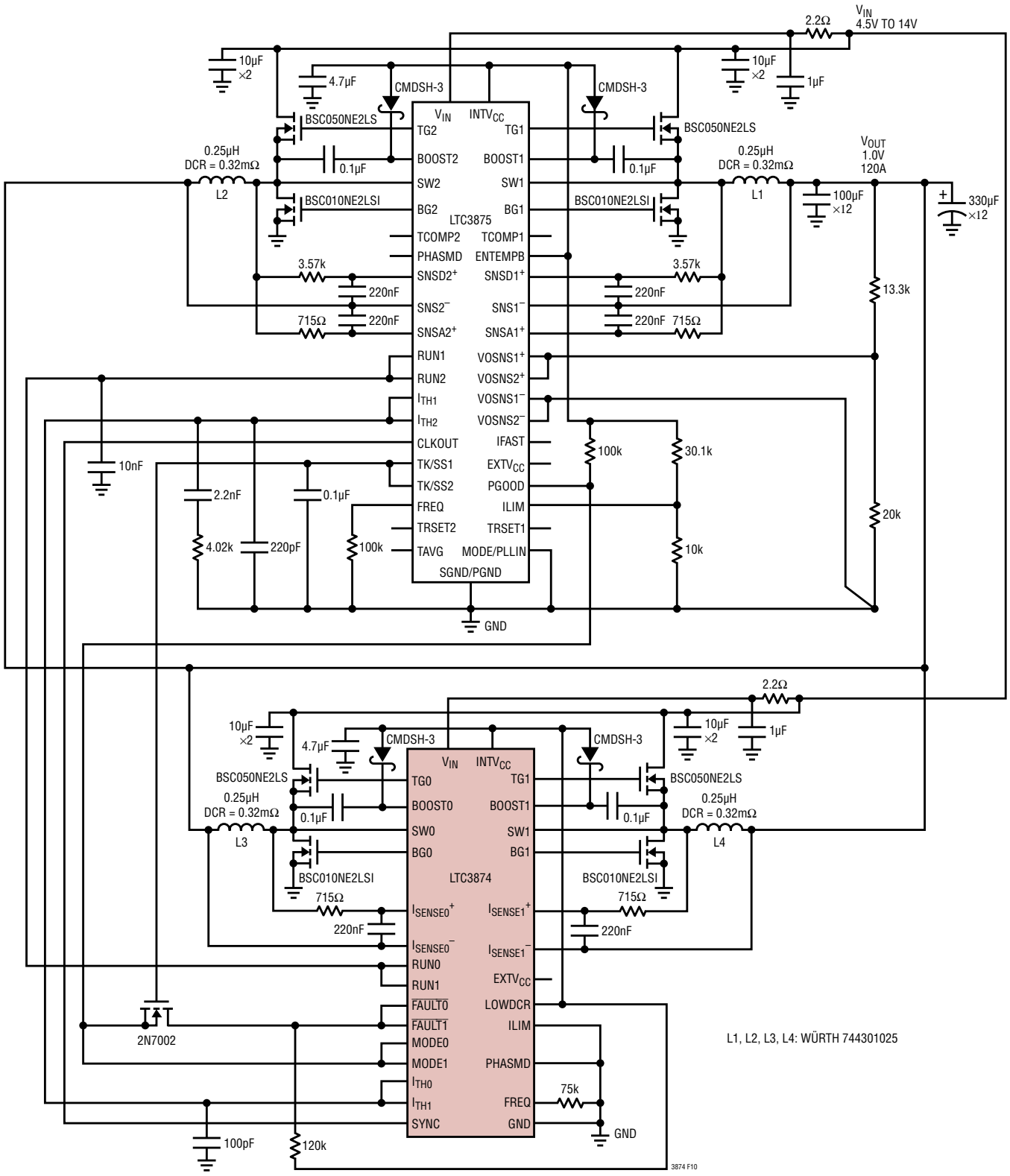


Figure 10. High Efficiency, 4-Phase 1V/120A Step-Down Supply

APPLICATIONS INFORMATION

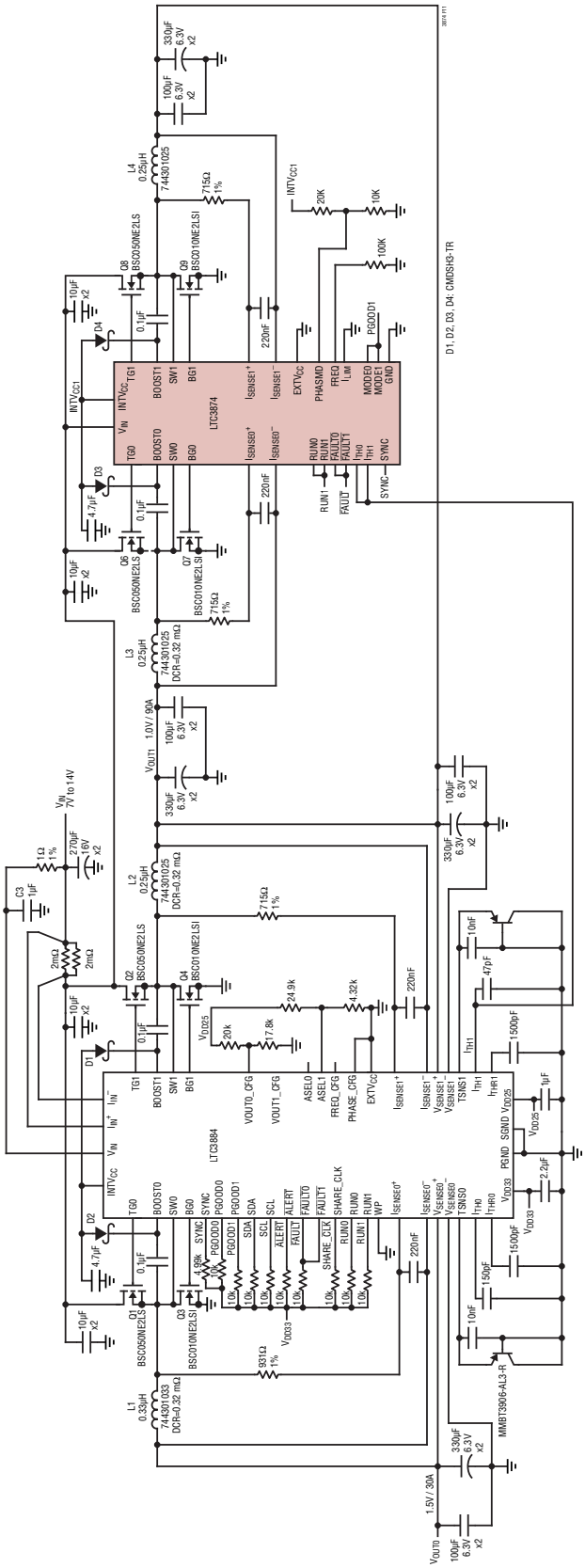
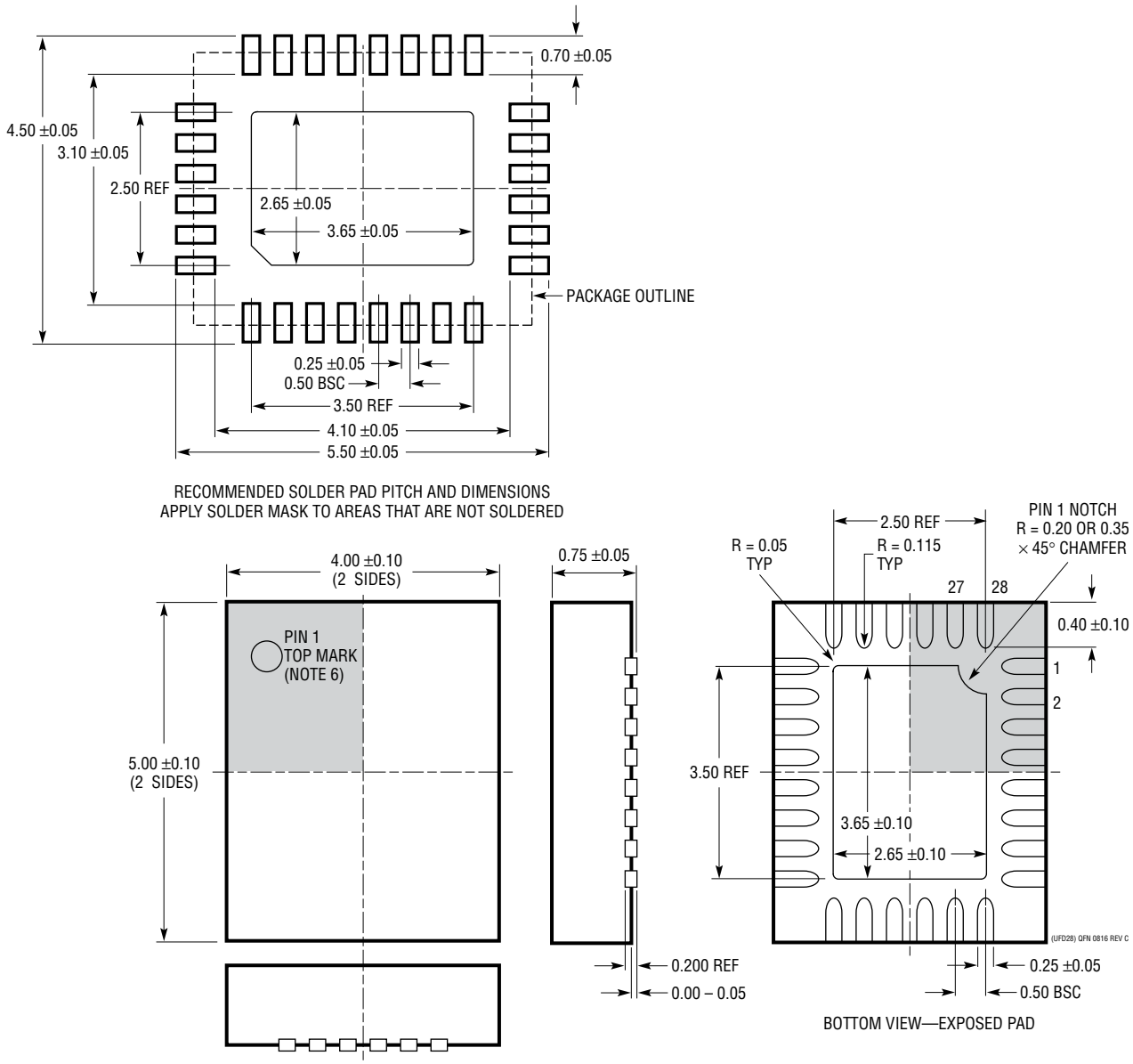


Figure 11. Master/Slave 3 +1 High Efficiency, Dual-Output, 1.5V/30A and 1.0V/90A Buck Converter (LTC3884/LTC3874)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3874#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



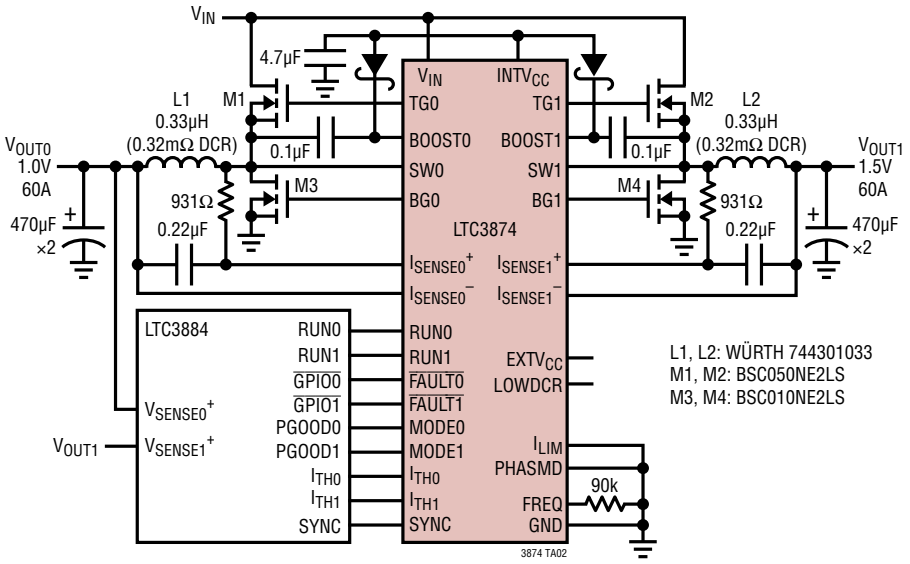
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Added Tape and Reel information link	2
B	01/16	Updated Applications schematic	1
		Added additional drawing to Figure 1	11
		Added application schematic	27
C	05/17	Reduced Minimum On-Time	3
		Changed $V_{ISENSE(MAX)}$ description from Table 1 to Table 3	3

TYPICAL APPLICATION

High Efficiency Dual 1.0V/1.5V Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4676A	Dual 13A or Single 26A Step-Down DC/DC µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤17V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, I^2C/PMBus Interface, 16mm × 16mm × 5mm, BGA Package
LTM4675	Dual 9A or Single 18A µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤17V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, I^2C/PMBus Interface, 11.9mm × 16mm × 5mm, BGA Package
LTM4677	Dual 18A or Single 36A µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤16V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 1.8V, I^2C/PMBus Interface, 16mm × 16mm × 5.01mm, BGA Package
LTC3884	Dual Output Multiphase Step-Down Controller with Sub mΩ DCR Sensing Current Mode Control and Digital Power System Management	4.5V ≤ V_{IN} ≤ 38V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, 70ms Start-Up, I^2C/PMBus Interface, Programmable Analog Loop Compensation, Input Current Sense
LTC3887/ LTC3887-1	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management, 70ms Start-Up	4.5V ≤ V_{IN} ≤ 24V, 0.5V ≤ $V_{OUT0,1}$ (±0.5%) ≤ 5.5V, 70ms Start-Up, I^2C/PMBus Interface, -1 Version Uses DrMOS or Power Blocks
LTC3882/ LTC3882-1	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	3V ≤ V_{IN} ≤ 38V, 0.5V ≤ $V_{OUT1,2}$ ≤ 5.25V, ±0.5% V_{OUT} Accuracy I^2C/PMBus Interface, Uses DrMOS or Power Blocks
LTC3866	Single Output Current Mode Synchronous Step-Down Controller with Sub-Milliohm DCR Sensing	4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V, with Remote V_{OUT} Sense, 4mm × 4mm, QFN-24, TSSOP-24 Packages
LTC3883/ LTC3883-1	Single Phase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Input Current Sense Amplifier, I^2C/PMBus Interface with EEPROM and 16-Bit ADC, ±0.5% V_{OUT} Accuracy
LT3875	Dual, Multiphase Current Mode Synchronous Step-Down Controller with Sub-Milliohm DCR Sensing, Up to 12 Phases	4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V, with Remote Sense
LTC3774	Dual, Multiphase Current Mode Synchronous Step-Down Controller with Sub-Milliohm DCR Sensing, Up to 12 Phases	V_{IN} Up to 40V, 0.6V ≤ V_{OUT} ≤ 3.5V, Very High Output Current Applications with Accurate Current Share Between Phases Supporting LTC3880/-1, LTC3883/-1, LTC3886, LTC3887/-1
LTC3877	Dual Phase Step-Down Synchronous Controller with 6-Bit V_{ID} Output Voltage Programming and Low Value DCR Sensing	4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 1.23V with V_{ID} in 10mV Steps, 0.6V ≤ V_{OUT} ≤ 5V without V_{ID}, Up to 12-Phase Operation

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