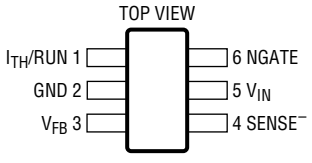
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 10V
SENSE$^-$, NGATE Voltages ..... –0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH}/RUN Voltages ..... –0.3V to 2.4V
NGATE Peak Output Current (<10µs) 1A
Storage Ambient Temperature Range .... –65°C to 150°C
Operating Temperature Range (Note 2).... –40°C to 85°C
Junction Temperature (Note 3) ..... 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



S6 PACKAGE
6-LEAD PLASTIC SOT-23

T_{JMAX} = 150°C, θ_{JA} = 230°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1872BES6#PBF	LTC1872BES6#TRPBF	LTXY	16-Lead Plastic SOT-23	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input DC Supply Current	Typicals at V_{IN} = 4.2V (Note 4)	●				
Normal Operation	2.4V ≤ V_{IN} ≤ 9.8V			270	420	µA
Sleep Mode	2.4V ≤ V_{IN} ≤ 9.8V			230	370	µA
Shutdown	2.4V ≤ V_{IN} ≤ 9.8V, V_{ITH}/RUN = 0V			8	22	µA
UVLO	V_{IN} < UVLO Threshold			6	10	µA
Undervoltage Lockout Threshold	V_{IN} Falling	●	1.55	2.00	2.35	V
	V_{IN} Rising		1.85	2.10	2.40	V
Shutdown Threshold (at I_{TH}/RUN)		●	0.15	0.35	0.55	V
Start-Up Current Source	V_{ITH}/RUN = 0V		0.25	0.5	0.85	µA
Regulated Feedback Voltage	0°C to 70°C(Note 5)	●	0.780	0.800	0.820	V
	–40°C to 85°C(Note 5)	●	0.770	0.800	0.830	V
V_{FB} Input Current	(Note 5)			10	50	nA
Oscillator Frequency	V_{FB} = 0.8V		500	550	650	kHz
Gate Drive Rise Time	C_{LOAD} = 3000pF			40		ns
Gate Drive Fall Time	C_{LOAD} = 3000pF			40		ns
Peak Current Sense Voltage	(Note 6)		114	120		mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1872BE is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$

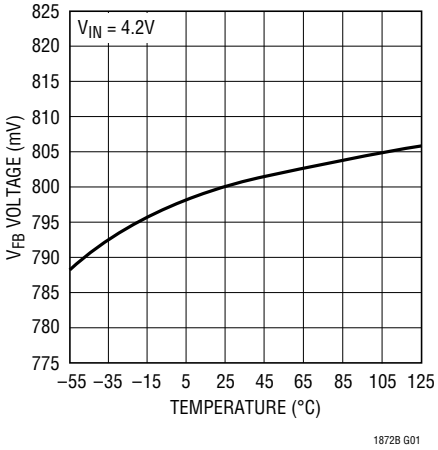
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: The LTC1872B is tested in a feedback loop that servos V_{FB} to the output of the error amplifier.

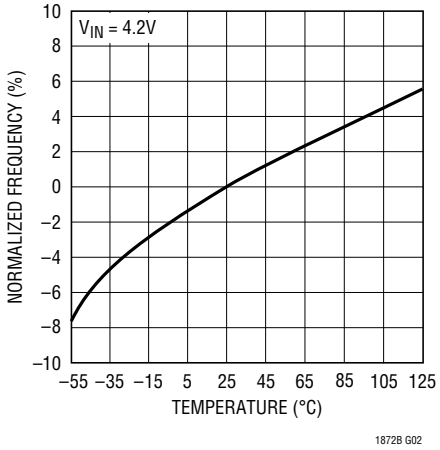
Note 6: Guaranteed by design at duty cycle = 30%. Peak current sense voltage is V_{REF}/6.67 at duty cycle <40%, and decreases as duty cycle increases due to slope compensation as shown in Figure 3.

TYPICAL PERFORMANCE CHARACTERISTICS

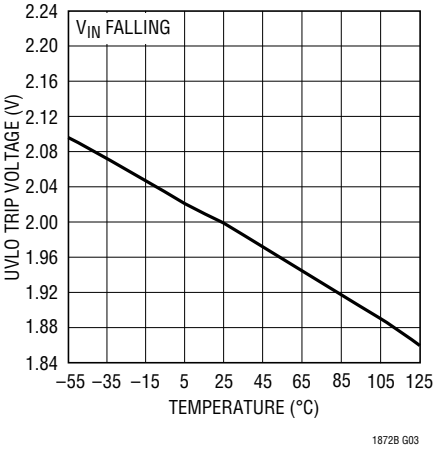
Reference Voltage vs Temperature



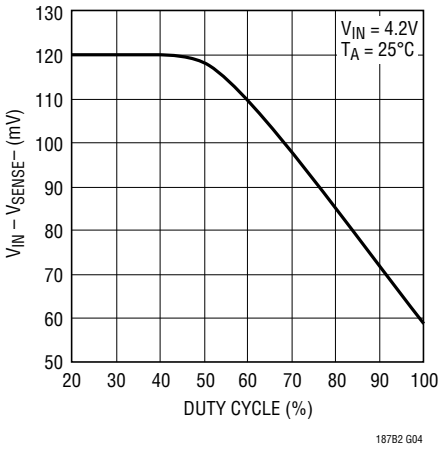
Normalized Oscillator Frequency vs Temperature



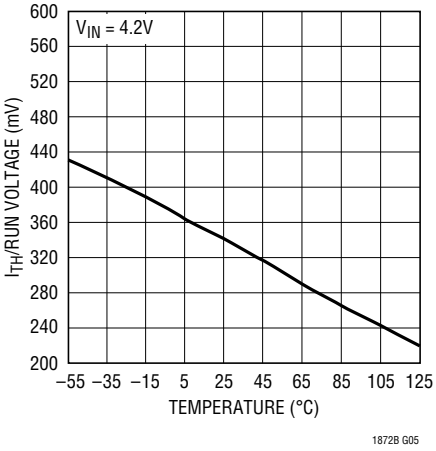
Undervoltage Lockout Trip Voltage vs Temperature



Maximum Current Sense Trip Voltage vs Duty Cycle



Shutdown Threshold vs Temperature



PIN FUNCTIONS

I_{TH}/RUN (Pin 1): This pin performs two functions. It serves as the error amplifier compensation point as well as the run control input. Nominal voltage range for this pin is 0.7V to 1.9V. Forcing this pin below 0.35V causes the device to be shut down. In shutdown all functions are disabled and the NGATE pin is held low.

GND (Pin 2): Ground Pin.

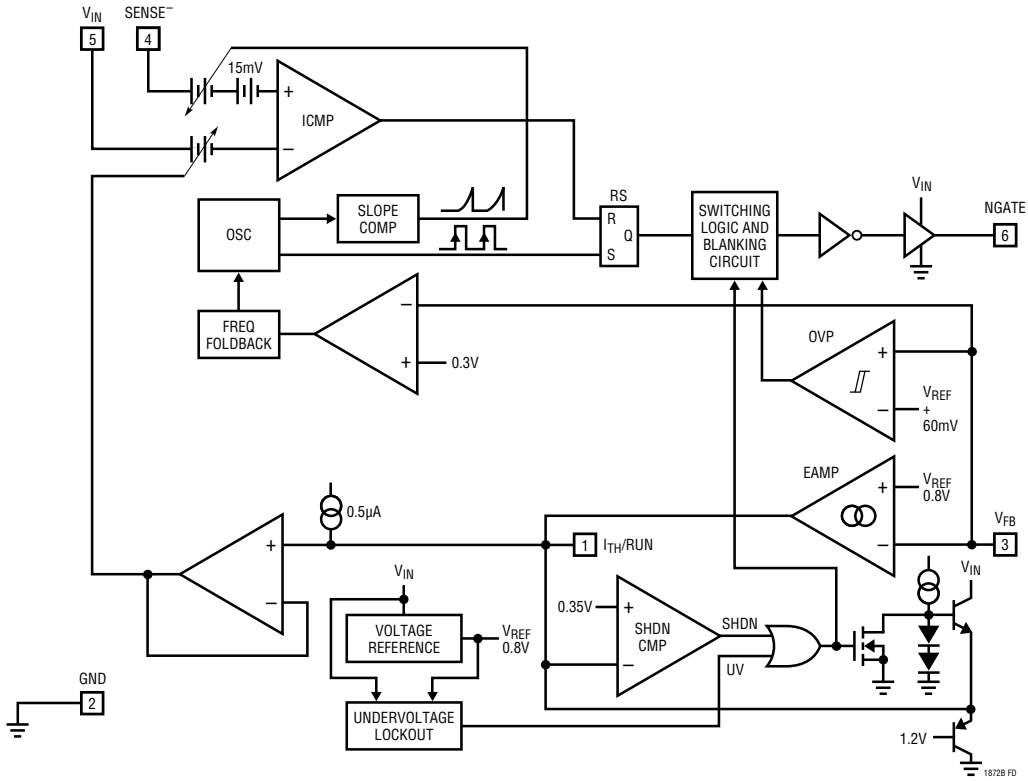
V_{FB} (Pin 3): Receives the feedback voltage from an external resistive divider across the output.

SENSE$^-$ (Pin 4): The Negative Input to the Current Comparator.

V_{IN} (Pin 5): Supply Pin. Must be closely decoupled to GND Pin 2.

NGATE (Pin 6): Gate Drive for the External N-Channel MOSFET. This pin swings from 0V to V_{IN}.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1872B is a constant frequency current mode switching regulator. During normal operation, the external N-channel power MOSFET is turned on each cycle by the oscillator and turned off when the current comparator (ICMP) resets the RS latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the I_{TH}/RUN pin, which is the output of the error amplifier EAMP. An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB}. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH}/RUN voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling the I_{TH}/RUN pin low. Releasing I_{TH}/RUN allows an internal 0.5µA current source to charge up the external compensation network. When the I_{TH}/RUN pin reaches 0.35V, the main control loop is enabled with the I_{TH}/RUN voltage then pulled up to its zero current level of approximately 0.7V. As the external compensation network continues to charge up, the corresponding output current trip level follows, allowing normal operation.

Comparator OVP guards against transient overshoots >7.5% by turning off the external N-channel power MOSFET and keeping it off until the fault is removed.

Low Load Current Operation

Under very light load current conditions, the I_{TH}/RUN pin voltage will be very close to the zero current level of 0.85V. As the load current decreases further, an internal offset at the current comparator input will assure that the current comparator remains tripped (even at zero load current) and the regulator will start to skip cycles, as it must, in order to maintain regulation. This behavior allows the regulator to maintain constant frequency down to very light loads, resulting in less low frequency noise generation over a wide load current range.

OPERATION (Refer to Functional Diagram)

Figure 2 illustrates this result for the circuit of Figure 1 using both an LTC1872 in Burst Mode operation and an LTC1872B (non-Burst Mode operation). At an output current of 50mA, the Burst Mode operation part exhibits an output ripple of approximately 80mV$_{P-P}$, whereas the non-Burst Mode operation part has an output ripple of ≈45mV$_{P-P}$. At lower output current levels, the improvement is even greater. This comes at a trade off of slightly lower efficiency for the non-Burst Mode operation part. Also notice the constant frequency operation of the LTC1872B, even at 5% of maximum output current.

Undervoltage Lockout

To prevent operation of the N-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated into the LTC1872B. When the input supply voltage drops below approximately 2.0V, the N-channel MOSFET and all circuitry is turned off except the undervoltage block, which draws only several microamperes.

Overvoltage Protection

The overvoltage comparator in the LTC1872B will turn the external MOSFET off when the feedback voltage has risen 7.5% above the reference voltage of 0.8V. This comparator has a typical hysteresis of 20mV.

Slope Compensation and Inductor's Peak Current

The inductor's peak current is determined by:

$$I_{PK} = \frac{V_{ITH} - 0.7}{10\,(R_{SENSE})}$$

when the LTC1872B is operating below 40% duty cycle. However, once the duty cycle exceeds 40%, slope compensation begins and effectively reduces the peak inductor current. The amount of reduction is given by the curves in Figure 3.

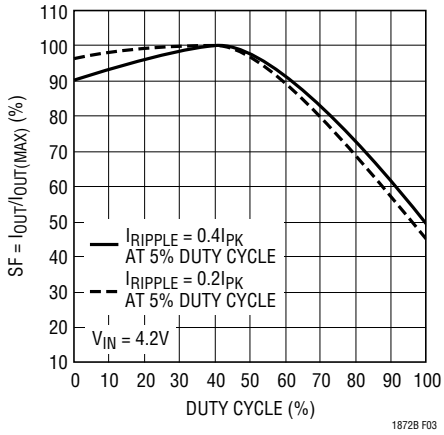
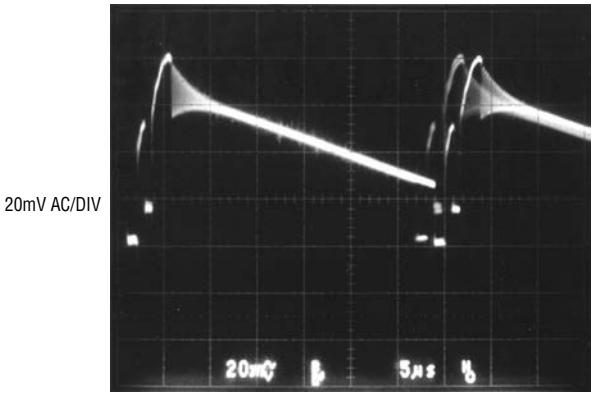
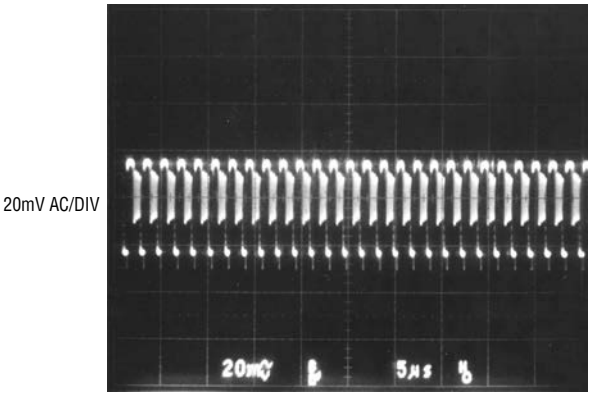


Figure 3. Maximum Output Current vs Duty Cycle



(2a) V_{OUT} Ripple for Figure 1 Circuit Using LTC1872 Burst Mode Operation



(2b) V_{OUT} Ripple for Figure 1 Circuit Using LTC1872B Non-Burst Mode Operation

Figure 2. Output Ripple Waveforms for the Circuit of Figure 1

OPERATION (Refer to Functional Diagram)

Short-Circuit Protection

Since the power switch in a boost converter is not in series with the power path from input to load, turning off the switch provides no protection from a short-circuit at the output. External means such as a fuse in series with the boost inductor must be employed to handle this fault condition.

APPLICATIONS INFORMATION

The basic LTC1872B application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L1 and R_{SENSE} (= R1). Next, the power MOSFET and the output diode D1 is selected followed by C_{IN}(= C1) and C_{OUT}(= C2).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. With the current comparator monitoring the voltage developed across R_{SENSE}, the threshold of the comparator determines the inductor's peak current. The output current the LTC1872B can provide is given by:

$$I_{OUT} = \left(\frac{0.12}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}\right)\frac{V_{IN}}{V_{OUT} + V_D}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation section) and V_D is the forward drop of the output diode at the full rated output current.

A reasonable starting point for setting ripple current is:

$$I_{RIPPLE} = (0.4)(I_{OUT})\frac{V_{OUT} + V_D}{V_{IN}}$$

Rearranging the above equation, it becomes:

$$R_{SENSE} = \frac{1}{(10)(I_{OUT})}\left(\frac{V_{IN}}{V_{OUT} + V_D}\right)$$

for Duty Cycle <40%

However, for operation that is above 40% duty cycle, slope compensation's effect has to be taken into consideration to select the appropriate value to provide the required amount of current. Using the scaling factor (SF, in %) in Figure 3, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{SF}{(10)(I_{OUT})(100)}\left(\frac{V_{IN}}{V_{OUT} + V_D}\right)$$

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses.

The inductance value also has a direct effect on ripple current. The ripple current, I_{RIPPLE}, decreases with higher inductance or frequency and increases with higher V_{OUT}. The inductor's peak-to-peak ripple current is given by:

$$I_{RIPPLE} = \frac{V_{IN}}{f(L)}\left(\frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D}\right)$$

where f is the operating frequency. Accepting larger values of I_{RIPPLE} allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is:

$$I_{RIPPLE} = 0.4\left(I_{OUT(MAX)}\right)\left(\frac{V_{OUT} + V_D}{V_{IN}}\right)$$

In Burst Mode operation, the ripple current is normally set such that the inductor current is continuous during the burst periods. Therefore, the peak-to-peak ripple current must not exceed:

$$I_{RIPPLE} \le \frac{0.03}{R_{SENSE}}$$

APPLICATIONS INFORMATION

This implies a minimum inductance of:

$$L_{MIN} = \frac{V_{IN}}{f\left(\frac{0.03}{R_{SENSE}}\right)}\left(\frac{V_{OUT}+V_D-V_{IN}}{V_{OUT}+V_D}\right)$$

A smaller value than L_{MIN} could be used in the circuit; however, the inductor current will not be continuous during burst periods.

Inductor Selection

When selecting the inductor, keep in mind that inductor saturation current has to be greater than the current limit set by the current sense resistor. Also, keep in mind that the DC resistance of the inductor will affect the efficiency. Off the shelf inductors are available from Murata, Coilcraft, Toko, Panasonic, Coiltronics and many other suppliers.

Power MOSFET Selection

The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$, the "on" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and total gate charge.

Since the LTC1872B is designed for operation down to low input voltages, a logic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC1872B is less than the absolute maximum V_{GS} rating, typically 8V.

The required minimum $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation given by:

$$R_{DS(ON)} \cong \frac{P_P}{(DC)\,I_{IN}^{\,2}(1+\delta p)}$$

where P_P is the allowable power dissipation and δp is the temperature dependency of $R_{DS(ON)}$. (1 + δp) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δp = 0.005/°C can be used as an approximation for low voltage MOSFETs. DC is the maximum operating duty cycle of the LTC1872B.

Output Diode Selection

Under normal load conditions, the average current conducted by the diode in a boost converter is equal to the output load current:

$$I_{D(avg)} = I_{OUT}$$

It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Schottky diodes are recommended for low forward drop and fast switching times. Remember to keep lead length short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

C_{IN} and C_{OUT} Selection

To prevent large input voltage ripple, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current for a boost converter is approximately equal to:

$$C_{IN} \text{ Required } I_{RMS} \approx (0.3)I_{RIPPLE}$$

where I_{RIPPLE} is as defined in the Inductor Value Calculation section.

Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the LTC1872B, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

APPLICATIONS INFORMATION

$$\Delta V_{OUT} \approx \left(I_O \bullet \frac{V_{OUT} + V_D}{V_{IN}} + \frac{I_{RIPPLE}}{2} \right) \bullet \left[ESR^2 + \left(\frac{1}{2\pi f C_{OUT}} \right)^2 \right]^{\frac{1}{2}}$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price. The output capacitor RMS current is approximately equal to:

$$I_{PK} \bullet \sqrt{DC - DC^2}$$

where I_{PK} is the peak inductor current and DC is the switch duty cycle.

When using electrolytic output capacitors, if the ripple and ESR requirements are met, there is likely to be far more capacitance than required.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. An excellent choice of tantalum capacitors is the AVX TPS and KEMET T510 series of surface mount tantalum capacitors. Also, ceramic capacitors in X5R pr X7R dielectrics offer excellent performance.

Low Supply Operation

Although the LTC1872B can function down to approximately 2.0V, the maximum allowable output current is reduced when V_{IN} decreases below 3V. Figure 4 shows the amount of change as the supply is reduced down to 2V. Also shown in Figure 4 is the effect of V_{IN} on V_{REF} as V_{IN} goes below 2.3V.

Setting Output Voltage

The LTC1872B develops a 0.8V reference voltage between the feedback (Pin 3) terminal and ground (see Figure 5). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V \left(1 + \frac{R2}{R1} \right)$$

For most applications, an 80k resistor is suggested for R1. To prevent stray pickup, locate resistors R1 and R2 close to LTC1872B.

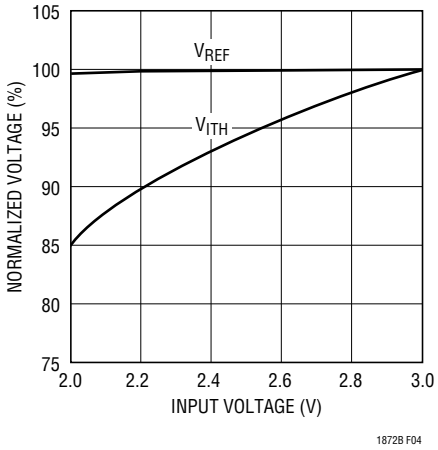


Figure 4. Line Regulation of V_{REF} and V_{ITH}

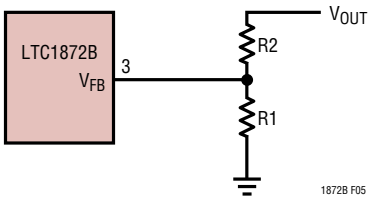


Figure 5. Setting Output Voltage

APPLICATIONS INFORMATION

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (η1 + η2 + η3 + ...)

where η1, η2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1872B circuits: 1) LTC1872B DC bias current, 2) MOSFET gate charge current, 3) I^2R losses and 4) voltage drop of the output diode.

1. The V_{IN} current is the DC supply current, given in the electrical characteristics, that excludes MOSFET driver and control currents. V_{IN} current results in a small loss which increases with V_{IN}.
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the contoller's DC supply current. In continuous mode, $I_{GATECHG} = f(Qp)$.
3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current sense resistor. The MOSFET $R_{DS(ON)}$ multiplied by duty cycle times the average output current squared can be summed with I^2R losses in the inductor ESR in series with the current sense resistor.
4. The output diode is a major source of power loss at high currents. The diode loss is calculated by multiplying the forward voltage by the load current.
5. Transition losses apply to the external MOSFET and increase at higher operating frequencies and input voltages. Transition losses can be estimated from:

   Transition Loss = $2(V_{IN})^2 I_{IN(MAX)} C_{RSS}(f)$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses, and inductor core losses, generally account for less than 2% total additional loss.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1872B. These items are illustrated graphically in the layout diagram in Figure 6. Check the following in your layout:

1. The Schottky diode should be closely connected between the output capacitor and the drain of the external MOSFET.
2. The (+) plate of C_{IN} should connect to the sense resistor as closely as possible. This capacitor provides AC current to the inductor.
3. The input decoupling capacitor (0.1µF) should be connected closely between V_{IN} (Pin 5) and ground (Pin 2).
4. Connect the end of R_{SENSE} as close to V_{IN} (Pin 5) as possible. The V_{IN} pin is the $SENSE^+$ of the current comparator.
5. The trace from $SENSE^-$ (Pin 4) to the Sense resistor should be kept short. The trace should connect close to R_{SENSE}.
6. Keep the switching node NGATE away from sensitive small signal nodes.
7. The V_{FB} pin should connect directly to the feedback resistors. The resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.

APPLICATIONS INFORMATION

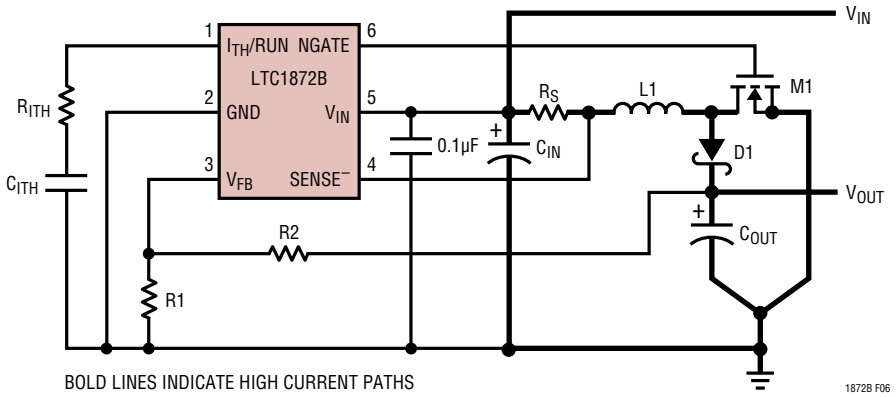
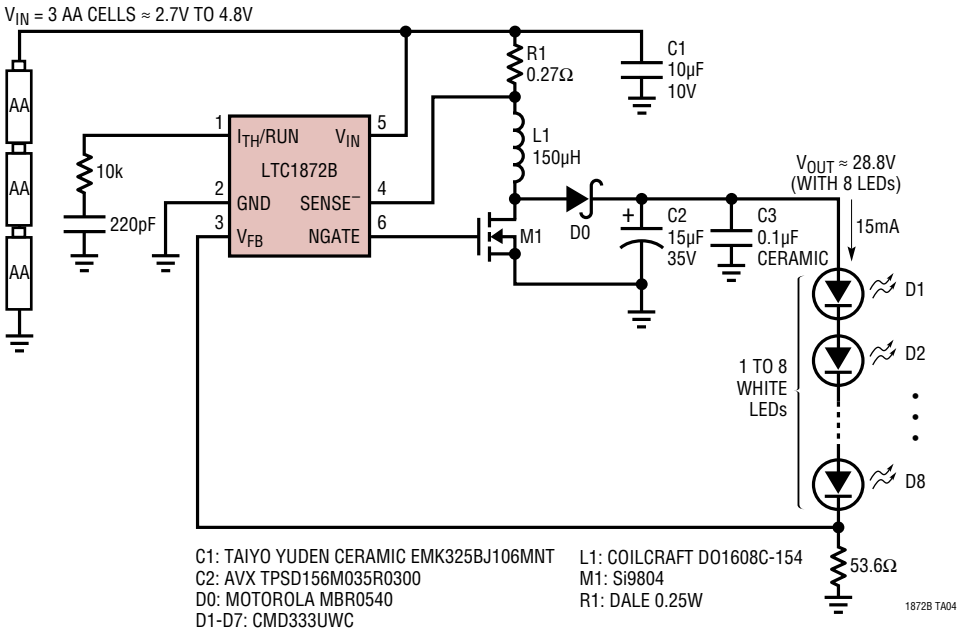


Figure 6. LTC1872B Layout Diagram (See PC Board Layout Checklist)

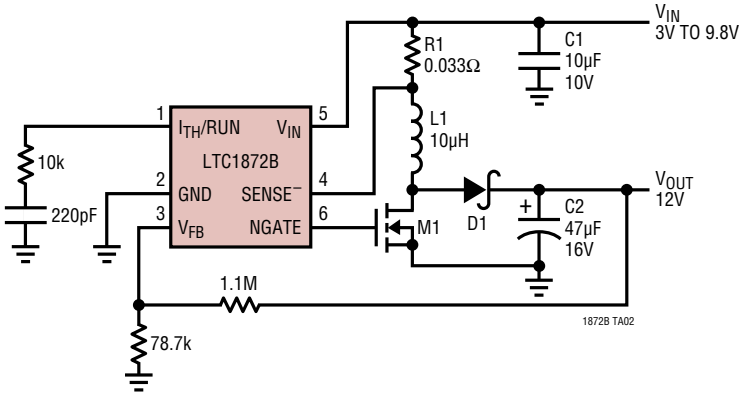
TYPICAL APPLICATIONS

LTC1872B 3-Cell White LED Driver



APPLICATIONS INFORMATION

LTC1872B 12V/500mA Boost Converter

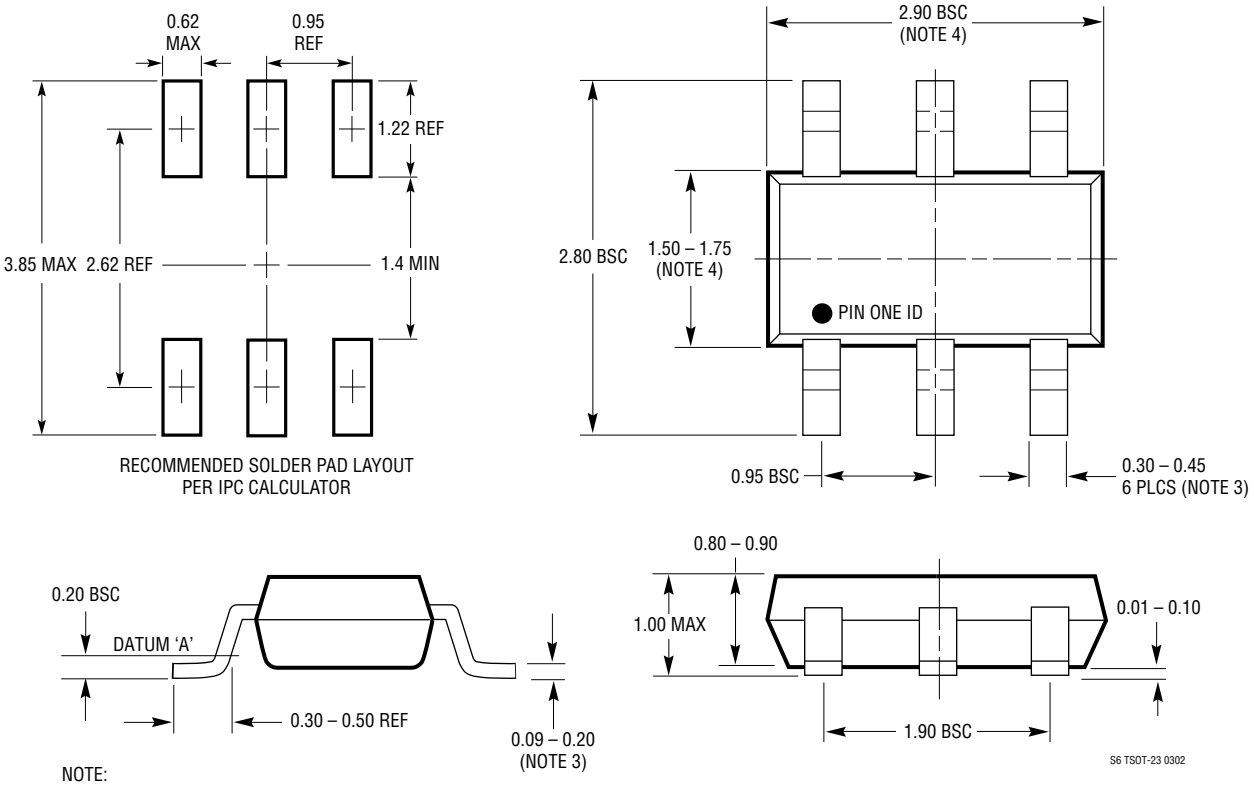


C1: TAIYO YUDEN CERAMIC EMK325BJ106MNT
C2: AVX TPSE476M016R0150
D1: IR10BQ015
L1: COILTRONICS UP2B-100
M1: Si9804DV
R1: DALE 0.25W

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



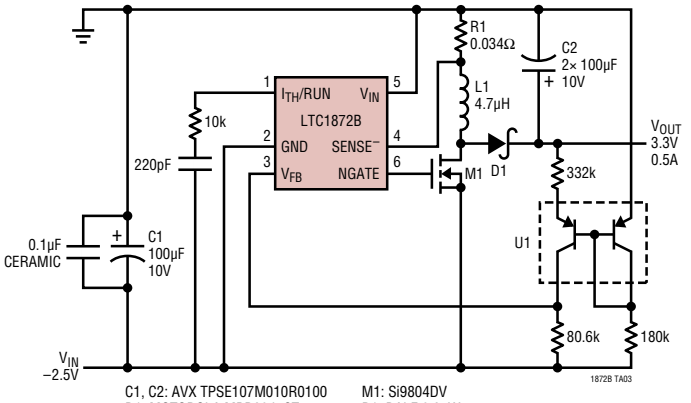
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/15	Revised package drawing	12

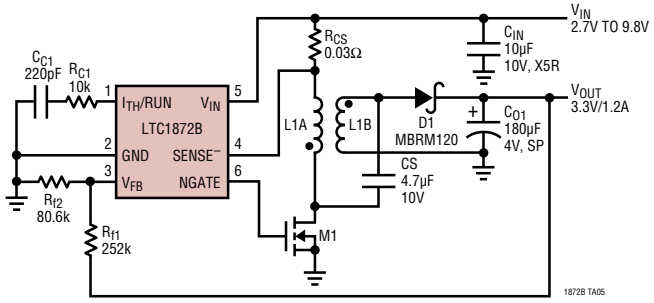
TYPICAL APPLICATION

LTC1872B –2.5V to 3.3V/0.5A Boost Converter



C1, C2: AVX TPSE107M010R0100
D1: MOTOROLA MBR2045CT
L1: COILTRONICS UP2B-4R7
M1: Si9804DV
R1: DALE 0.25W
U1: PANASONIC 2SB709A

LTC1872B 2.7V to 9.8V Input to 3.3V/1.2A Output SEPIC Converter



CIN, CS; TOKO, MURATA OR TAIYO YUDEN
CO1: PANASONIC EEFUE0G181R
L1: BH ELECTRONICS 511-1012
M1: IRLMS2002
RCS: DALE OR IRC

FOR VOUT = 5V CHANGE
Rf1 TO 427kΩ AND
CO1 TO 150µF, 6V PANASONIC
SP TYPE CAPACITOR

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1304	Micropower DC/DC Converter with Low-Battery Detector	120µA Quiescent Current, 1.5V ≤ V_{IN} ≤ 8V
LT1610	1.7MHz, Single Cell Micropower DC/DC Converter	30µA Quiescent Current, V_{IN} Down to 1V
LT1613	1.4MHz, Single Cell DC/DC Converter in 5-Lead ThinSOT	Internally Compensated, V_{IN} Down to 1V
LT1619	Low Voltage Current Mode PWM Controller	8-Lead MSOP Package, 1.9V ≤ V_{IN} ≤ 18V
LT1680	High Power DC/DC Step-Up Controller	Operation Up to 60V, Fixed Frequency Current Mode
LTC1624	High Efficiency SO-8 N-Channel Switching Regulator Controller	8-Pin N-Channel Drive, 3.5V ≤ V_{IN} ≤ 36V
LT1615	Micropower Step-Up DC/DC Converter in ThinSOT	20µA Quiescent Current, V_{IN} Down to 1V
LTC1700	No R_{SENSE} Synchronous Current Mode DC/DC Step-Up Controller	95% Efficient, 0.9V ≤ V_{IN} ≤ 5V, 550kHz Operation
LTC1772	Constant Frequency Current Mode Step-Down DC/DC Controller	V_{IN} 2.5V to 9.8V, I_{OUT} up to 4A, ThinSOT Package
LTC1872	Constant Frequency Current Mode Step-Up DC/DC Controller in ThinSOT	With Burst Mode Operation for Higher Efficiency at Light Load Current
LTC3401/LTC3402	1A/2A, 3MHz Micropower Synchronous Boost Converter	10-Lead MSOP Package, 0.5V ≤ V_{IN} ≤ 5V

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