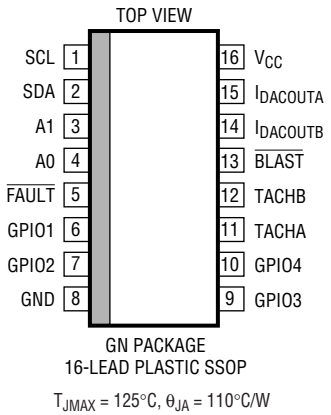
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{CC}$ to GND ..... –0.3 to 6V
A0, A1 ..... –0.3 to ($V_{CC}$ + 0.3V)
$I_{DACOUTA}$, $I_{DACOUTB}$ ..... –0.3 to ($V_{CC}$ + 0.75V)
All other pins ..... –0.3 to 6V
Operating Temperature
LTC1840C ..... 0°C to 70°C
LTC1840I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




GN PACKAGE
16-LEAD PLASTIC SSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 110°C/W

| ORDER PART NUMBER |
|---|
| LTC1840CGN<br>LTC1840IGN |
| **GN PART MARKING** |
| 1840<br>1840I |

Consult LTC marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3V**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DACs** | | | | | | | |
| n | Resolution | | | 8 | | | Bits |
| DNL | Differential Nonlinearity | $V_{DACOUT}$ = 1.1V, Guaranteed Monotonic | ● | | | ±0.9 | LSB |
| INL | Integral Nonlinearity | $V_{DACOUT}$ = 1.1V | | | | ± 4 | LSB |
| ZSE | Zero-Scale Error | $V_{DACOUT}$ = 1.1V | | –0.2 | 0.1 | 2 | µA |
| | Output Voltage Rejection | 1.1V< $V_{DACOUT}$ < 3.75V | | | | ±1 | LSB |
| | Output Voltage Rejection | $V_{CC}$ = 5.75V, 1.1V < $V_{DACOUT}$ < 6.5V | | | | ±2 | LSB |
| $I_{DACOUTA(FS)}$,<br>$I_{DACOUTB(FS)}$ | Full-Scale Current | Sinking<br>$V_{DACOUT}$ = 1.1V | <br>● | 97<br>95 | | 103<br>105 | µA<br>µA |
| **Power Supply** | | | | | | | |
| $V_{CC}$ | Positive Supply Voltage | | ● | 2.7 | | 5.75 | V |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 3V, A0 and A1 Floating<br>$V_{CC}$ = 5V, A0 and A1 Floating | | | 400<br>500 | 600<br>750 | µA<br>µA |
| $V_{UVLO}$ | UVLO/POR Voltage | | ● | 2.1 | 2.4 | 2.69 | V |
| $V_{UVHYS}$ | UVLO/POR Voltage Hysteresis | (Note 2) | | 20 | 90 | 160 | mV |
| **Oscillator Performance** | | | | | | | |
| $f_{OSC}$ | Oscillator Frequency | | ● | 47 | 50 | 53 | kHz |
| PSRR | Supply Sensitivity | 2.7V < $V_{CC}$ < 5.75V | | | 0.1 | 0.5 | %/V |
| **GPIO Performance** | | | | | | | |
| $I_O$ | Output Current Sink | $V_{GPIOX}$ = 0.7V, Internal Pull-Down Enabled | ● | 10 | | | mA |
| $V_{IL}$ | Digital Input Low Voltage | Internal Pull-Down Disabled | ● | | | 0.3$V_{CC}$ | V |
| $V_{IH}$ | Digital Input High Voltage | Internal Pull-Down Disabled | ● | 0.7$V_{CC}$ | | | V |
| $V_{IHYST}$ | Input Hysteresis | (Note 2) | | 50 | | | mV |
| $I_{LEAK}$ | Leakage | Internal Pull-Down Disabled | | | | ±1 | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3V**

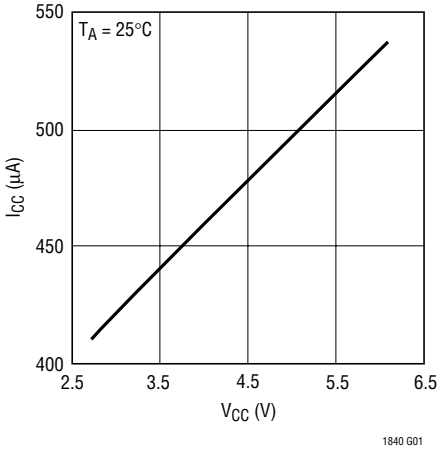
| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Digital Inputs SCL, SDA** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | | ● | 1.4 | | | V |
| $V_{IL}$ | Digital Input Low Voltage | | ● | | | 0.6 | V |
| $V_{LTH}$ | Logic Threshold Voltage | (Note 2) | | | 1 | | V |
| $I_{LEAK}$ | Digital Input Leakage | $V_{CC}$ = 5V and 0V, $V_{IN}$ = GND to $V_{CC}$ | | | | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 2) | | | | 10 | pF |
| **Digital Output SDA** | | | | | | | |
| $V_{OL}$ | Digital Output Low Voltage | $I_{PULL-UP}$ = 3mA | ● | | | 0.4 | V |
| **Digital Output $\overline{FAULT}$** | | | | | | | |
| $V_{OL}$ | Digital Output Low Voltage | $I_{PULL-UP}$ = 1mA | ● | | | 0.4 | V |
| **Digital Inputs TACHA, TACHB** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | | ● | $0.7V_{CC}$ | | | V |
| $V_{IL}$ | Digital Input Low Voltage | | ● | | | $0.3V_{CC}$ | V |
| $I_{LEAK}$ | Digital Input Leakage | $V_{CC}$ = 5V and 0V, $V_{IN}$ = GND to $V_{CC}$ | | | | ±1 | µA |
| **Digital Input $\overline{BLAST}$** | | | | | | | |
| $V_{LTH}$ | Logic Threshold Voltage | Measured on $\overline{BLAST}$ Falling Edge | | 0.95 | 1.0 | 1.05 | V |
| $V_{IHYST}$ | Input Hysteresis | (Note 2), Measured on Rising Edge | | 20 | | | mV |
| $I_{LEAK}$ | Digital Input Leakage | $V_{CC}$ = 5V and 0V, $V_{IN}$ = GND to $V_{CC}$ | | | | ±1 | µA |
| **Address Inputs A0, A1** | | | | | | | |
| $V_{IH}$ | Input High Voltage | | ● | $0.9V_{CC}$ | | | V |
| $V_{IL}$ | Input Low Voltage | | ● | | | $0.1V_{CC}$ | V |
| $I_{IN}$ | Input Current | AX Shorted to GND or $V_{CC}$, $V_{CC}$ = 5V | | | | ±100 | µA |
| **Timing Characteristics** | | | | | | | |
| $f_{I2C}$ | $I^2C$ Operating Frequency | (Note 2) | | 0 | | 100 | kHz |
| $t_{BUF}$ | Bus Free Time Between Stop and Start Condition | (Note 2) | | 4.7 | | | µs |
| $t_{hD, STA}$ | Hold Time after (Repeated) Start Condition | (Note 2) | | 4 | | | µs |
| $t_{su, STA}$ | Repeated Start Condition Setup Time | (Note 2) | | 4.7 | | | µs |
| $t_{su, STO}$ | Stop Condition Setup Time | (Note 2) | | 4 | | | µs |
| $t_{hD, DAT}$ | Data Hold Time | | | 300 | | | ns |
| $t_{su, DAT}$ | Data Setup Time | (Note 2) | | 250 | | | ns |
| $t_{LOW}$ | Clock Low Period | (Note 2) | | 4.7 | | | µs |
| $t_{HIGH}$ | Clock High Period | (Note 2) | | 4.0 | | | µs |
| $t_f$ | Clock, Data Fall Time | (Note 2) | | | | 300 | ns |
| $t_r$ | Clock, Data Rise Time | (Note 2) | | | | 1000 | ns |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Guaranteed by design not subject to test.

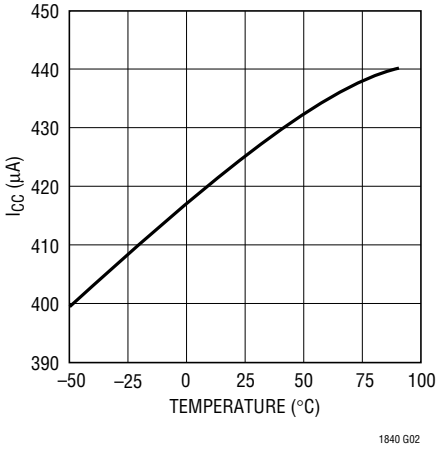
## TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current vs Supply Voltage**



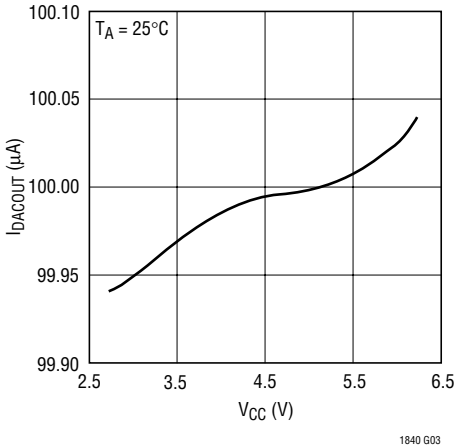

1840 G01

**Supply Current vs Temperature ($V_{CC}$ = 3V)**



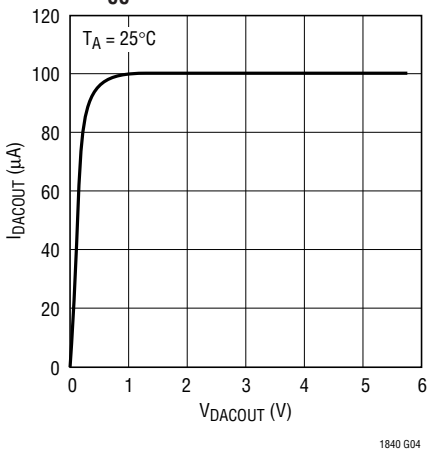

1840 G02

**$I_{DACOUT}$ Full Scale vs $V_{CC}$, $V_{DACOUT}$ = 1.1V**



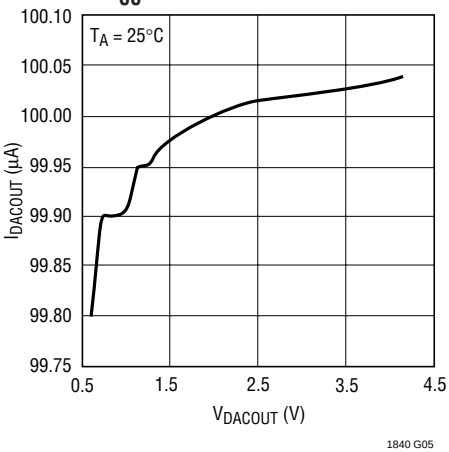

1840 G03

**$I_{DACOUT}$ FS vs $V_{DACOUT}$ at $V_{CC}$ = 3V to 5V**



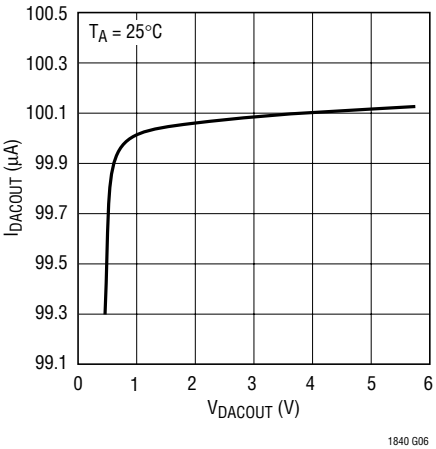

1840 G04

**$I_{DACOUT}$ FS vs $V_{DACOUT}$ at $V_{CC}$ = 3V**



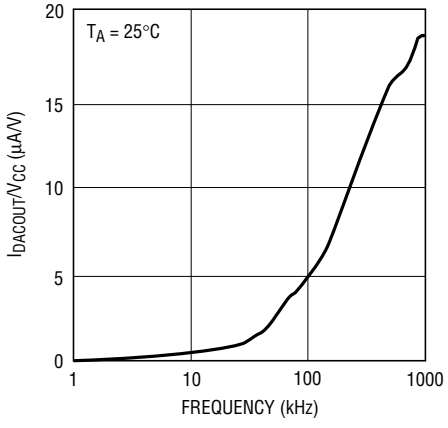

1840 G05

**$I_{DACOUT}$ FS vs $V_{DACOUT}$ at $V_{CC}$ = 5V**



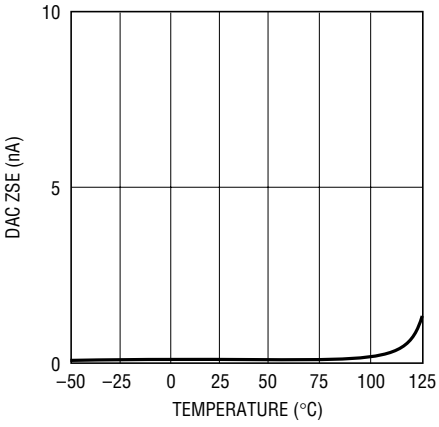

1840 G06

**$I_{DACOUT}$ AC Supply Rejection at Full Scale, $V_{CC}$ = 3V DC**



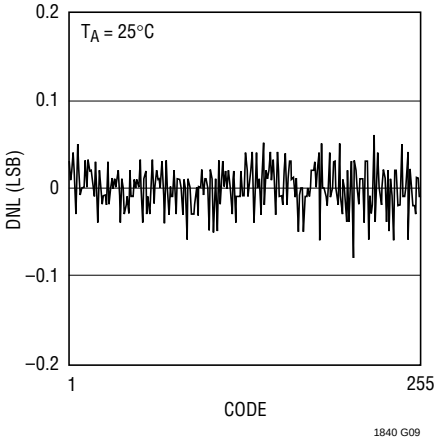

1840 G07

**DAC Zero Scale Error at $V_{CC}$ = 3V, $V_{DACOUT}$ = 1.1V**




1840 G08

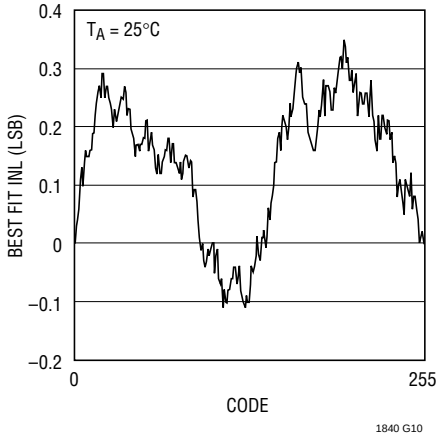
**DAC DNL vs Code at $V_{CC}$ = 3V**



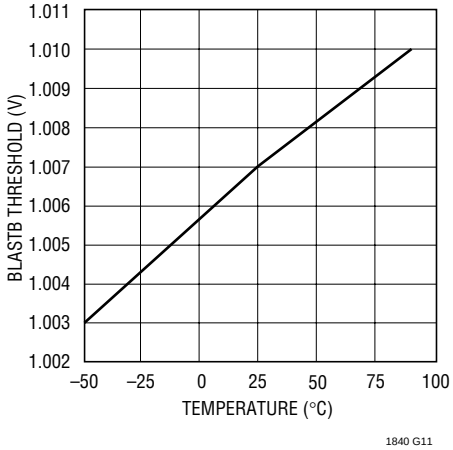

1840 G09

## TYPICAL PERFORMANCE CHARACTERISTICS

**DAC INL at $V_{CC}$ = 3V**




**$\overline{BLAST}$ Falling Threshold at $V_{CC}$ = 3V**




## PIN FUNCTIONS

**SCL (Pin 1):** Serial Clock Input. The 2-wire bus master device clocks this pin at a frequency between 0kHz and 100kHz to enable serial bus communications. Data at the SDA pin is shifted in or out on rising SCL edges. SCL has a logic threshold of 1V and an external pull-up resistor or current source is normally required.

**SDA (Pin 2):** Serial Data Input. This is a bidirectional data pin which normally has an external pull-up resistor or current source and can be pulled down by the open drain device on the LTC1840 or by external devices. The master controls SDA during addressing, the writing of data, and read acknowledgment, while the LTC1840 controls SDA when data is being read back and during write acknowledgment. SDA data is shifted in or out on rising SCL edges. SDA has a logic threshold of 1V.

**A1 (Pin 3):** Three State Address Programming Input. This pin can cause three different logic states internally, depending upon whether it is pulled to supply, pulled to ground, or not connected (NC). Combined with the A0 pin, this provides for nine different possible two-wire bus addresses for the LTC1840 (see Table 1).

**A0 (Pin 4):** Three State Address Programming Input. See A1.

**$\overline{FAULT}$ (Pin 5):** Fault Indicator Pull-Down Output. This pin has an open drain pull-down that is used to signal various fault conditions on the LTC1840. An external 10k pull-up is recommended.

**GPIO1, GPIO2, GPIO3, GPIO4 (Pins 6, 7, 9, 10):** General Purpose Inputs/Outputs. These pins can be used as digital inputs with CMOS logic thresholds or digital outputs/LED drivers with open drain pull-downs that can be programmed to blink. GPIO pins can be programmed to produce faults due to changes in their logic states, and these faults can only be cleared by software or powering the LTC1840 down. All GPIOs default to nonfaulting logic inputs upon power-up and their functionality is changed through the serial interface.

**GND (Pin 8):** Ground. Connect to analog ground plane.

**TACHA (Pin 11):** Tachometer Input A. This pin is a digital input that is designed to interface to the tachometer output from a 3-wire fan. Internal logic counts between rising TACHA edges at serially programmable frequencies of 25kHz, 12.5kHz, 6.25kHz or 3.125kHz and the most recently completed count is stored in a register accessible through the serial interface. The maximum count is 255 and the LTC1840 is programmable to produce faults when a count exceeds this number. This pin has CMOS thresholds and the default conditions are to count at 3.125kHz and to not produce faults.

**TACHB (Pin 12):** Tachometer Input B. See TACHA

## PIN FUNCTIONS

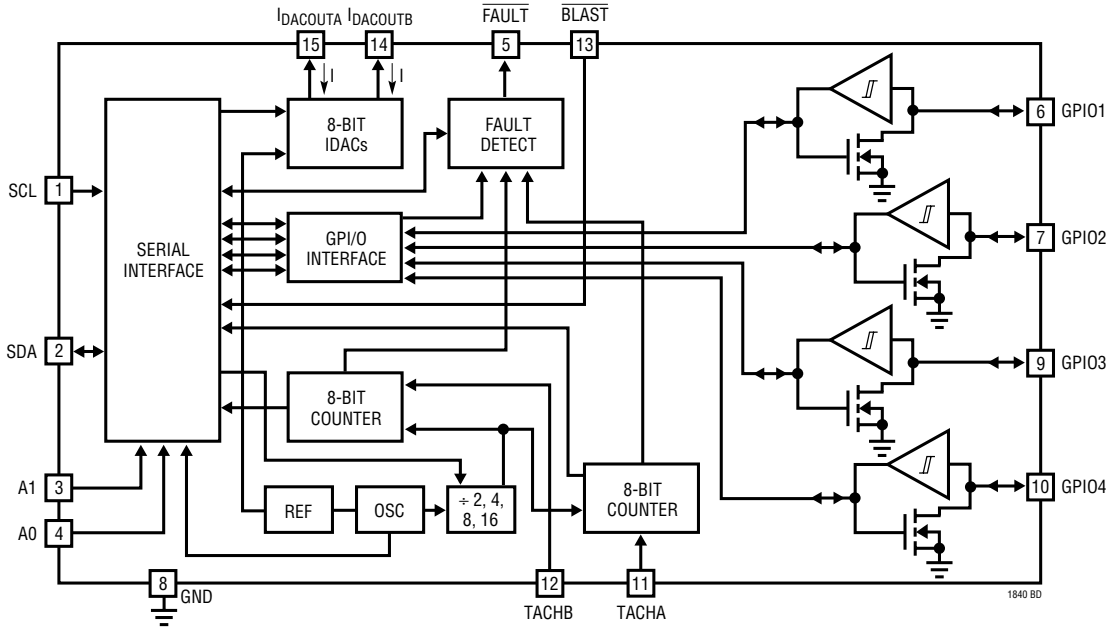
**$\overline{\text{BLAST}}$ (Pin 13):** Blast/Timer Function Input. This is a multifunction digital input pin that controls blast and timer operation. If this pin is in a logic high state at power-up or is transitioned from high to low, it will "blast" the current DAC outputs to full scale (100µA) no matter what their previous state was and set a fault condition. In addition, if $\overline{\text{BLAST}}$ is in a logic high state, the serial access timer is active; this circuit measures time between serial communications to the LTC1840 and forces a blast and trips a fault if the part hasn't been accessed for about 1.5 minutes. This pin has a 1V logic threshold.

**$I_{DACOUTB}$ (Pin 14):** Current DAC Output B. This is a high impedance output with a sinking current output of 0µA to 100µA. This current can be programmed to one of 256 values through the serial interface or it can be "blasted" immediately to full scale using the $\overline{\text{BLAST}}$ pin or by the serial access timer if it is enabled and the LTC1840 is not accessed for about 1.5 minutes. This pin will maintain the programmed current to a very tight tolerance from as low as 1.1V to at least 0.75V above $V_{CC}$. The current DAC is guaranteed to be monotonic over its full 8-bit range.

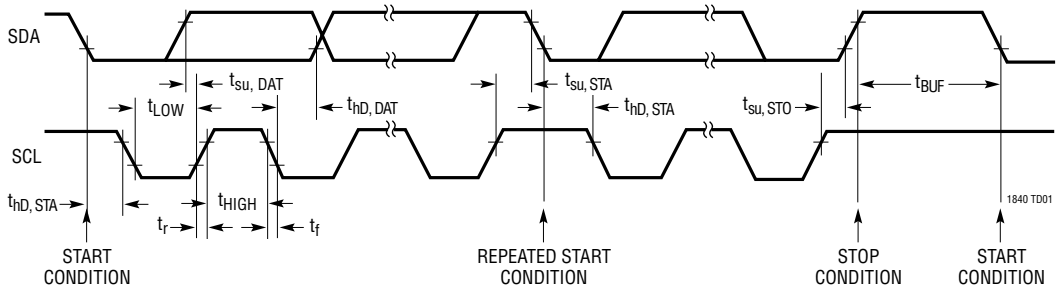
**$I_{DACOUTA}$ (Pin 15):** Current DAC Output A. See $I_{DACOUTB}$

**$V_{CC}$ (Pin 16):** Positive Supply. This pin must be closely decoupled to ground (pin 8). A 10µF tantalum and a 0.1µF ceramic capacitor in parallel are recommended.

## BLOCK DIAGRAM

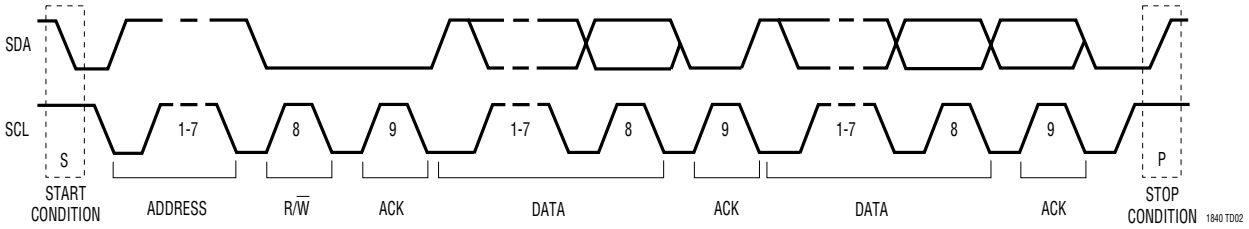



## TIMING DIAGRAM



# OPERATION

**Typical 2-Wire Serial I²C or SMBus Transmission**




## Serial Interface

- Simple 2-wire interface
- Multiple devices on same bus
- Idle bus must have SDA and SCL lines high
- LTC1840 is read/write
- Master controls bus
- Devices listen for unique address that precedes data

## The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

## Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. An acknowledge (LOW active) generated by the slave lets the master know that the latest byte of information was received. The acknowledge-related clock pulse is generated by the master. The transmitter master releases the SDA line (HIGH) during the acknowledge clock pulse. The slave receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

When a slave receiver doesn't acknowledge the slave address (for example, it's unable to receive because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver acknowledges the slave address, but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the "not acknowledge" on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

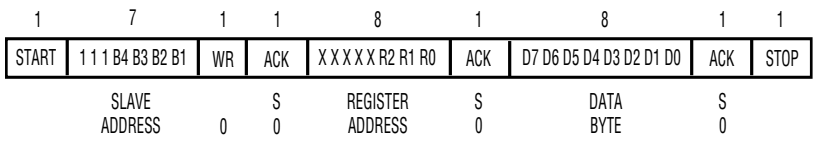
## Commands Supported

The LTC1840 supports read byte, write byte, read word (the second data byte will be all ones) and write word (the second data byte will be ignored) commands.

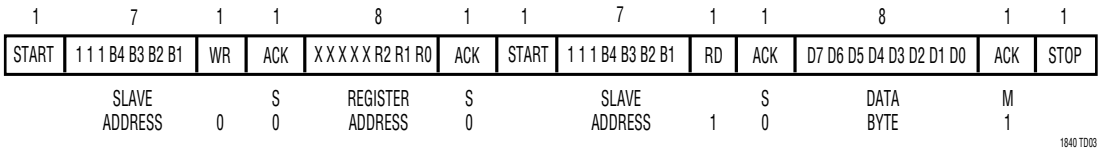
## Data Transfer Timing for Write Commands

In order to help assure that bad data is not written into the LTC1840, data from a write command is only stored after a valid acknowledge has been performed. The part will detect that SDA is low on the rising edge of SCL that marks the end of the period in which the LTC1840 acknowledges the data write and then latch the data during the following SCL low period.

**LTC1840 Write Byte Protocol**




**LTC1840 Read Byte Protocol**



# OPERATION

## LTC1840 Device Addressing

It is possible to configure the part to operate with any one of nine separate addresses through the three state A0 and A1 pins. Table 1 shows the correspondence of addresses to the states of the pins:

**Table 1. Device Addressing**

| LTC1840 Device Address | | 2-Wire Bus Slave Address Bits (B7,B6,B5 = 111) | | | |
|---|---|---|---|---|---|
| **A0** | **A1** | **B4** | **B3** | **B2** | **B1** |
| L | NC | 0 | 0 | 0 | 0 |
| NC | H | 0 | 0 | 0 | 1 |
| NC | NC | 0 | 0 | 1 | 0 |
| H | NC | 0 | 0 | 1 | 1 |
| L | L | 0 | 1 | 0 | 0 |
| H | H | 0 | 1 | 0 | 1 |
| NC | L | 0 | 1 | 1 | 0 |
| H | L | 0 | 1 | 1 | 1 |
| L | H | 1 | 0 | 0 | 0 |

For the A0 and A1 lines, L refers to a grounded pin, H is a pin shorted to $V_{CC}$ and NC is no connect. The pin voltage will be set to approximately $V_{CC}/2$ when not connected. Bits B7, B6 and B5 of the address are hardwired to 111.

## Register Addresses and Contents

Fault conditions are cleared by the action of writing to the fault register, but the data byte from the write command is not actually loaded into the register.

A TACHA/B FLT (fault) bit will be high if the corresponding TACHA/B FLTEN bit in the status register has been set high and the corresponding TACHA/B counter has overflowed its maximum count of 255. These faults are latched internally and must be cleared by writing to the fault register or by setting TACHA/B FLTEN low. The fault will be reasserted if the counter is still in overflow after a write to the fault register. The TACH FLT bits power-up in the low state.

The blast and timer bits become high after blasting and serial access time-out events, respectively.

A high GPIOX FLT bit reflects that the GPIOX pin has caused a fault condition; to do so, the pin must be enabled as fault producing in the GPIO setup register (GPIOX FLTEN set high) and the logic state of the pin must change after the enable. The fault is latched internally and must be cleared through software by writing to the fault register or by setting GPIOX FLTEN low; a change in the state of the GPIOX pin from its state at the point of the fault register being written will cause another fault to be signalled.

**Table 2. LTC1840 Register Address and Contents**

| Register Name | Register Address | Data Byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **(R/W)** | **R2 R1 R0** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| FAULT | 000 | TACHA FLT (0) | TACHB FLT (0) | Blast (0) | Timer (0) | GPIO4 FLT (0) | GPIO3 FLT (0) | GPIO2 FLT (0) | GPIO1 FLT (0) |
| STATUS | 001 | TACHA FLTEN (0) | TACHB FLTEN (0) | DIV1 (0) | DIV0 (0) | *See Note 2 (0/1) | (0) | (0) | (1) |
| DACA | 010 | MSB (0) | Bit 6 (0) | Bit 5 (0) | Bit 4 (0) | Bit 3 (0) | Bit 2 (0) | Bit 1 (0) | LSB (0) |
| DACB | 011 | MSB (0) | Bit 6 (0) | Bit 5 (0) | Bit 4 (0) | Bit 3 (0) | Bit 2 (0) | Bit 1 (0) | LSB (0) |
| TACHA | 100 | Cnt A7 (1) | Cnt A6 (1) | Cnt A5 (1) | Cnt A4 (1) | Cnt A3 (1) | Cnt A2 (1) | Cnt A1 (1) | Cnt A0 (1) |
| TACHB | 101 | Cnt B7 (1) | Cnt B6 (1) | Cnt B5 (1) | Cnt B4 (1) | Cnt B3 (1) | Cnt B2 (1) | Cnt B1 (1) | Cnt B0 (1) |
| GPIO Data | 110 | GPIO4 Pin (N/A) | GPIO3 Pin (N/A) | GPIO2 Pin (N/A) | GPIO1 Pin (N/A) | GPIO4 Reg (1) | GPIO3 Reg (1) | GPIO2 Reg (1) | GPIO1 Reg (1) |
| GPIO Setup | 111 | GPIO4 BLNK (0) | GPIO3 BLNK (0) | GPIO2 BLNK (0) | GPIO1 BLNK (0) | GPIO4 FLTEN (0) | GPIO3 FLTEN (0) | GPIO2 FLTEN (0) | GPIO1 FLTEN (0) |

Note 1: Number in ( )signifies default bit status upon power-up.

Note 2: State of bit depends on slave address used.

## OPERATION

DIV1 and DIV0 program the ratio by which the internal 50kHz oscillator frequency is divided down to produce the tachometer clocks (2, 4, 8, or 16). The DIV bits power-up low, which corresponds to a frequency division of 16. For example, if DIV1 and DIV0 are both high, the divide ratio is set to 2. If DIV1 is high and DIV0 is low, the divide ratio is set to 4. If DIV1 is low and DIV0 is high, the divide ratio is set to 8.

The TACHA and TACHB registers will be set to all ones by a UVLO condition. The tach counters count between rising edges on the TACHA and TACHB pins. If a counter overflows its maximum count of 255, the latch holding the count results is immediately set to 255 without waiting for the next edge on its TACH pin. This is done so that a suddenly stopped or locked rotor will be easily detectable by reading its corresponding tach register; otherwise, the register would merely hold the previous count and be waiting for a tach signal edge that isn't coming to update the overflow count.

The GPIOX pin bits in the GPIO data register reflect the logic state of the pin itself, while the GPIOX register bits reflect the data that is stored in the register that controls the gate of the internal pull-down for the pin. The logic polarities of the GPIOX bits are the same as those of the GPIOX pins assuming an appropriately sized pull-up resistor (for example, a 1 value for the GPIO1 register bit will force the internal N-channel MOSFET pull-down to an off-state, resulting in a 1 value at the GPIO1 pin). For a GPIO to be used as a digital input, the GPIOX register bit is set high, which turns off the internal pull-down N-channel MOSFET, and the state of the pin can be controlled externally and read back via the GPIOX pin bit. The GPIO register bits power-up in the high state.

The GPIOX BLNK bits in the GPIO setup register control whether the internal pull-down on a GPIO shuts on and off at about 1.5Hz when the GPIOX register bit is low, and the GPIOX FLTEN bits control whether a GPIO pin can trigger a fault condition by a change in state. The GPIO FLTEN and GPIO BLNK bits power-up in the low state.

### Serial Interface Example

In this example, an LTC1840 has both address pins open (NC) and the output current of DACA will be programmed to half of full-scale (50µA current sink).

Provide a start condition on the bus by pulling SDA from high to low while SCL is high and then write the SDA bit stream 1110010 to the part for the LTC1840 slave address, followed by a 0 to indicate that a write operation will follow. All SDA transitions must happen when SCL is low, or a start or stop condition will be interpreted. The LTC1840 will then pull the SDA line low during the next SCL clock phase to indicate that it is responding to the communication attempt. To write to the DACA output register, write 00000010 to the LTC1840 and wait for the LTC1840 to acknowledge again on the following SCL cycle by pulling SDA low. Next, send the LTC1840 the value indicating the DACA current; writing the SDA data stream 10000000 sets the DAC to sink 50µA. The LTC1840 will then acknowledge a third time by pulling SDA low for the next SCL cycle. Then the data will be written into the internal DACA register and $I_{DACOUTA}$ pin will sink 50µA. Now generate a stop condition by forcing SDA from low to high while SCL is high.

### Tachometer Interface Operation

It is common for fans to have tachometer outputs that produce two pulses per blade revolution. The LTC1840 provides two inputs that interface to circuits that count between rising edges on these pulses. The frequency at which the counting is done is programmable via the serial interface to 25kHz, 12.5kHz, 6.25kHz, and 3.125kHz, equivalent to divide by 2, 4, 8, and 16 operations on the internal 50kHz oscillator. The count values corresponding to these two inputs can also be read via the serial interface. The output registers storing these counts power-up to all ones, and they will also be loaded with all ones whenever a counter overflows between two rising edges to allow for the detection of a suddenly stopped rotor. The part can also be configured to produce a fault as soon as the counter overflows. However, the default state is to not produce such faults, so as to prevent unnecessary fault conditions while the fan is spinning up at start-up.

Multiple fans with open drain tachometer output signals can be connected to a single LTC1840 tachometer input in a wired-OR fashion, as long as the fans are not active at the same time. If the fans happen to be spinning simultaneously, the counts in the tach registers will not be meaningful.

# OPERATION

## GPIO Operation

The GPIO circuits feature N-channel MOSFET open drain pull-downs that can drive LEDs and readback circuitry to allow the logic states of the GPIO pins to be accessed through the serial interface. The circuits that read the logic states of the pins have standard CMOS thresholds. The user must take care to minimize the power dissipation in the pull-downs. LEDs should have series resistors added to limit current and to limit the voltage drop across the internal pull-down if their forward drop is less than about $V_{CC}$ minus 0.7V. The N-channel MOSFET pull-downs can sink 10mA at 0.7V drop to drive LEDs. A series resistor is usually required to limit LED current and the LTC1840 internal power dissipation. See Table 3 for resistor values.

**Table 3. Recommended LED Resistor Values**

| LED Current (mA) | Recommended Series Resistor (Ω) | |
|---|---|---|
| | $V_{CC}$ = 3V | $V_{CC}$ = 5V |
| 1 | 1k | 3k |
| 3 | 270 | 910 |
| 5 | 120 | 510 |
| 10 | 30 | 240 |

Note: LED forward voltage drop assumed to be 2V.

## $\overline{FAULT}$ Operation

Normally, the $\overline{FAULT}$ pin internal pull-down is only enabled if one of the fault bits in the fault register is high. But it is also enabled if the part is shut down by the POR block due to low $V_{CC}$ supply. This POR fault does not have a corresponding fault register bit.

## $\overline{BLAST}$ and Serial Interface Watchdog Timer Operation

The $\overline{BLAST}$ pin is used to force the DAC output currents to full value instantaneously and also to gate the operation of the serial interface watchdog timer. A blast will occur if the $\overline{BLAST}$ pin is high when the part comes out of POR or if there is a high to low transition on $\overline{BLAST}$ after POR. The threshold of the $\overline{BLAST}$ pin is about 1V, independent of $V_{CC}$. The serial interface watchdog timer, which will signal a fault condition if the part has not been addressed via the serial interface for about a minute and a half, is only active if the $\overline{BLAST}$ pin is high. If neither blasts nor an active serial interface watchdog timer are desired, this pin should be tied to ground. If timer operation is desired without having a blast occur at power-up, the pin should be pulled above 1V after the part's supply has ramped up. The blast state is cleared by writing to the fault register.

## Current Output DAC Interface to Switching Regulator

The output of a current DAC is used to control the output voltage of a switching regulator that powers a fan, which determines the rotational speed of the fan. The resistor divider from the output of the regulator to the feedback pin to ground should be ratioed to give the minimum desired voltage from the fan, which corresponds to the minimum fan speed. The size of the resistor from the output to the feedback pin is then chosen by dividing the difference between the maximum and minimum desired fan voltages by the nominal maximum current output of the DAC, which is 100µA. The value of the resistor from the feedback pin to ground is then derived from the divider ratio and the resistor value just calculated.

For example, if the feedback pin of the regulator is at 1.25V with respect to ground and the minimum desired fan voltage is 5V, the top resistor in the divider should be (5V – 1.25V)/1.25V = 3 times larger than the resistor from the feedback node to ground. If the maximum desired fan voltage is 12V, the top resistor value is then (12V – 5V)/100µA = 69.8k, and the bottom resistor is 69.8k/3 = 23.2k. See Figure 1.

If the feedback pin voltage of a regulator is lower than the 1.1V compliance voltage of either of the LTC1840's current output DACs, the resistor from the regulator output to the feedback pin can be divided into two resistors, giving the DAC more room to operate. See Figure 2.

If more than one fan is controlled by one regulator output, small differences in the actual rotational speeds of the fans may result in audible beat frequencies, which can be very annoying. To avoid this problem, the actual voltages applied to the fans can be varied by adding resistors or diodes in series with some of the fans, resulting in larger differences between their rotational speeds and less noticeable beating. See Figure 3.

## OPERATION

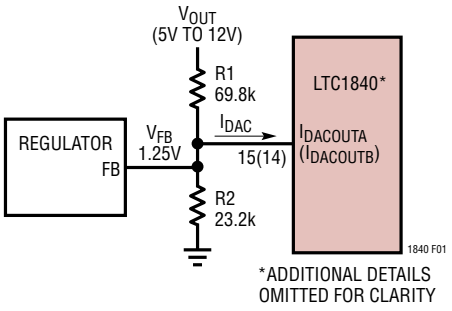



**Figure 1. Feedback Divider for 1.25V Reference**

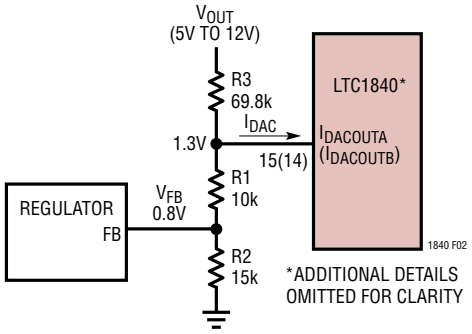
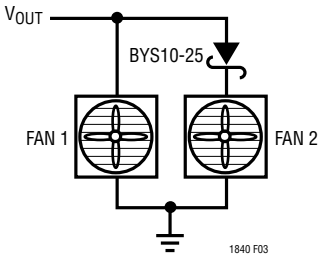



**Figure 2. Feedback Divider for 0.8V Reference**

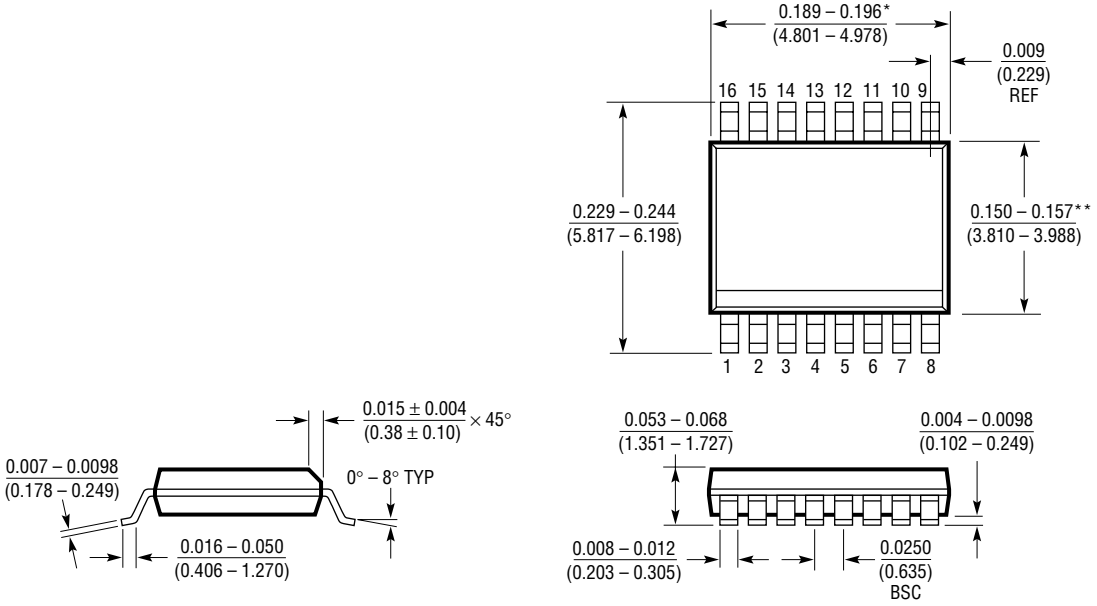



FAN 1, FAN 2: NMB 6820PL-04W-B49-D50

**Figure 3. Series Diode to Avoid Beat Frequencies**

## PACKAGE DESCRIPTION

**GN Package**
**16-Lead Plastic SSOP (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1641)



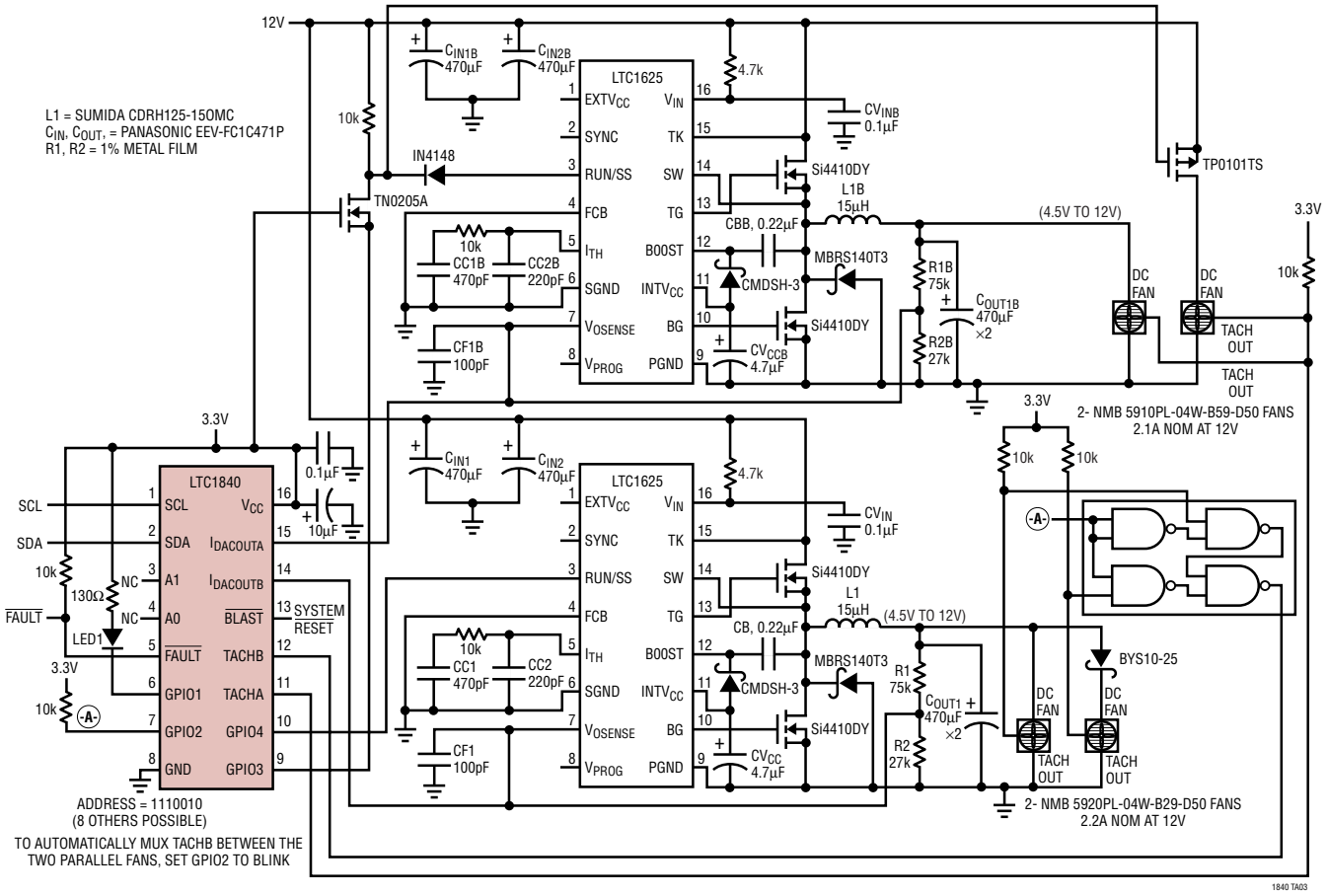

* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

# TYPICAL APPLICATION

**Controlling Fan Pair with Automatic Blast Redundancy and Fan Pair with Automatic Tach Muxing**




# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1625 | No $R_{SENSE}$™ Current Mode Synchronous Step-Down Switching Regulator | Up to 97% Efficiency; $1.19V \le V_{IN} \le 36V$; $1.19V \le V_{OUT} \le V_{IN}$; Up to 99% Duty Cycle |
| LTC1695 | SMBus/I²C Fan Speed Controller in ThinSOT™ | 0.75Ω PMOS Linear Regulator with 180mA Output Current Rating |
| LTC1694/LTC1694-1 | SMBus Accelerator | Includes DC and AC Pull-Up Current/AC Pull-Up Current Only |
| LTC1771 | Ultralow Supply Current Step-Down DC/DC Controller | 10µA Supply Current; 93% Efficiency; $1.23V \le V_{OUT} \le 18V$; $2.8V \le V_{IN} \le 20V$; Up to 100% Duty Cycle |
| LTC4300-1 | Hot Swappable 2-Wire Bus Buffer | Prevents SDA, SCL Corruption During Live Insertion; Bidirectional Bus Buffer; Isolates Backplane and Card Capacitance |

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