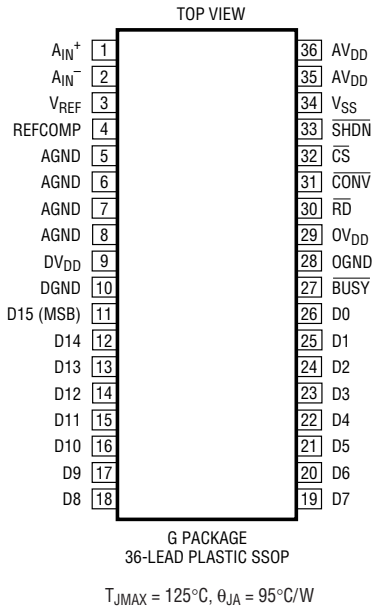
ABSOLUTE MAXIMUM RATINGS

$AV_{DD} = DV_{DD} = OV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
V_{REF} Voltage (Note 4) ..... –0.3V to (V_{DD} + 0.3V)
REFCOMP Voltage (Note 4) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) ..... –0.3V to 10V
Digital Output Voltage ..... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC1603C ..... 0°C to 70°C
LTC1603I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1603CG
LTC1603IG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	16	16		Bits
Integral Linearity Error	(Note 7)	●		±1	±3	LSB
Transition Noise	(Note 8)			0.7		LSB
Offset Error	(Note 9)	●		±0.05	±0.125	%
Offset Tempco	(Note 9)			0.5		ppm/°C
Full-Scale Error	Internal Reference External Reference			±0.125	±0.25 ±0.25	% %
Full-Scale Tempco	I_{OUT}(Reference) = 0, Internal Reference			±15		ppm/°C

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 2)	4.75 ≤ V_{DD} ≤ 5.25V, –5.25 ≤ V_{SS} ≤ –4.75V, V_{SS} ≤ (A_{IN}^-, A_{IN}^+) ≤ AV_{DD}			±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			43 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time				380		ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				–1.5		ns
t_{jitter}	Sample-and-Hold Acquisition Delay Time Jitter				5		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	–2.5V < (A_{IN}^- = A_{IN}^+) < 2.5V			68		dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/N	Signal-to-Noise Ratio	5kHz Input Signal 100kHz Input Signal	● ●	87	90 90		dB dB
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	5kHz Input Signal 100kHz Input Signal (Note 10)	 ●	 84	90 89		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	5kHz Input Signal 100kHz Input Signal	 ●		–100 –94	 –88	dB dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal			96		dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–88		dB
	Full Power Bandwidth				5		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 84dB				350		kHz

INTERNAL REFERENCE CHARACTERISTICS

(Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	2.475	2.500	2.515	V
V_{REF} Output Tempco	I_{OUT} = 0		±15		ppm/°C
V_{REF} Line Regulation	4.75 ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V		0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	0 ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA		7.5		kΩ
REFCOMP Output Voltage	I_{OUT} = 0		4.375		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_{OUT} = –10µA V_{DD} = 4.75V, I_{OUT} = –400µA	 ●	 4.0	4.5		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_{OUT} = 160µA V_{DD} = 4.75V, I_{OUT} = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D15 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D15 to D0	$\overline{CS}$ High (Note 11)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Notes 12, 13)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 12)		–4.75		–5.25	V
I_{DD}	Positive Supply Current	$\overline{CS}$ = $\overline{RD}$ = 0V	●		18	30	mA
	Nap Mode	$\overline{CS}$ = 0V, $\overline{SHDN}$ = 0V			1.5	2.4	mA
	Sleep Mode	$\overline{CS}$ = 5V, $\overline{SHDN}$ = 0V			1	100	µA
I_{SS}	Negative Supply Current	$\overline{CS}$ = $\overline{RD}$ = 0V	●		26	40	mA
	Nap Mode	$\overline{CS}$ = 0V, $\overline{SHDN}$ = 0V			1	100	µA
	Sleep Mode	$\overline{CS}$ = 5V, $\overline{SHDN}$ = 0V			1	100	µA
P_D	Power Dissipation	$\overline{CS}$ = $\overline{RD}$ = 0V	●		220	350	mW
	Nap Mode	$\overline{CS}$ = 0V, $\overline{SHDN}$ = 0V			7.5	12	mW
	Sleep Mode	$\overline{CS}$ = 5V, $\overline{SHDN}$ = 0V			0.01	1	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	250			kHz
t_{CONV}	Conversion Time		●	2.2	3.3	3.8	µs
t_{ACQ}	Acquisition Time	(Note 11)	●			480	ns
$t_{ACQ+CONV}$	Throughput Time (Acquisition + Conversion)		●			4	µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 11, 12)	●	0			ns
t_2	$\overline{CS}$↓ to $\overline{CONVST}$↓ Setup Time	(Notes 11, 12)	●	10			ns
t_3	$\overline{SHDN}$↓ to $\overline{CS}$↑ Setup Time	(Notes 11, 12)	●	10			ns
t_4	$\overline{SHDN}$↑ to $\overline{CONVST}$↓ Wake-Up Time	$\overline{CS}$ = Low (Note 12)			400		ns
t_5	$\overline{CONVST}$ Low Time	(Note 12)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			36		ns
			●			80	ns
t_7	Data Ready Before $\overline{BUSY}$↑				60		ns
			●	32			ns
t_8	Delay Between Conversions	(Note 12)	●	200			ns
t_9	Wait Time $\overline{RD}$↓ After $\overline{BUSY}$↑	(Note 12)	●	–5			ns
t_{10}	Data Access Time After $\overline{RD}$↓	C_L = 25pF			40	50	ns
			●			60	ns
		C_L = 100pF			45	60	ns
			●			75	ns
t_{11}	Bus Relinquish Time				50	60	ns
		LTC1603C	●			70	ns
		LTC1603I	●			75	ns
t_{12}	$\overline{RD}$ Low Time	(Note 12)	●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time	(Note 12)	●	40			ns
t_{14}	Aperture Delay of Sample-and-Hold				2		ns

TIMING CHARACTERISTICS (Note 5)

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, OGND and AGND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = –5V, f_{SMPL} = 250kHz, and $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specification apply for a single-ended A_{IN}^+ input with A_{IN}^- grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Typical RMS noise at the code transitions. See Figure 17 for histogram.

Note 9: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111.

Note 10: Signal-to-Noise Ratio (SNR) is measured at 5kHz and distortion is measured at 100kHz. These results are used to calculate Signal-to-Nosie Plus Distortion (SINAD).

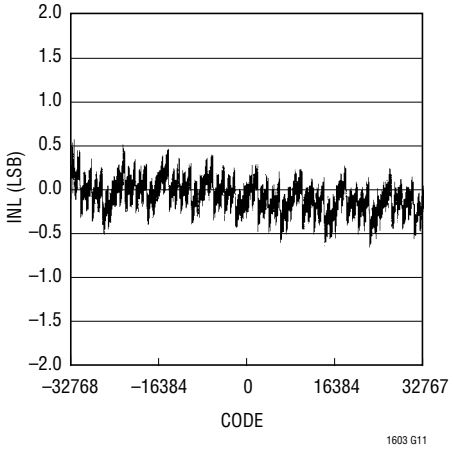
Note 11: Guaranteed by design, not subject to test.

Note 12: Recommended operating conditions.

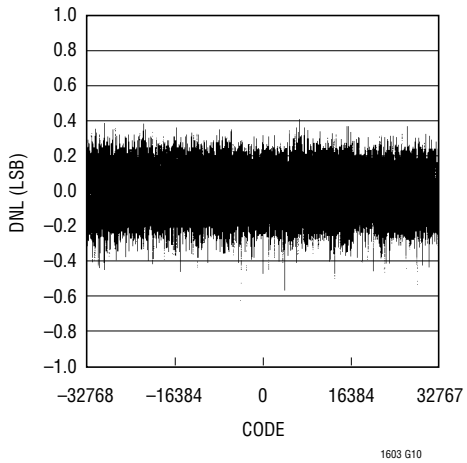
Note 13: The falling $\overline{\text{CONVST}}$ edge starts a conversion. If $\overline{\text{CONVST}}$ returns high at a critical point during the conversion it can create small errors. For best performance ensure that $\overline{\text{CONVST}}$ returns high either within 250ns after conversion start or after $\overline{\text{BUSY}}$ rises.

TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity vs Output Code



Differential Nonlinearity vs Output Code



PIN FUNCTIONS

A_{IN}^+ (Pin 1): Positive Analog Input. The ADC converts the difference voltage between A_{IN}^+ and A_{IN}^- with a differential range of ±2.5V. A_{IN}^+ has a ±2.5V input range when A_{IN}^- is grounded.

A_{IN}^- (Pin 2): Negative Analog Input. Can be grounded, tied to a DC voltage or driven differentially with A_{IN}^+.

V_{REF} (Pin 3): 2.5V Reference Output. Bypass to AGND with 2.2µF tantalum in parallel with 0.1µF ceramic.

REFCOMP (Pin 4): 4.375V Reference Compensation Pin. Bypass to AGND with 47µF tantalum in parallel with 0.1µF ceramic.

AGND (Pins 5 to 8): Analog Grounds. Tie to analog ground plane.

DV_{DD} (Pin 9): 5V Digital Power Supply. Bypass to DGND with 10µF tantalum in parallel with 0.1µF ceramic.

DGND (Pin 10): Digital Ground for Internal Logic. Tie to analog ground plane.

D15 to D0 (Pins 11 to 26): Three-State Data Outputs. D15 is the Most Significant Bit.

$\overline{BUSY}$ (Pin 27): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress. Data is valid on the rising edge of $\overline{BUSY}$.

OGND (Pin 28): Digital Ground for Output Drivers.

OV_{DD} (Pin 29): Digital Power Supply for Output Drivers. Bypass to OGND with 10µF tantalum in parallel with 0.1µF ceramic.

$\overline{RD}$ (Pin 30): Read Input. A logic low enables the output drivers when $\overline{CS}$ is low.

$\overline{CONVST}$ (Pin 31): Conversion Start Signal. This active low signal starts a conversion on its falling edge when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 32): The Chip Select Input. Must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

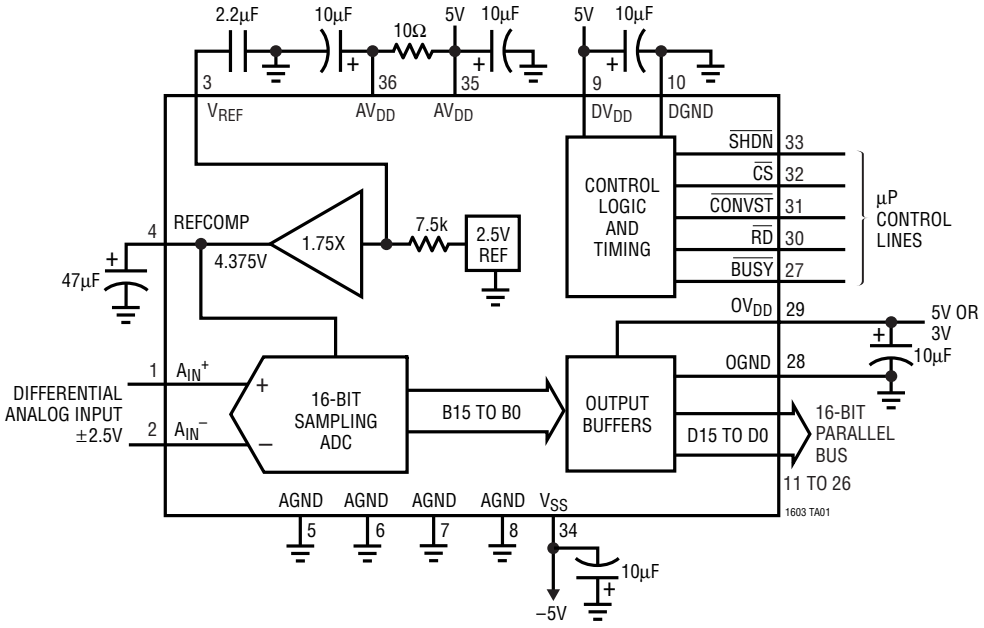
$\overline{SHDN}$ (Pin 33): Power Shutdown. Drive this pin low with $\overline{CS}$ low for nap mode. Drive this pin low with $\overline{CS}$ high for sleep mode.

V_{SS} (Pin 34): –5V Negative Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

AV_{DD} (Pin 35): 5V Analog Power Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

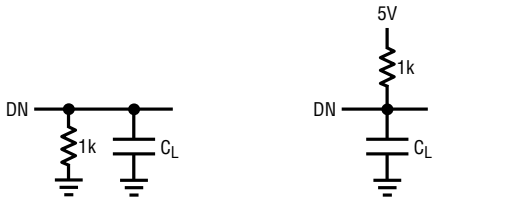
AV_{DD} (Pin 36): 5V Analog Power Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic and connect this pin to Pin 35 with a 10Ω resistor.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

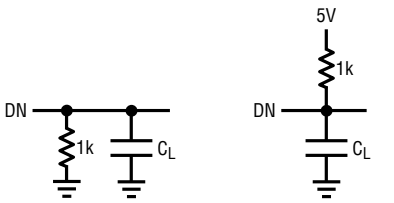
Load Circuits for Access Timing



(A) Hi-Z TO V_{OH} AND V_{OL} TO V_{OH} (B) Hi-Z TO V_{OL} AND V_{OH} TO V_{OL}

1603 TC01

Load Circuits for Output Float Delay



(A) V_{OH} TO Hi-Z (B) V_{OL} TO Hi-Z

1603 TC02

APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1603 uses a successive approximation algorithm and internal sample-and-hold circuit to convert an analog signal to a 16-bit parallel output. The ADC is complete with a sample-and-hold, a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion the successive approximation register (SAR) resets. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal differential 16-bit capacitive DAC output is sequenced by the SAR from the Most Significant Bit (MSB) to the Least Significant Bit (LSB). Referring to Figure 1, the A_{IN}^+ and A_{IN}^- inputs are acquired during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a duration of 480ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches connect the C_{SMPL} capacitors to ground, transferring the differential analog input charge onto the summing junctions. This input charge is successively compared with the binary-weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the A_{IN}^+ and A_{IN}^- input charges. The SAR contents (a 16-bit data word) which represent the difference of A_{IN}^+ and A_{IN}^- are loaded into the 16-bit output latches.

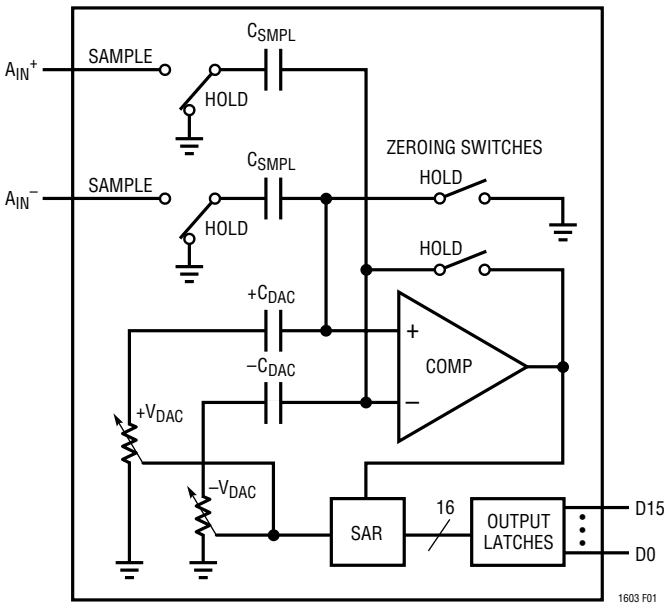


Figure 1. Simplified Block Diagram

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that runs the A/D conversion. The internal clock is factory trimmed to achieve a typical conversion time of 3.3µs and a maximum conversion time of 3.8µs over the full temperature range. No external adjustments are required. The guaranteed maximum acquisition time is 480ns. In addition, a throughput time (acquisition + conversion) of 4µs and a minimum sampling rate of 250ksps are guaranteed.

3V Input/Output Compatible

The LTC1603 operates on ±5V supplies, which makes the device easy to interface to 5V digital systems. This device can also talk to 3V digital systems: the digital input pins ($\overline{SHDN}$, $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$) of the LTC1603 recognize 3V or 5V inputs. The LTC1603 has a dedicated output supply pin (OV_{DD}) that controls the output swings of the digital output pins (D0 to D15, $\overline{BUSY}$) and allows the part to talk to either 3V or 5V digital systems. The output is two's complement binary.

Power Shutdown

The LTC1603 provides two power shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from Nap to active is 200ns. In Sleep mode all bias

APPLICATIONS INFORMATION

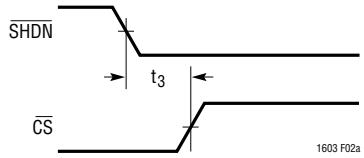


Figure 2a. Nap Mode to Sleep Mode Timing

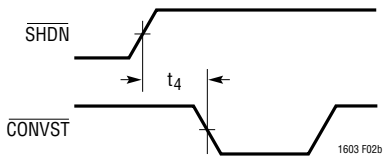


Figure 2b. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

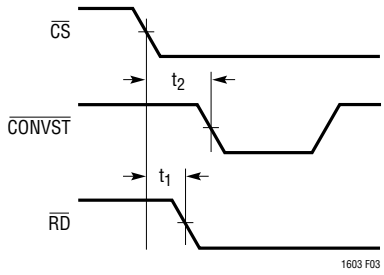


Figure 3. $\overline{CS}$ to $\overline{CONVST}$ Setup Timing

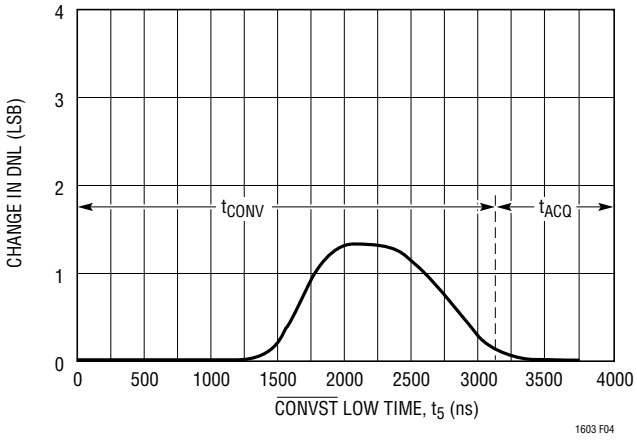


Figure 4. Change in DNL vs $\overline{CONVST}$ Low Time. Be Sure the $\overline{CONVST}$ Pulse Returns High Early in the Conversion or After the End of Conversion

currents are shut down and only leakage current remains (about 1μA). Wake-up time from Sleep mode is much slower since the reference circuit must power up and settle. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 160ms with the recommended 47μF capacitor.

Shutdown is controlled by Pin 33 ($\overline{SHDN}$). The ADC is in shutdown when $\overline{SHDN}$ is low. The shutdown mode is selected with Pin 32 ($\overline{CS}$). When $\overline{SHDN}$ is low, $\overline{CS}$ low selects nap and $\overline{CS}$ high selects sleep.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CONVST}$, $\overline{CS}$ and $\overline{RD}$. A falling edge applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

We recommend using a narrow logic low or narrow logic high $\overline{CONVST}$ pulse to start a conversion as shown in Figures 5 and 6. A narrow low or high $\overline{CONVST}$ pulse prevents the rising edge of the $\overline{CONVST}$ pulse from upsetting the critical bit decisions during the conversion time. Figure 4 shows the change of the differential nonlinearity error versus the low time of the $\overline{CONVST}$ pulse. As shown, if $\overline{CONVST}$ returns high early in the conversion (e.g., $\overline{CONVST}$ low time <500ns), accuracy is unaffected. Similarly, if $\overline{CONVST}$ returns high after the conversion is over (e.g., $\overline{CONVST}$ low time >t_{CONV}), accuracy is unaffected. For best results, keep t_5 less than 500ns or greater than t_{CONV}.

Figures 5 through 9 show several different modes of operation. In modes 1a and 1b (Figures 5 and 6), $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 7) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal starts the conversion. Data outputs are in

APPLICATIONS INFORMATION

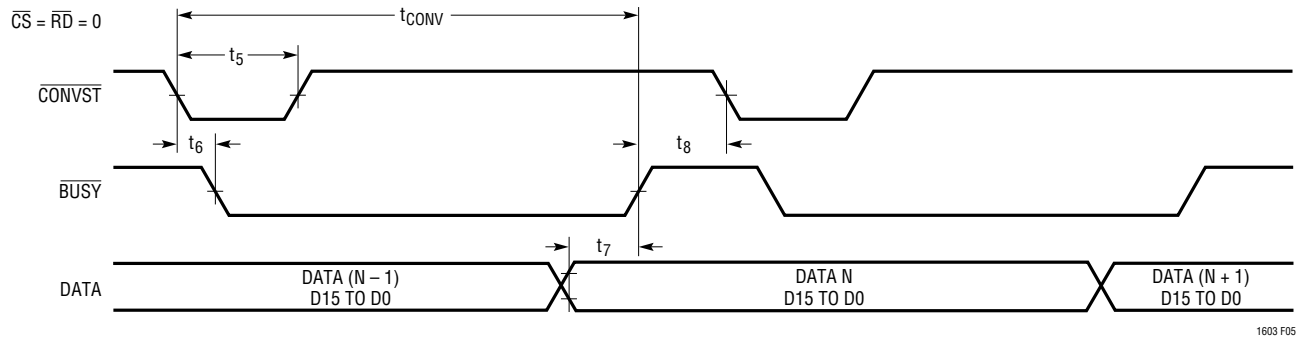


Figure 5. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⊓⊓⊓)

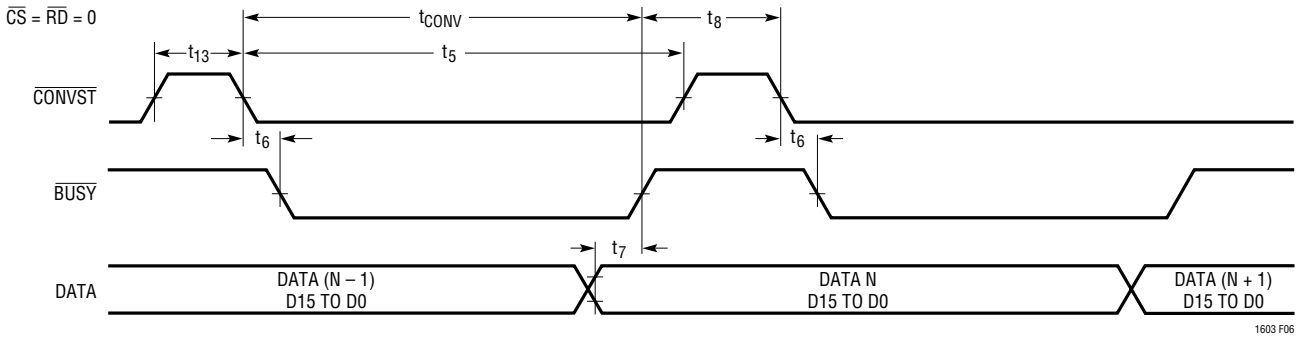


Figure 6. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⊓_⊓_⊓)

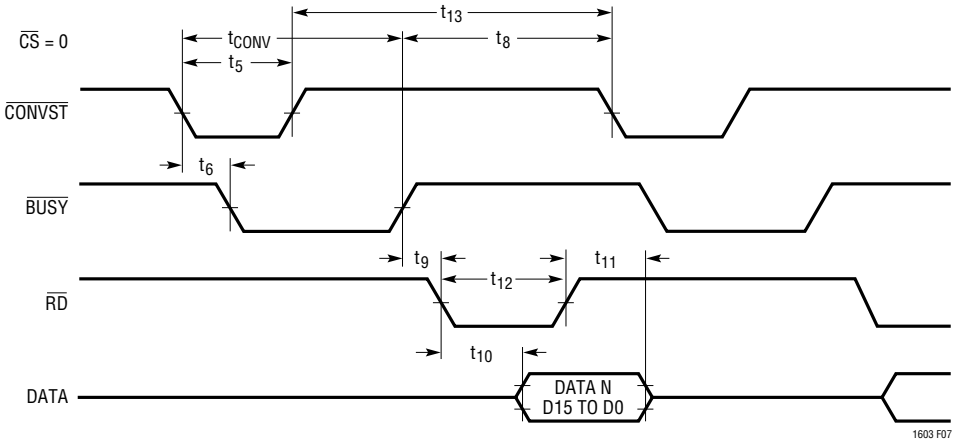


Figure 7. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

APPLICATIONS INFORMATION

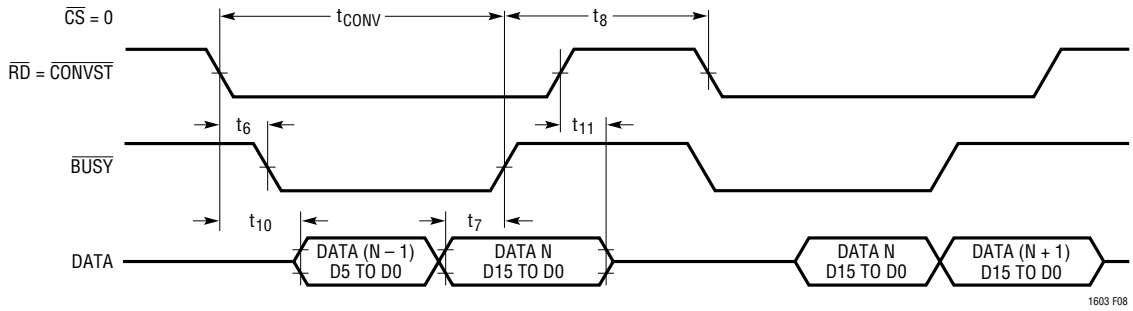


Figure 8. Mode 2. Slow Memory Mode Timing

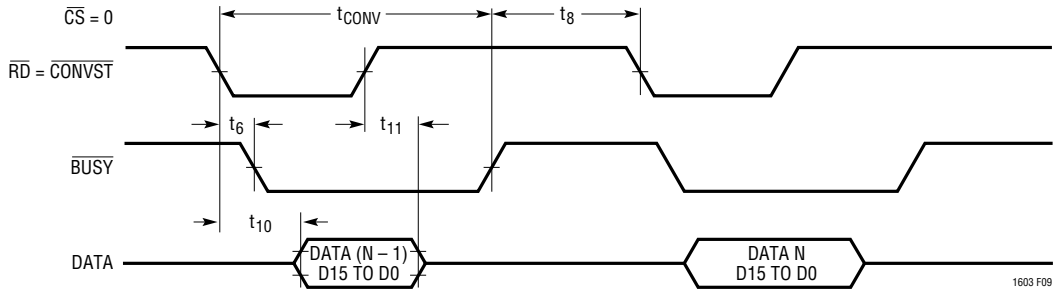


Figure 9. ROM Mode Timing

three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared data bus.

In slow memory and ROM modes (Figures 8 and 9) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the combined $\overline{CONVST}$-$\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock is needed).

In slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high, releasing the processor and the processor takes $\overline{RD}$ (= $\overline{CONVST}$) back high and reads the new conversion data.

In ROM mode, the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

DIFFERENTIAL ANALOG INPUTS

Driving the Analog Inputs

The differential analog inputs of the LTC1603 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is grounded). The A_{IN}^+ and A_{IN}^- inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1603 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 10). For minimum acquisition time with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion

APPLICATIONS INFORMATION

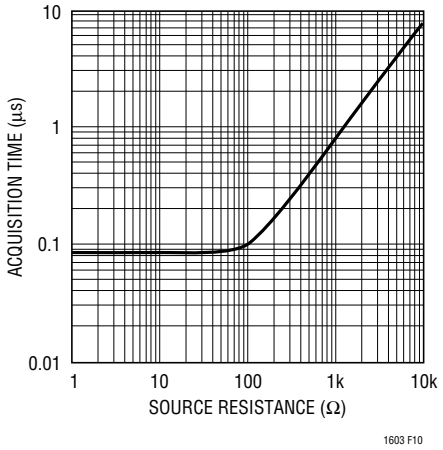


Figure 10. t_{ACQ} vs Source Resistance

starts (settling time must be 200ns for full throughput rate).

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of +1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz should be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 15MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1603 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1603. More detailed information is available in the Linear Technology databooks, the LinearView™ CD-ROM and on our web site at: www.linear-tech. com.

LT®1007: Low Noise Precision Amplifier. 2.7mA supply current, ±5V to ±15V supplies, gain bandwidth product 8MHz, DC applications.

LT1097: Low Cost, Low Power Precision Amplifier. 300µA supply current, ±5V to ±15V supplies, gain bandwidth product 0.7MHz, DC applications.

LT1227: 140MHz Video Current Feedback Amplifier. 10mA supply current, ±5V to ±15V supplies, low noise and low distortion.

LT1360: 37MHz Voltage Feedback Amplifier. 3.8mA supply current, ±5V to ±15V supplies, good AC/DC specs.

LT1363: 50MHz Voltage Feedback Amplifier. 6.3mA supply current, good AC/DC specs.

LT1364/LT1365: Dual and Quad 50MHz Voltage Feedback Amplifiers. 6.3mA supply current per amplifier, good AC/DC specs.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1603 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 15MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 11 shows a 3000pF capacitor from A_{IN}^+ to ground and a 100Ω source resistor to limit the input bandwidth to 530kHz. The 3000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

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APPLICATIONS INFORMATION

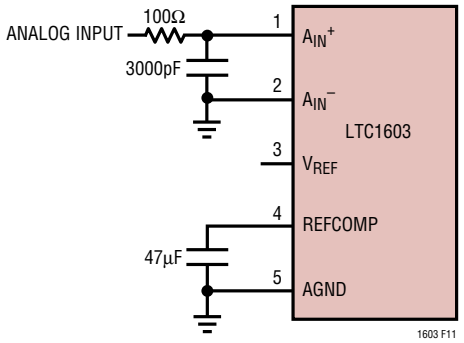


Figure 11. RC Input Filter

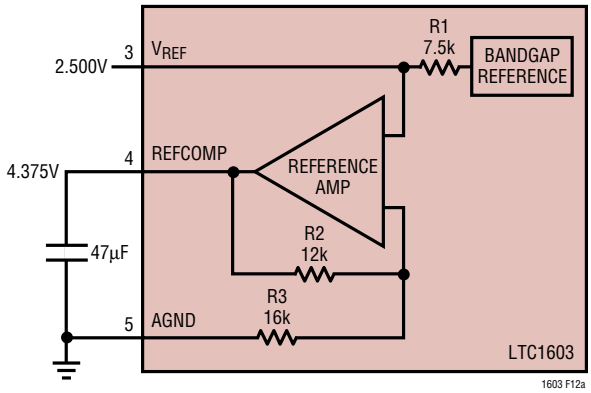


Figure 12a. LTC1603 Reference Circuit

Input Range

The ±2.5V input range of the LTC1603 is optimized for low noise and low distortion. Most op amps also perform well over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1603 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

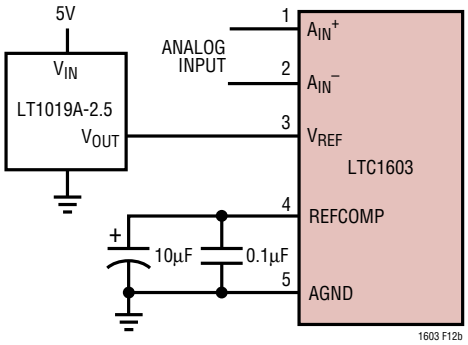


Figure 12b. Using the LT1019-2.5 as an External Reference

Internal Reference

The LTC1603 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3) (see Figure 12a). A 7.5k resistor is in series with the output so that it can be easily overdriven by an external reference or other circuitry (see Figure 12b). The reference amplifier gains the voltage at the V_{REF} pin by 1.75 to create the required internal reference voltage. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The reference amplifier compensation pin (REFCOMP, Pin 4) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 22µF or greater. For the best noise performance a 47µF ceramic or 47µF tantalum in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with a DAC or other means shown in Figure 13. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1603 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 20ms should be allowed for after a reference adjustment.

Differential Inputs

The LTC1603 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $A_{IN}^+ - A_{IN}^-$ independent of the common mode voltage (see Figure 15a). The common mode rejection holds up to extremely high frequencies (see Figure 14a). The only requirement is that both inputs

APPLICATIONS INFORMATION

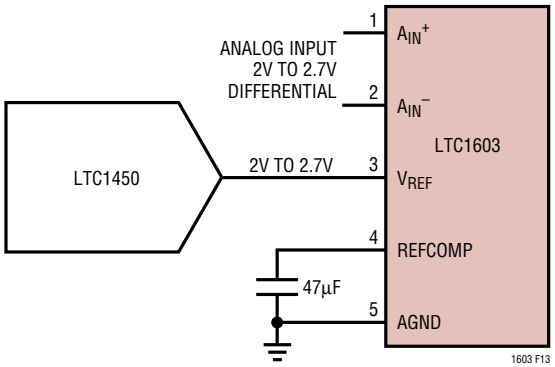


Figure 13. Driving V_{REF} with a DAC

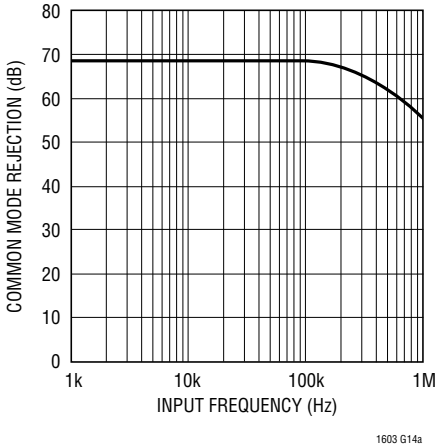


Figure 14a. CMRR vs Input Frequency

can not exceed the AV_{DD} or V_{SS} power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Dynamic performance is also affected by the common mode voltage. THD will degrade as the inputs approach either power supply rail, from 96dB with a common mode of 0V to 86dB with a common mode of 2.5V or –2.5V.

Differential inputs allow greater flexibility for accepting different input ranges. Figure 14b shows a circuit that converts a 0V to 5V analog input signal with only an additional buffer that is not in the signal path.

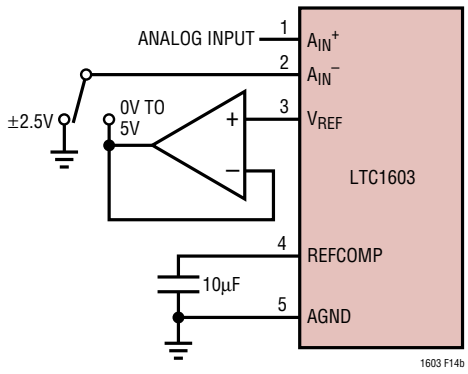


Figure 14b. Selectable 0V to 5V or ±2.5V Input Range

Full-Scale and Offset Adjustment

Figure 15a shows the ideal input/output characteristics for the LTC1603. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB,... FS – 1.5LSB, FS – 0.5LSB). The output is two's complement binary with 1LSB = FS – (–FS)/65536 = 5V/65536 = 76.3µV.

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 15b shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply

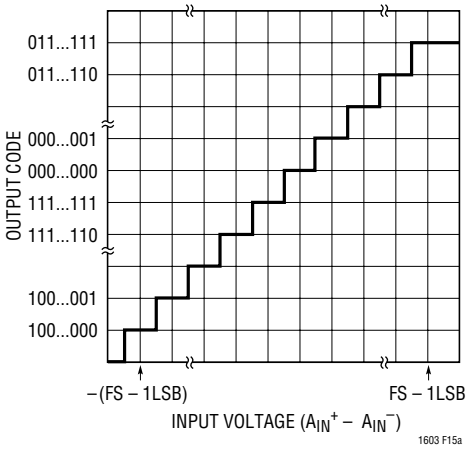


Figure 15a. LTC1603 Transfer Characteristics

APPLICATIONS INFORMATION

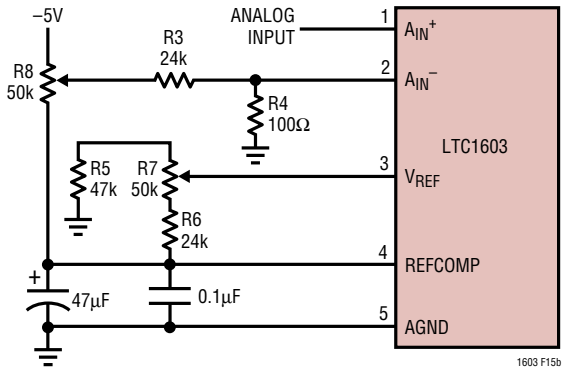


Figure 15b. Offset and Full-Scale Adjust Circuit

–38µV (i.e., –0.5LSB) at A_{IN}^+ and adjust the offset at the A_{IN}^- input by varying R8 until the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. For full-scale adjustment, an input voltage of 2.499886V (FS/2 – 1.5LSBs) is applied to A_{IN}^+ and R7 is adjusted until the output code flickers between 0111 1111 1111 1110 and 0111 1111 1111 1111.

BOARD LAYOUT AND GROUNDING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1603, a printed circuit board with ground plane is required. Layout should ensure that digital and analog signal lines are separated as much as possible. Particular care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.The analog input should be screened by AGND.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 to Pin 8 (AGNDs), Pin 10 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the DV_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1603 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- leads will be rejected by the input CMRR. The A_{IN}^- input can be used as a ground sense for the A_{IN}^+ input; the LTC1603 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 1) and A_{IN}^- (Pin 2) should be kept as short as possible. In applications where this is not possible, the A_{IN}^+ and A_{IN}^- traces should be run side by side to equalize coupling.

SUPPLY BYPASSING

High quality, low series resistance ceramic, 10µF or 47µF bypass capacitors should be used at the V_{DD} and REFCOMP pins as shown in Figure 16 and in the Typical Application on the first page of this data sheet. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively, 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

APPLICATIONS INFORMATION

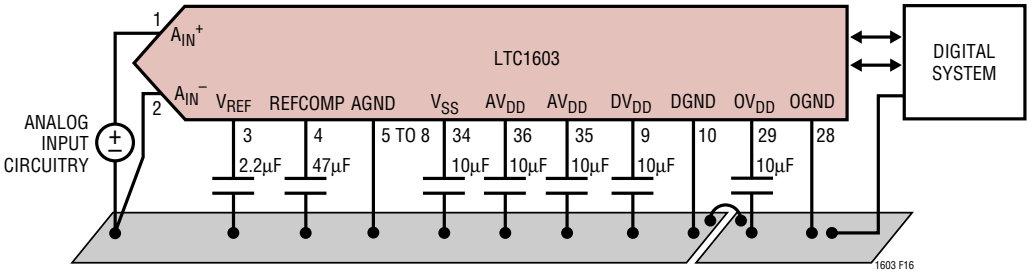


Figure 16. Power Supply Grounding Practice

DC PERFORMANCE

The noise of an ADC can be evaluated in two ways: signal-to-noise raio (SNR) in frequency domain and histogram in time domain. The LTC1603 excels in both. Figure 18a demonstrates that the LTC1603 has an SNR of over 90dB in frequency domain. The noise in the time domain histogram is the transition noise associated with a high resolution ADC which can be measured with a fixed DC signal applied to the input of the ADC. The resulting output codes are collected over a large number of conversions. The shape of the distribution of codes will give an indication of the magnitude of the transition noise. In Figure 17 the distribution of output codes is shown for a DC input that has been digitized 4096 times. The distribution is Gaussian and the RMS code transition noise is about 0.66LSB. This corresponds to a noise level of 90.9dB relative to full scale. Adding to that the theoretical 98dB of quantization error for 16-bit ADC, the resultant corresponds to an SNR level of 90.1dB which correlates very well to the frequency domain measurements in DYNAMIC PERFORMANCE section.

DYNAMIC PERFORMANCE

The LTC1603 has excellent high speed sampling capability. Fast fourier transform (FFT) test techniques are used to test the ADC's frequency response, distortions and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figures 18a and 18b show typical LTC1603 FFT plots.

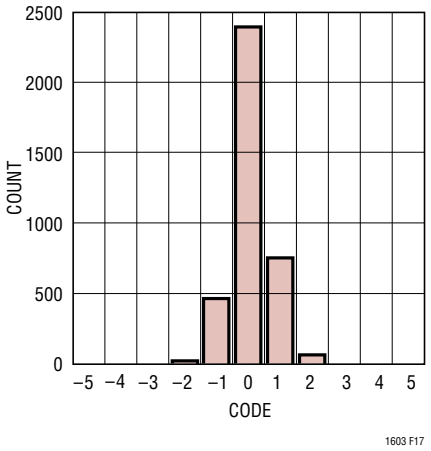


Figure 17. Histogram for 4096 Conversions

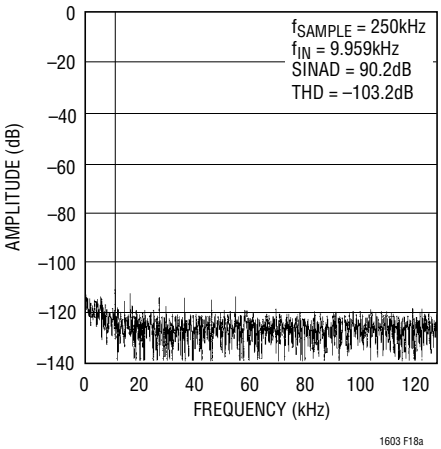


Figure 18a. This FFT of the LTC1603's Conversion of a Full-Scale 10kHz Sine Wave Shows Outstanding Response with a Very Low Noise Floor When Sampling at 250ksps

APPLICATIONS INFORMATION

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 18a shows a typical spectral content with a 250kHz sampling rate and a 5kHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist limit of 125kHz.

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 250kHz the LTC1603 maintains above 14 bits up to the Nyquist input frequency of 125kHz (refer to Figure 19).

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\frac{\sqrt{V2^2 + V3^2 + V4^2 + ...Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. THD vs Input Frequency is shown in Figure 20. The LTC1603 has good distortion performance up to the Nyquist frequency and beyond.

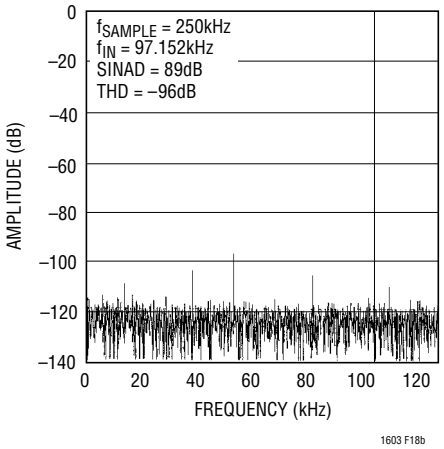


Figure 18b. Even with Inputs at 100kHz, the LTC1603's Dynamic Linearity Remains Robust

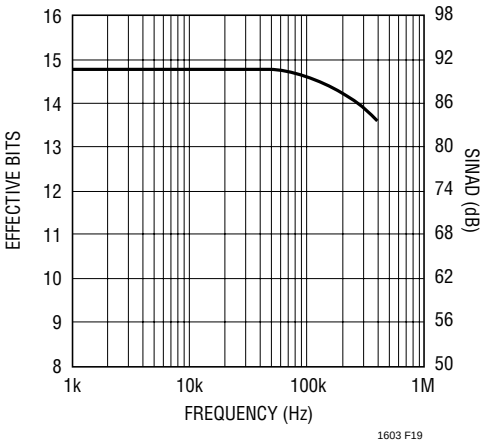


Figure 19. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

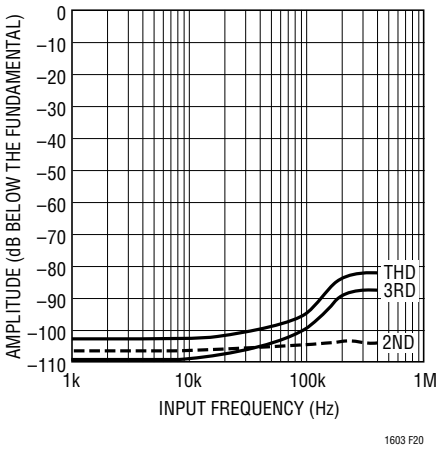


Figure 20. Distortion vs Input Frequency

APPLICATIONS INFORMATION

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ±nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa – fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(fa \pm fb\right) = 20Log\frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

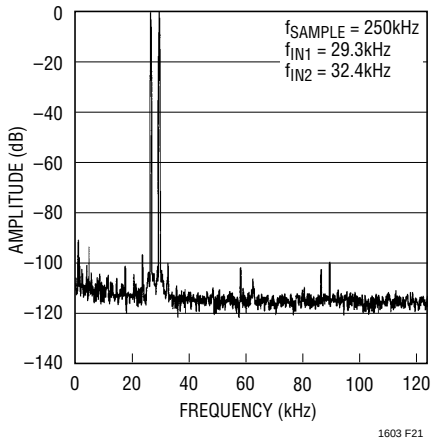


Figure 21. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

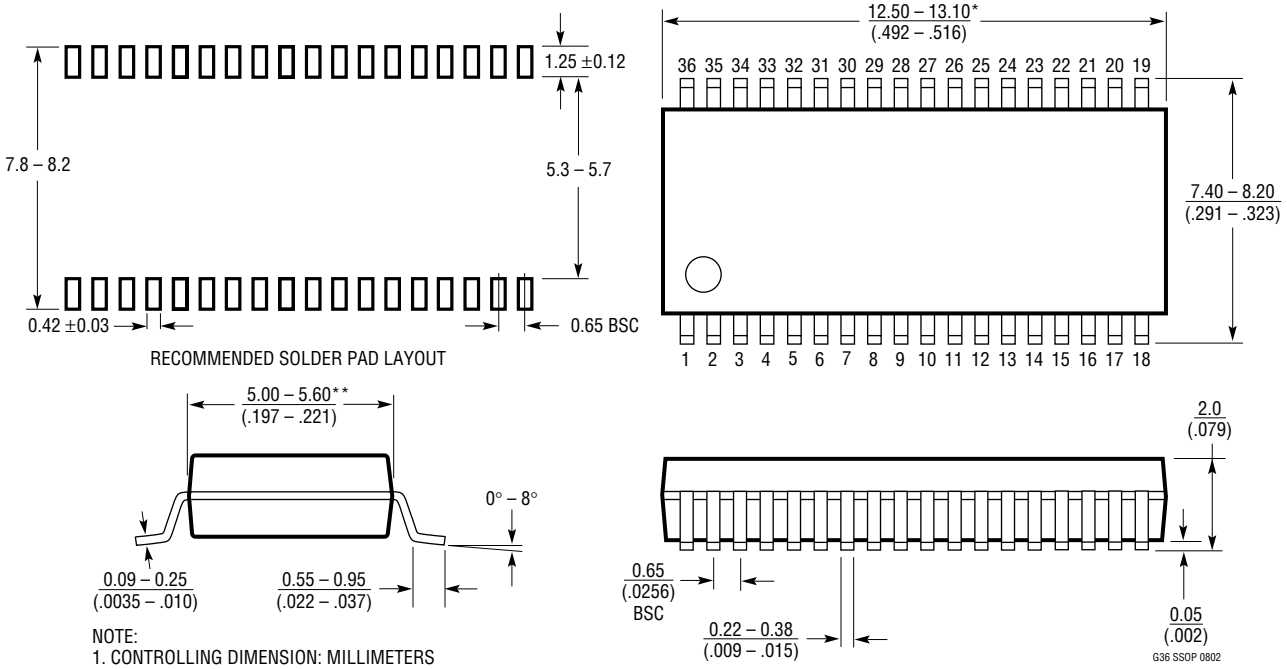
Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 84dB (13.66 effective bits). The LTC1603 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

PACKAGE DESCRIPTION

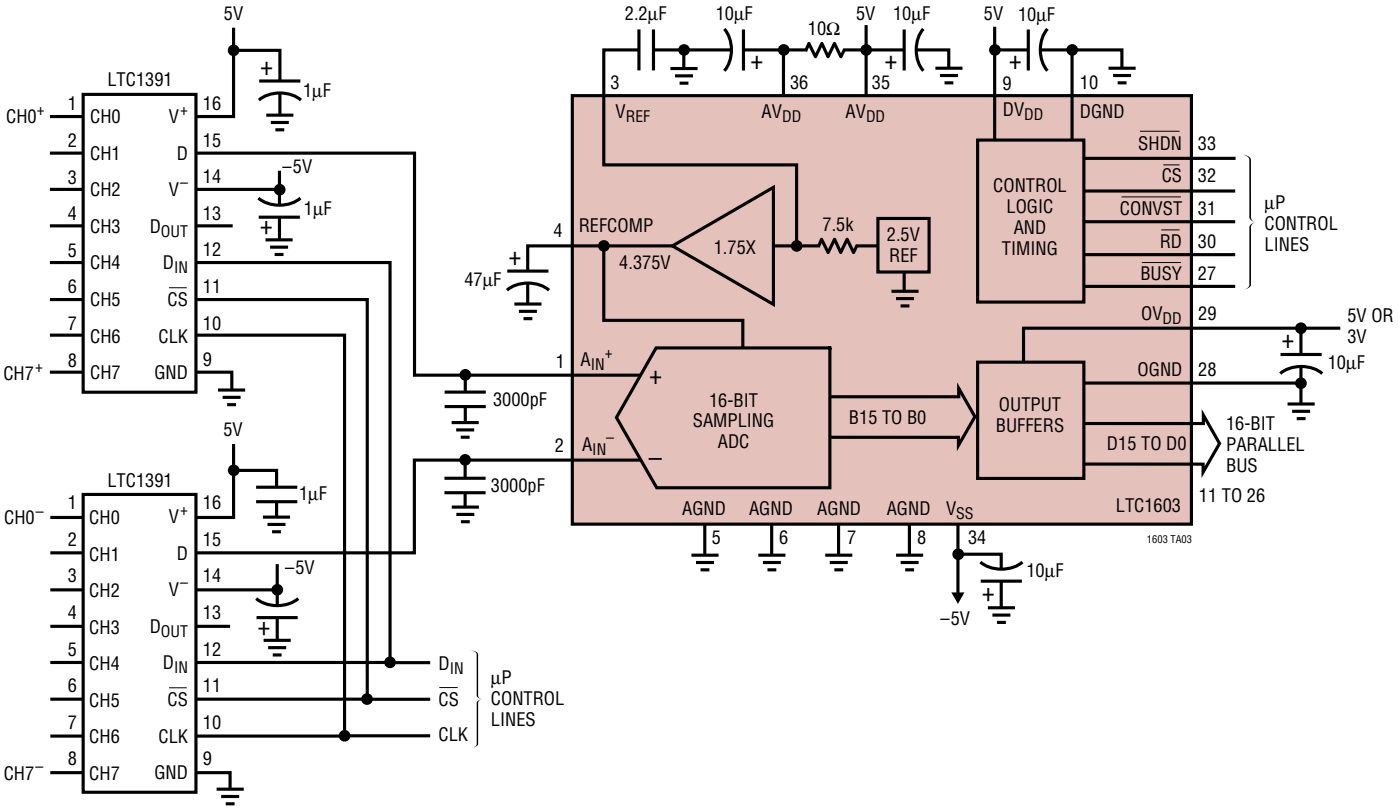
G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

Using the LTC1603 and Two LTC1391s as an 8-Channel Differential 16-Bit ADC System



RELATED PARTS

SAMPLING ADCs

PART NUMBER	DESCRIPTION	COMMENTS
LTC1410	12-Bit, 1.25Msps, ±5V ADC	71.5dB SINAD at Nyquist, 150mW Dissipation
LTC1415	12-Bit, 1.25Msps, Single 5V ADC	55mW Power Dissipation, 72dB SINAD
LTC1418	14-Bit, 200ksps, Single 5V ADC	15mW, Serial/Para llel ±10V
LTC1419	Low Power 14-Bit, 800ksps ADC	True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipation
LTC1604	16-Bit, 333ksps, ±5V ADC	Pin Compatible with LTC1603
LTC1605	16-Bit, 100ksps, Single 5V ADC	±10V Inputs, 55mW, Byte or Parallel I/O
LTC1608	16-Bit, 500ksps, ±5V ADC	Pin Compatible with LTC1603

DACs

PART NUMBER	DESCRIPTION	COMMENTS
LTC1592	16-Bit Serial SoftSpan™ DAC	±1LSB Max INL/DNL, Software-Selectable Output Spans
LTC1595	16-Bit Serial Multiplying I_{OUT} DAC in SO-8	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1596	16-Bit Serial Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, AD7543/DAC8143 16-Bit Upgrade
LTC1597	16-Bit Parallel, Multiplying DAC	±1LSB Max INL/DNL, Low Glitch, 4 Quadrant Resistors
LTC1650	16-Bit Serial V_{OUT} DAC	Low Power, Low Gritch, 4-Quadrant Multiplication

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