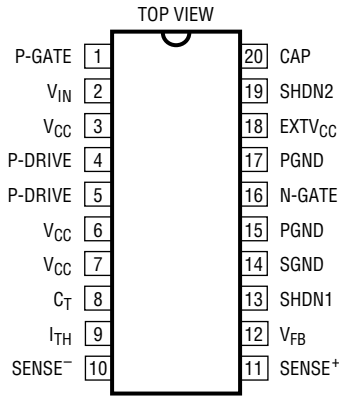
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (Pin 2) ..... –15V to 60V
V_{CC} Output Current (Pin 3) 50mA
Continuous Pin Currents (Any Pin) 50mA
Sense Voltages ..... –0.3V to 13V
Shutdown Voltages 7V
$EXTV_{CC}$ Input Voltage 15V
Junction Temperature (Note 2) ..... 125°C

Operating Temperature Range
LTC1159C ..... 0°C to 70°C
LTC1159I ..... –40°C to 85°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

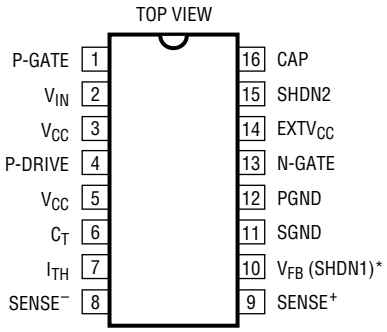


G PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER PART NUMBER

LTC1159CG
LTC1159CG-3.3
LTC1159CG-5



N PACKAGE
16-LEAD PDIP

S PACKAGE
16-LEAD PLASTIC SO

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 80°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LTC1159CN
LTC1159CN-3.3
LTC1159CN-5
LTC1159CS
LTC1159CS-3.3
LTC1159CS-5
LTC1159IS
LTC1159IS-3.3
LTC1159IS-5

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{SHDN1} = 0V (Note 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage (LTC1159 Only)		●	1.21	1.25	1.29	V
I_{FB}	Feedback Current (LTC1159 Only)		●		0.2		µA
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	LTC1159-3.3	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	LTC1159-5	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 40V		–40	0	40	mV
	Output Voltage Load Regulation						
	LTC1159-3.3	5mA < I_{LOAD} < 2A	●		40	65	mV
	LTC1159-5	5mA < I_{LOAD} < 2A	●		60	100	mV
	Burst Mode Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_{IN}	V_{IN} Pin Current (Note 4)						
	Normal Mode	V_{IN} = 12V, $EXTV_{CC}$ = 5V			200		µA
		V_{IN} = 40V, $EXTV_{CC}$ = 5V			300		µA
	Shutdown	V_{IN} = 12V, V_{SHDN2} = 2V			15		µA
		V_{IN} = 40V, V_{SHDN2} = 2V			25		µA
I_{EXTVCC}	$EXTV_{CC}$ Pin Current (Note 4)	$EXTV_{CC}$ = 5V, Sleep Mode			250		µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{SHDN1} = 0V (Note 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, $EXTV_{CC}$ = 0V, I_{CC} = 10mA	●	4.25	4.5	4.75	V
$V_{IN} - V_{CC}$	V_{CC} Dropout Voltage	V_{IN} = 4V, $EXTV_{CC}$ = Open, I_{CC} = 10mA			300	400	mV
$V_{EXT} - V_{CC}$	$EXTV_{CC}$ Switch Drop	V_{IN} = 12V, $EXTV_{CC}$ = 5V, I_{SWITCH} = 10mA			250	350	mV
$V_{P-GATE} - V_{IN}$	P-Gate to Source Voltage (Off)	V_{IN} = 12V V_{IN} = 40V		−0.2 −0.2	0 0		V V
$V_{SENSE}^+ - V_{SENSE}^-$	Current Sense Threshold Voltage LTC1159	 V_{SENSE}^- = 5V, V_{FB} = 1.32V (Forced) V_{SENSE}^- = 5V, V_{FB} = 1.15V (Forced)	 ●	 130	 25 150	 170	 mV mV
	LTC1159-3.3	V_{SENSE}^- = 3.4V (Forced) V_{SENSE}^- = 3.1V (Forced)	 ●	 130	 25 150	 170	 mV mV
	LTC1159-5	V_{SENSE}^- = 5.2V (Forced) V_{SENSE}^- = 4.7V (Forced)	 ●	 130	 25 150	 170	 mV mV
V_{SNDN1}	SHDN1 Threshold LTC1159CG, LTC1159-3.3, LTC1159-5			0.5	0.8	2	V
V_{SHDN2}	SHDN2 Threshold			0.8	1.4	2	V
I_{SHDN2}	Shutdown 2 Input Current	V_{SHDN2} = 5V			12	20	µA
I_{CT}	C_T Pin Discharge Current	V_{OUT} in Regulation V_{OUT} = 0V		50	70 2	90 10	µA µA
t_{OFF}	Off-Time (Note 5)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins P-Drive and N-Gate), V_{IN} = 6V			100	200	ns

−40°C ≤ T_A ≤ 85°C (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage (LTC1159 Only)		1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage LTC1159-3.3 LTC1159-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA	 3.17 4.85	 3.30 5.05	 3.43 5.25	 V V
I_{IN}	V_{IN} Pin Current (Note 4) Normal	 V_{IN} = 12V, $EXTV_{CC}$ = 5V V_{IN} = 40V, $EXTV_{CC}$ = 5V		 200 300		 µA µA
	Shutdown	V_{IN} = 12V, V_{SHDN2} = 2V V_{IN} = 40V, V_{SHDN2} = 2V		15 25		µA µA
I_{EXTVCC}	$EXTV_{CC}$ Pin Current (Note 4)	$EXTV_{CC}$ = 5V, Sleep Mode		250		µA
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, $EXTV_{CC}$ = 0V, I_{CC} = 10mA		4.5		V
$V_{SENSE}^+ - V_{SENSE}^-$	Current Sense Threshold Voltage	Low Threshold (Forced) High Threshold (Forced)		25 150	 175	mV mV
V_{SHDN2}	SHDN2 Threshold		0.8	1.4	2	V
t_{OFF}	Off-Time (Note 5)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V	3.5	5	6.5	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1159CG, LTC1159CG-3.3, LTC1159CG-5: $T_J = T_A + (P_D \bullet 135°C/W)$
LTC1159CN, LTC1159CN-3.3, LTC1159CN-5: $T_J = T_A + (P_D \bullet 80°C/W)$
LTC1159CS, LTC1159CS-3.3, LTC1159CS-5: $T_J = T_A + (P_D \bullet 110°C/W)$

Note 3: On LTC1159 versions which have a SHDN1 pin, it must be at ground potential for testing.

Note 4: The LTC1159 V_{IN} and $EXTV_{CC}$ current measurements exclude MOSFET driver currents. When V_{CC} power is derived from the output via $EXTV_{CC}$, the input current increases by ($I_{GATECHG}$ • Duty Cycle)/(Efficiency). See Typical Performance Characteristics and Applications Information.

Note 5: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

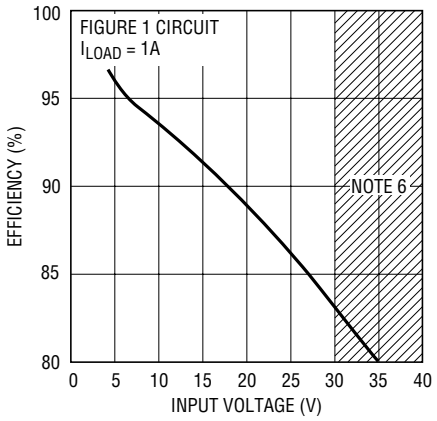
ELECTRICAL CHARACTERISTICS

Note 6: The LTC1159C, LTC1159C-3.3, and LTC1159C-5 are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation. The LTC1159I, LTC1159I-3.3 and LTC1159I-5 are guaranteed and tested over the –40°C to 85°C operating temperature range.

Note 7: The logic-level power MOSFETs shown in Figure 1 are rated for $V_{DS(MAX)}$ = 30V. For operation at V_{IN} > 30V, use standard threshold MOSFETs with $EXTV_{CC}$ powered from a 12V supply. See Applications Information.

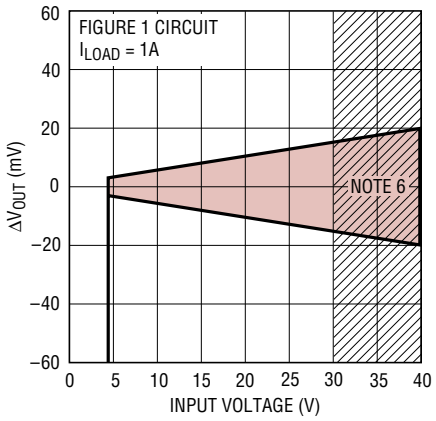
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



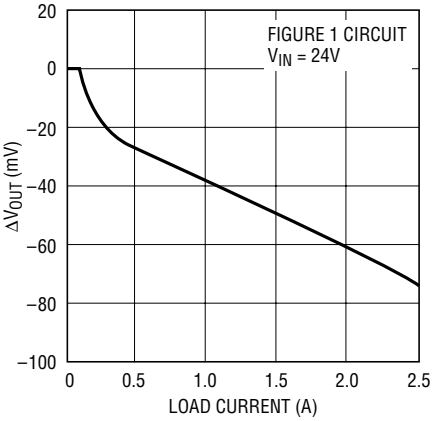
LTC1159 • TPC01

Line Regulation



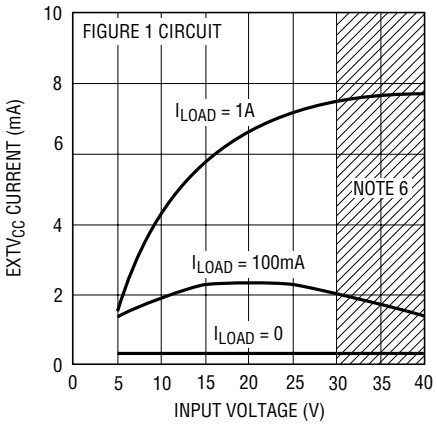
LT1159 • TPC02

Load Regulation



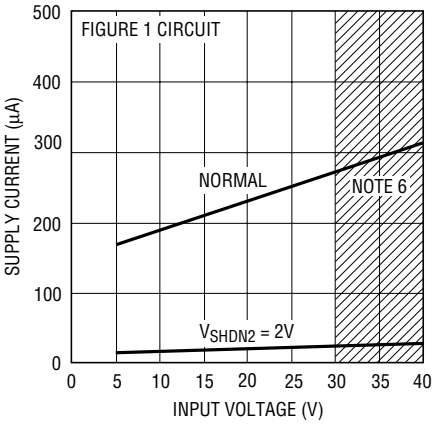
LTC1159 • TPC03

$EXTV_{CC}$ Pin Current



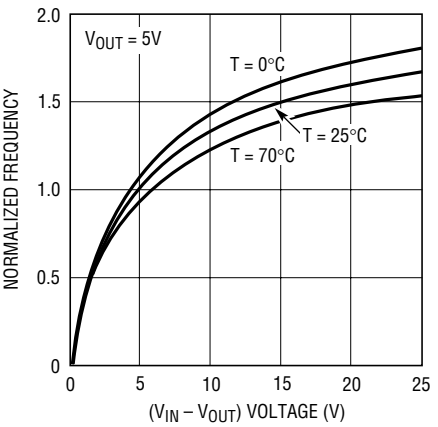
LTC1159 • TPC04

V_{IN} Pin Current



LTC1159 • TPC05

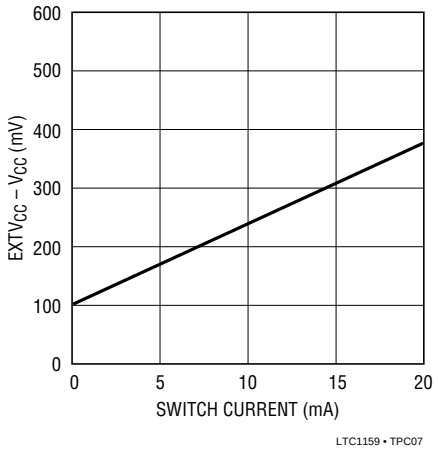
Operating Frequency vs (V_{IN} – V_{OUT})



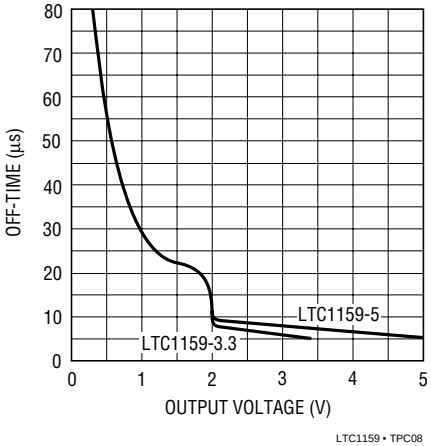
LTC1159 • TPC06

TYPICAL PERFORMANCE CHARACTERISTICS

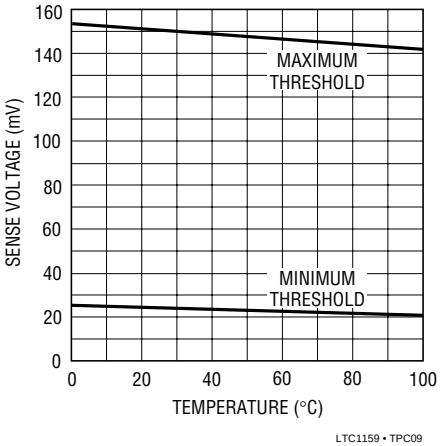
EXTV$_{CC}$ Switch Drop



Off-Time vs V$_{OUT}$



Current Sense Threshold Voltage



PIN FUNCTIONS

V$_{IN}$: Main Supply Input Pin.

SGND: Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

PGND: Driver Power Grounds. Connect to source of N-channel MOSFET and the (–) terminal of C_{IN}.

V$_{CC}$: Outputs of internal 4.5V linear regulator, EXTV$_{CC}$ switch, and supply inputs for driver and control circuits. The driver and control circuits are powered from the higher of the 4.5V regulator or EXTV$_{CC}$ voltage. Must be closely decoupled to power ground.

C$_T$: External capacitor C_T from this pin to ground sets the operating frequency. (The frequency is also dependent on the ratio V_{OUT}/V_{IN}.)

I$_{TH}$: Gain Amplifier Decoupling Point. The current comparator threshold increases with the I_{TH} pin voltage.

V$_{FB}$: For the LTC1159 adjustable version, the V_{FB} pin receives the feedback voltage from an external resistive divider used to set the output voltage.

SENSE$^–$: Connects to internal resistive divider which sets the output voltage in fixed output versions. The SENSE$^–$ pin is also the (–) input of the current comparator.

SENSE$^+$: The (+) Input for the Current Comparator. A built-in offset between the SENSE$^+$ and SENSE$^–$ pins, in conjunction with R_{SENSE}, sets the current trip threshold.

N-Gate: High Current Drive for the Bottom N-Channel MOSFET. The N-Gate pin swings from ground to V_{CC}.

P-Gate: Level-Shifted Gate Drive Signal for the Top P-Channel MOSFET. The voltage swing at the P-gate pin is from V_{IN} to $V_{IN} – V_{CC}$.

P-Drive: High Current Gate Drive for the Top P-Channel MOSFET. The P-drive pin(s) swing(s) from V_{CC} to ground.

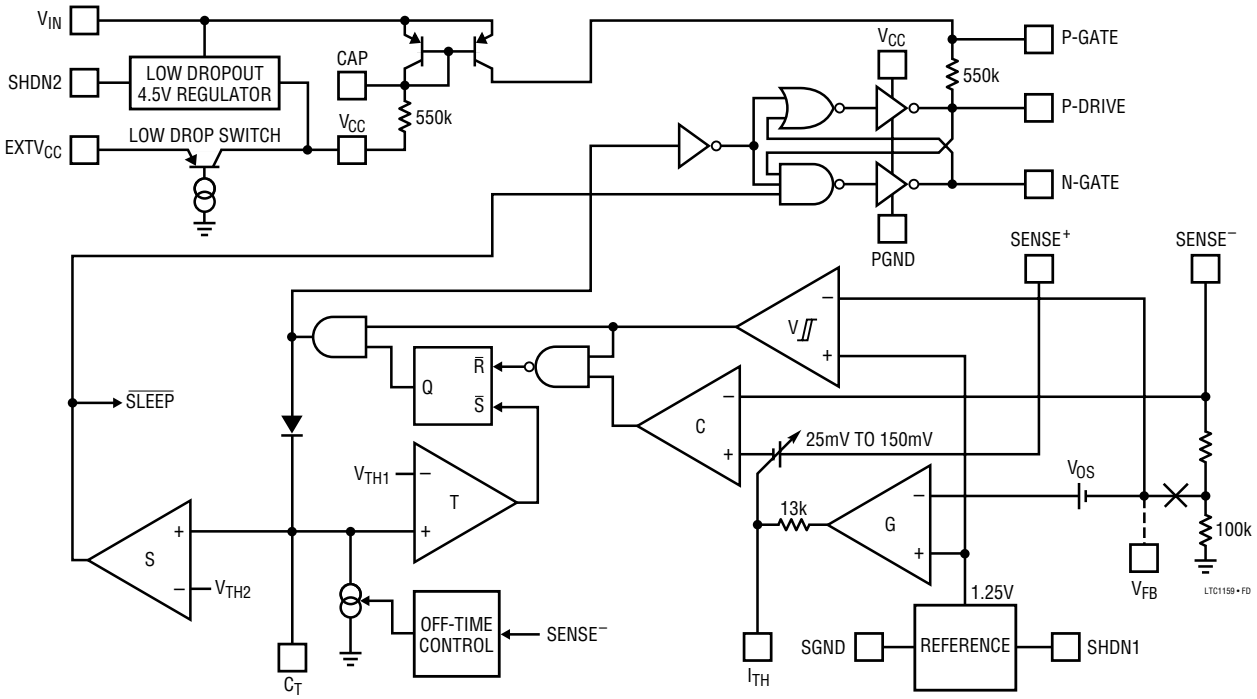
CAP: Charge Compensation Pin. A capacitor to V_{CC} provides charge required by the P-gate level-shift capacitor during supply transitions. *The charge compensation capacitor must be larger than the gate drive capacitor.*

SHDN1: This pin shuts down the control circuitry only (V_{CC} is not affected). Taking SHDN1 pin high turns off the control circuitry and holds both MOSFETs off. This pin must be at ground potential for normal operation.

SHDN2: Master Shutdown Pin. Taking SHDN2 high shuts down V_{CC} and all control circuitry.

FUNCTIONAL DIAGRAM

Internal divider broken at V_{FB} for adjustable versions.



OPERATION

(Refer to Functional Diagram)

The LTC1159 uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the C_T pin.

The output voltage is sensed either by an internal voltage divider connected to the SENSE$^-$ pin (LTC1159-3.3 and LTC1159-5) or an external divider returned to the V_{FB} pin (LTC1159). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1159 automatically switches between two modes of operation, burst and continuous.

A low dropout 4.5V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry during start-up. During normal operation, the LTC1159 family powers the drivers and control from the output via the $EXTV_{CC}$ pin to improve efficiency. The N-GATE pin is referenced to ground and drives the N-channel MOSFET gate directly. The P-channel gate drive must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the P-drive signal via an internal 550k resistor and external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between the SENSE$^+$ and SENSE$^-$ pins connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-gate output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor C_T is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the N-gate output is high, turning on the N-channel MOSFET.

When the voltage on C_T has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-gate output to go low (turning off the N-channel MOSFET) and the P-gate output to also go low (turning the P-channel MOSFET back on). The cycle then repeats. As the load current

OPERATION (Refer to Functional Diagram)

increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{SLEEP}$ line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, much of the circuitry is turned off, dropping the supply current from several milliamps (with the MOSFETs switching) to 300μA. When the output capacitor has discharged by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats. To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset is incorporated in the gain stage.

To prevent both the external MOSFETs from being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-gate output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low when the N-gate output is high.

APPLICATIONS INFORMATION

The LTC1159 Compared to the LTC1148/LTC1149 Families

The LTC1159 family is closest in operation to the LTC1149 and shares much of the applications information. In addition to reduced quiescent and shutdown currents, the LTC1159 adds an internal switch which allows the driver and control sections to be powered from an external source for higher efficiency. This change affects Power MOSFET Selection, $EXTV_{CC}$ Pin Connection, Important Information About LTC1159 Adjustable Applications, and Efficiency Considerations found in this section.

The basic LTC1159 application circuit shown in Figure 1 is limited to a maximum input voltage of 30V due to MOSFET breakdown. If the application does not require greater than 18V operation, then the LTC1148 or LTC1148HV should be used. For higher input voltages where quiescent and shutdown current are not critical, the LTC1149 may be a better choice since it is set up to drive standard threshold MOSFETs.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1159 current comparator has a threshold range that extends from a minimum of $0.025V/R_{SENSE}$ to a maximum of $0.15V/R_{SENSE}$. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)} = 0.025V/R_{SENSE}$ (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1159 and external component values yields:

$$R_{SENSE} = \frac{100}{I_{MAX}}\ m\Omega$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2. The LTC1159 series works well with values of R_{SENSE} from 0.02Ω to 0.2Ω.

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short-circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following equations:

APPLICATIONS INFORMATION

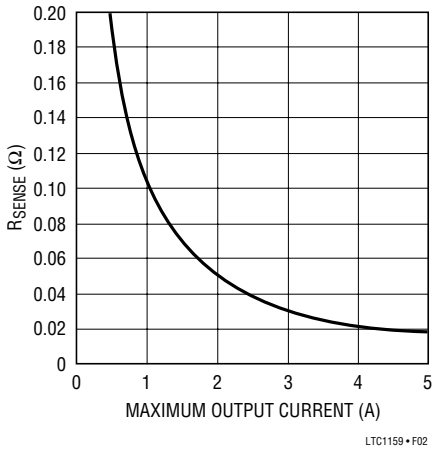


Figure 2. R_{SENSE} vs Maximum Output Current

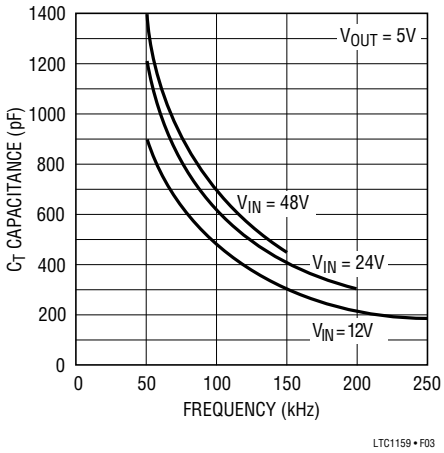


Figure 3. Timing Capacitor Selection

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1159 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The LTC1159 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{7.8 \bullet 10^{-5}}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where $t_{OFF} = 1.3 \bullet 10^4 \bullet C_T$

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $0.025V/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \bullet 10^5 \bullet R_{SENSE} \bullet C_T \bullet V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the LTC1159 may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As inductance increases, core losses go down but copper (I^2R) losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered in the LTC1159. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new surface mount designs available from Coiltronics do not increase the height significantly.

Power MOSFET Selection

Two external power MOSFETs must be selected for use with the LTC1159: a P-channel MOSFET for the main switch and an N-channel MOSFET for the synchronous switch.

The peak-to-peak drive levels are set by the V_{CC} voltage on the LTC1159. This voltage is typically 4.5V during start-up and 5V to 7V during normal operation (see $EXTV_{CC}$ Pin Connection). Consequently, *logic-level threshold MOSFETs must be used in most LTC1159 family applications*. The only exception is applications in which $EXTV_{CC}$ is powered from an external supply greater than 8V, in which standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the LTC1159 is operating in continuous mode, the duty cycle for the P-channel MOSFET is given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET dissipations at maximum output current are given by:

$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_P) R_{DS(ON)} + k(V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_N) R_{DS(ON)}$$

where ∂ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the P-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The N-channel MOSFET losses are the greatest at high input voltage or during a short circuit when the N-channel duty cycle is nearly 100%.

The term $(1 + \partial)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\partial = 0.007/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET electrical characteristics. The constant $k = 5$ can be used for the LTC1159 to estimate the relative contributions of the two terms in the P-channel dissipation equation.

The Schottky diode D1 shown in Figure 1 only conducts during the dead time between the conduction of the two power MOSFETs. D1 prevents the body diode of the N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.6V when conducting I_{MAX}.

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C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}\,[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{MAX}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. An additional 0.1µF ceramic capacitor may also be required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1159:

$$C_{OUT}\ \text{Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. Manufacturers such as Nichicon, Chemicon, and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum value of C_{OUT} is suggested to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes the Burst Mode operation to be activated when the LTC1159 would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

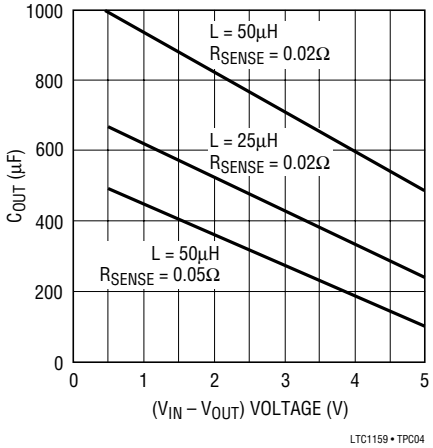

Figure 4. Minimum Suggested C_{OUT}

Load Transient Response

Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The I_{TH} external components shown in the Figure 1 circuit will provide adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The

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discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Line Transient Response

The LTC1159 has better than 60dB line rejection and is generally impervious to large positive or negative line voltage transients. However, one rarely occurring condition can cause the output voltage to overshoot if the proper precautions are not observed. This condition is a negative V_{IN} transition of several volts followed within 100µs by a positive transition of greater than 0.5V/µs slew rate.

The reason this condition rarely occurs is because it takes tens of amps to slew the regulator input capacitor at this rate! The solution is to add a diode between the cap and V_{IN} pins of the LTC1159 as shown in several of the typical application circuits. If you think your system could have this problem, add the diode. Note that in surface mount applications it can be combined with the P-gate diode by using a low cost common cathode dual diode.

$EXTV_{CC}$ Pin Connection

The LTC1159 contains an internal PNP switch connected between the $EXTV_{CC}$ and V_{CC} pins. The switch closes and supplies the V_{CC} power whenever the $EXTV_{CC}$ pin is higher in voltage than the 4.5V internal regulator. This allows the MOSFET driver and control power to be derived from the output during normal operation and from the internal regulator when the output is out of regulation (start-up, short circuit).

Significant efficiency gains can be realized by powering V_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V regulators this simply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other low voltage regulators, additional circuitry is required to derive V_{CC} power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Left Open. This will cause V_{CC} to be powered only from the internal 4.5V regulator resulting in reduced MOSFET gate drive levels and an efficiency penalty of up to 10% at high input voltages.

2. $EXTV_{CC}$ Connected Directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.

3. $EXTV_{CC}$ Connected to an Output-Derived Boost Network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.5V. This can be done either with the inductive boost winding shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics and generally provides the highest efficiency at the expense of a slightly higher parts count.

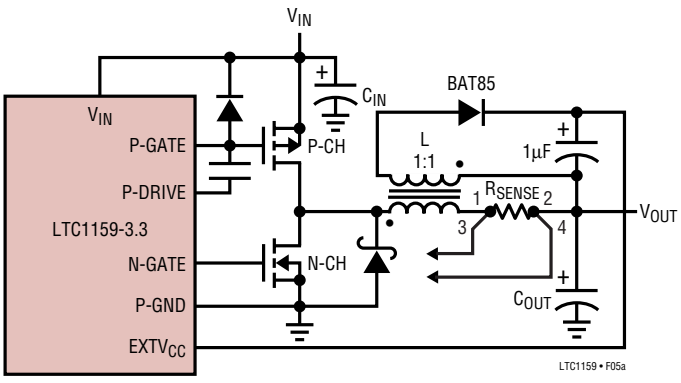

Figure 5a. Inductive Boost Circuit for $EXTV_{CC}$

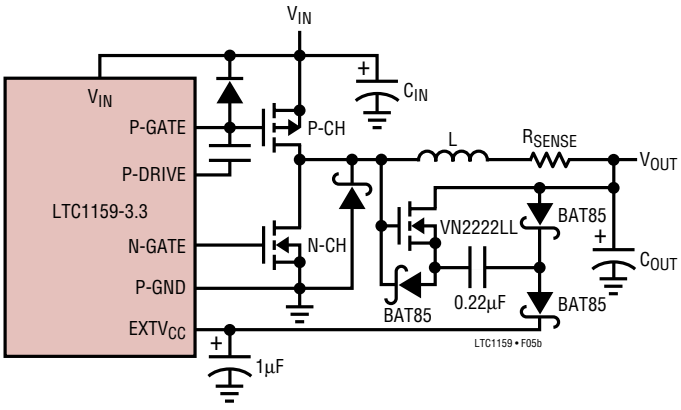

Figure 5b. Capacitive Charge Pump for $EXTV_{CC}$

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4. $EXTV_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 12V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. There are no restrictions on the $EXTV_{CC}$ voltage relative to V_{IN}. $EXTV_{CC}$ may be higher than V_{IN} providing $EXTV_{CC}$ does not exceed the 15V absolute maximum rating.

When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive. The LTC1149 family should also be considered for applications which require the use of standard threshold MOSFETs.

Important Information About LTC1159 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1159 adjustable version is used with an external resistive divider from V_{OUT} to the V_{FB} pin (Figure 6). The regulated voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) 1.25V$$

The V_{FB} pin is extremely sensitive to pickup from the inductor switching node. Care should be taken to isolate the feedback network from the inductor, and the 100pF capacitor should be connected between the V_{FB} and SGND pins next to the package.

In LTC1159N and LTC1159S applications with V_{OUT} > 5.5V, the V_{CC} pin may self-power through the SENSE pins when SHDN2 is taken high, preventing shutdown. In these applications, a pull-down must be added to the $SENSE^-$ pin as shown in Figure 6. This pull-down effectively takes the place of the SHDN1 pin, ensuring complete shutdown. Note: For versions in which both the SHDN1 and SHDN2 pins are available (LTC1159G and all fixed output versions), the two pins are simply connected to each other and driven together to guarantee complete shutdown.

The Figure 6 circuit cannot be used to regulate a V_{OUT} which is greater than the maximum voltage allowed on the LTC1159 SENSE pins (13V). In applications with V_{OUT} > 13V, R_{SENSE} must be moved to the ground side of the output capacitor and load. This operates the current sense comparator at 0V common mode, increasing the off-time approximately 40% and requiring the use of a smaller timing capacitor C_T.

Inverting Regular Applications

The LTC1159 can also be used to obtain negative output voltages from positive inputs. In these inverting applications, the current sense resistor connects to ground while the LTC1159 and N-channel MOSFET connections, which would normally go to ground, instead ride on the negative output. This allows the negative output voltage to be set by

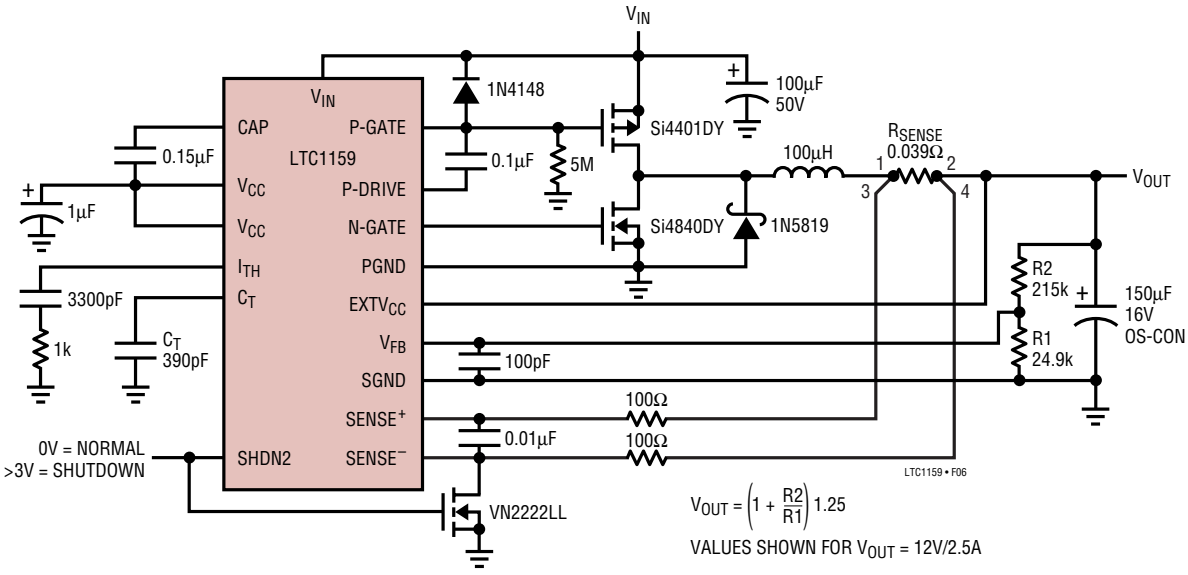

Figure 6. High Efficiency Adjustable Regulator with 5.5V < V_{OUT} < 13V

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the same process as in conventional applications, using either the internal divider (LTC1159-3.3, LTC1159-5) or an external divider with the adjustable version.

Figure 15 in the Typical Applications shows a synchronous 12V to –12V converter that can supply up to 1A with better than 85% efficiency. By grounding the $EXTV_{CC}$ pin in the Figure 15 circuit, the entire 12V output voltage is placed across the driver and control circuits since the LTC1159 ground pins are at –12V. During start-up or short-circuit conditions, operating power is supplied by the internal 4.5V regulator. The shutdown signal is level-shifted to the negative output rail by Q3, and Q4 ensures that Q1 and Q2 remain off during the entire shutdown sequence.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100 - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1159 circuits: 1) LTC1159 V_{IN} current, 2) LTC1159 V_{CC} current, 3) I^2R losses and 4) P-channel transition losses.

1. LTC1159 V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<1%) loss which increases with V_{IN}.

2. LTC1159 V_{CC} current is the sum of the MOSFET driver and control circuit currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{CC} to ground. The resulting dQ/dt is a current out of V_{CC} which is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} \approx f(Q_P + Q_N)$, where Q_P and Q_N are the gate charges of the two MOSFETs.

By powering $EXTV_{CC}$ from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For example in a 20V to 5V application, 10mA of V_{CC} current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode all of the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.1\Omega$, $R_L = 0.15\Omega$, and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.

4. Transition losses apply only to the P-channel MOSFET, and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} \approx 5(V_{IN})^2(I_{MAX})(C_{RSS})(f)$$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead time, and inductor core losses, generally account for less than 2% total additional loss.

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1159 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network that cancels the 0.025V minimum current comparator threshold. This technique is also useful for eliminating audible noise from

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certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the SENSE$^-$ pin to subtract from the built-in 0.025V offset. An example of this technique is shown in Figure 7. Two 100Ω resistors are inserted in series with the leads from the sense resistor. With the addition of R3, a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1 + R3}\right)$$

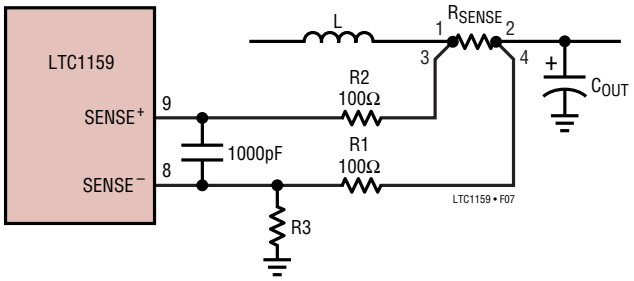

Figure 7. Suppressing Burst Mode Operation

If V_{OFFSET} > 0.025V, the minimum threshold will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be reduced:

$$R_{SENSE} \approx \frac{75}{I_{MAX}}\ m\Omega$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across the SENSE$^-$ and SENSE$^+$ pins.

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1159. These items are also illustrated graphically in the layout diagram of Figure 8. Check the following in your layout:

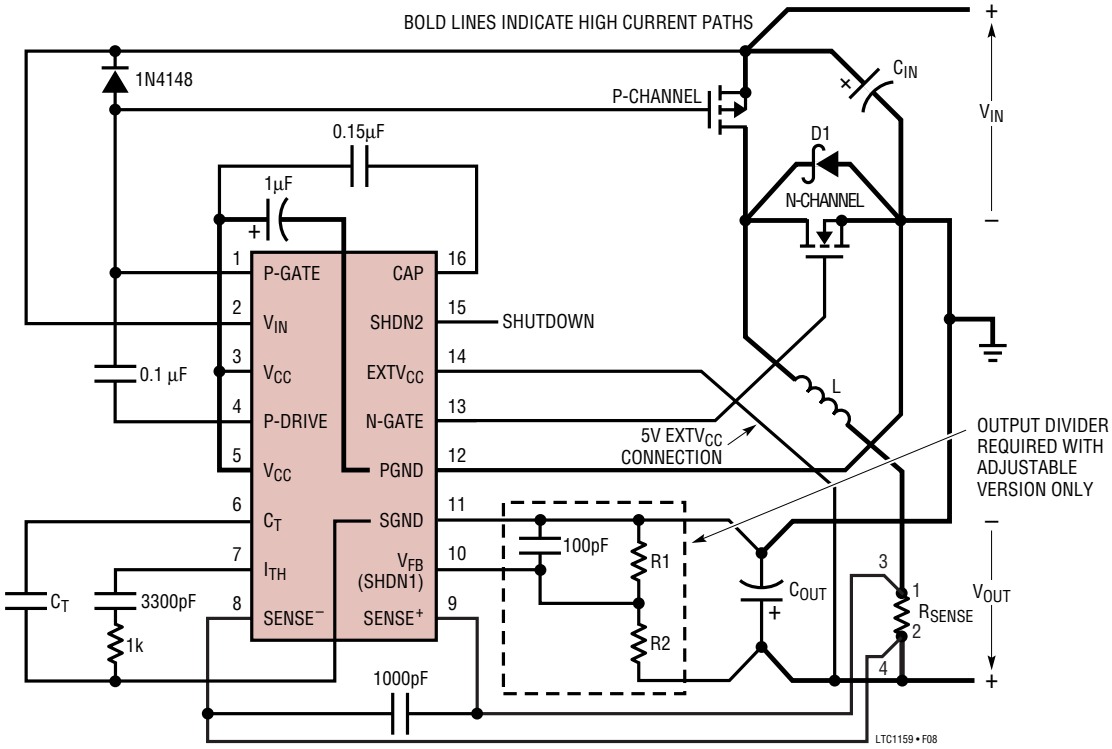

Figure 8. LTC1159 Layout Diagram (N and S Packages)

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1) Are the signal and power grounds segregated? The LTC1159 signal ground must connect separately to the (–) plate of C_{OUT}. The other ground pin(s) should return to the source of the N-channel MOSFET, anode of the Schottky diode and (–) plate of C_{IN}, which should have as short lead lengths as possible.

2) Does the LTC1159 SENSE$^-$ pin connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.

3) Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The differential decoupling capacitor between the two SENSE pins should be as close as possible to the LTC1159. Up to 100Ω may be placed in series with each sense lead to help decouple the SENSE pins. However, when these resistors are used, the capacitor should be no larger than 1000pF.

4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1µF ceramic capacitor between V_{IN} and power ground may be required in some applications.

5) Is the V_{CC} decoupling capacitor connected closely between the V_{CC} pins of the LTC1159 and power ground? This capacitor carries the MOSFET driver peak currents.

6) In adjustable versions, the feedback pin is very sensitive to pickup from the switch node. Care must be taken to isolate V_{FB} from possible capacitive coupling of the inductor switch signal.

7) Is the SHDN1 pin actively pulled to ground during normal operation? SHDN1 is a high impedance pin and must not be allowed to float.

Troubleshooting Hints

Since efficiency is critical to LTC1159 applications it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the C_T pin .

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a. When the load current is low ($I_{LOAD} < I_{BURST}$), Burst Mode operation should occur with the C_T waveform periodically falling to ground as shown in Figure 9b.

If the C_T pin is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

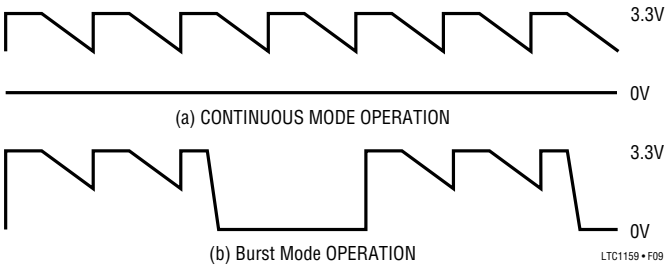


Figure 9. C_T Pin 6 Waveforms

TYPICAL APPLICATIONS

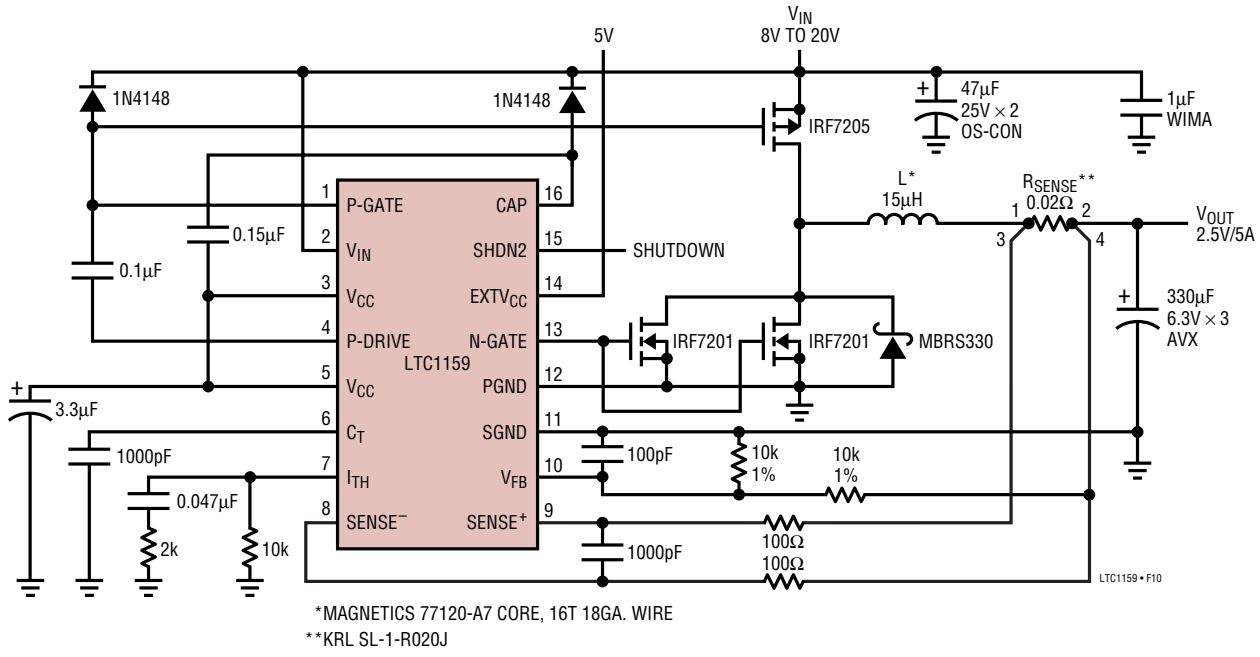


Figure 10. High Efficiency 8V to 20V Input 2.5/5A Output Regulator

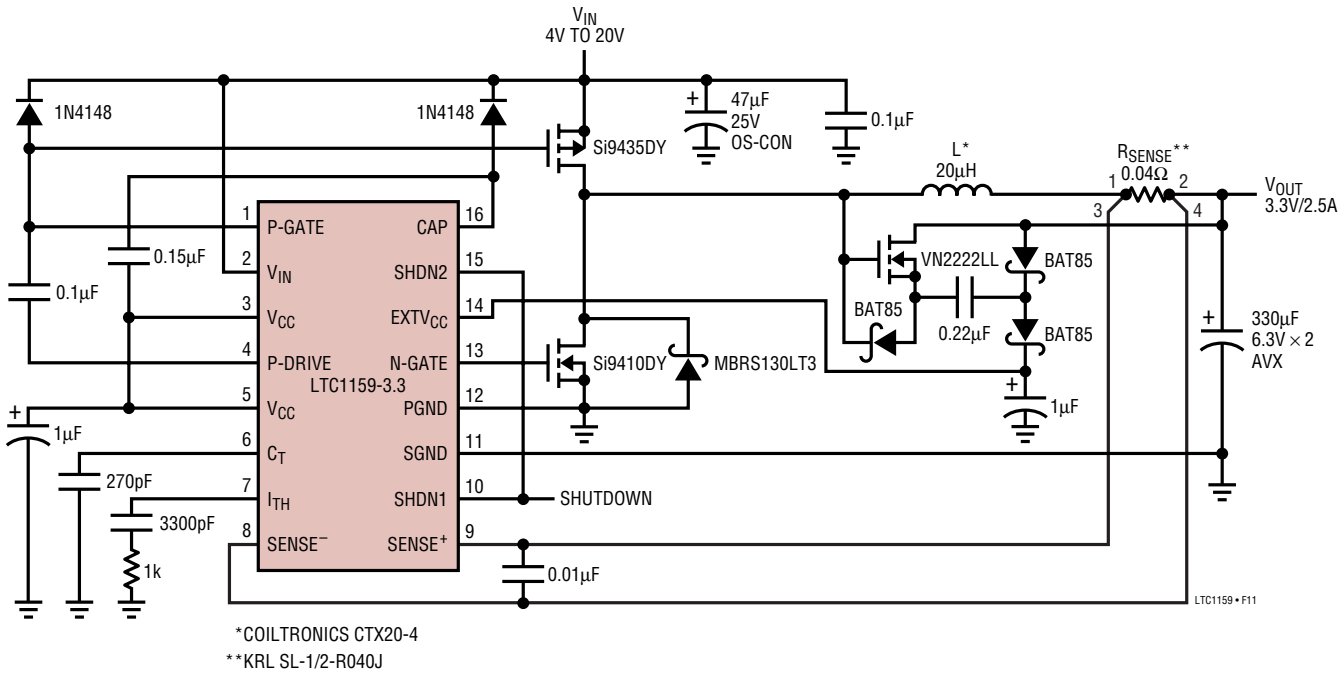


Figure 11. 5:1 Input Range (4V to 20V) High Efficiency 3.3V/2.5A Regulator

TYPICAL APPLICATIONS

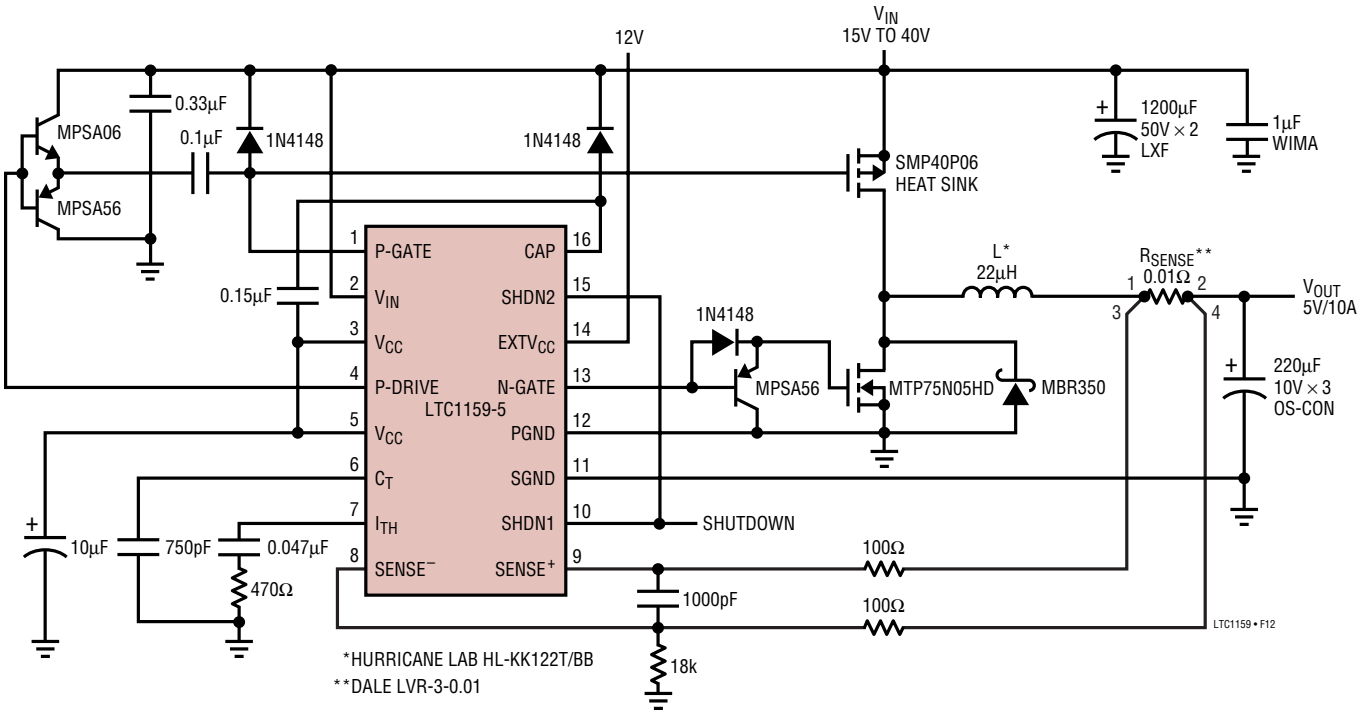


Figure 12. High Current, High Efficiency 15V to 40V Input 5V/10A Output Regulator

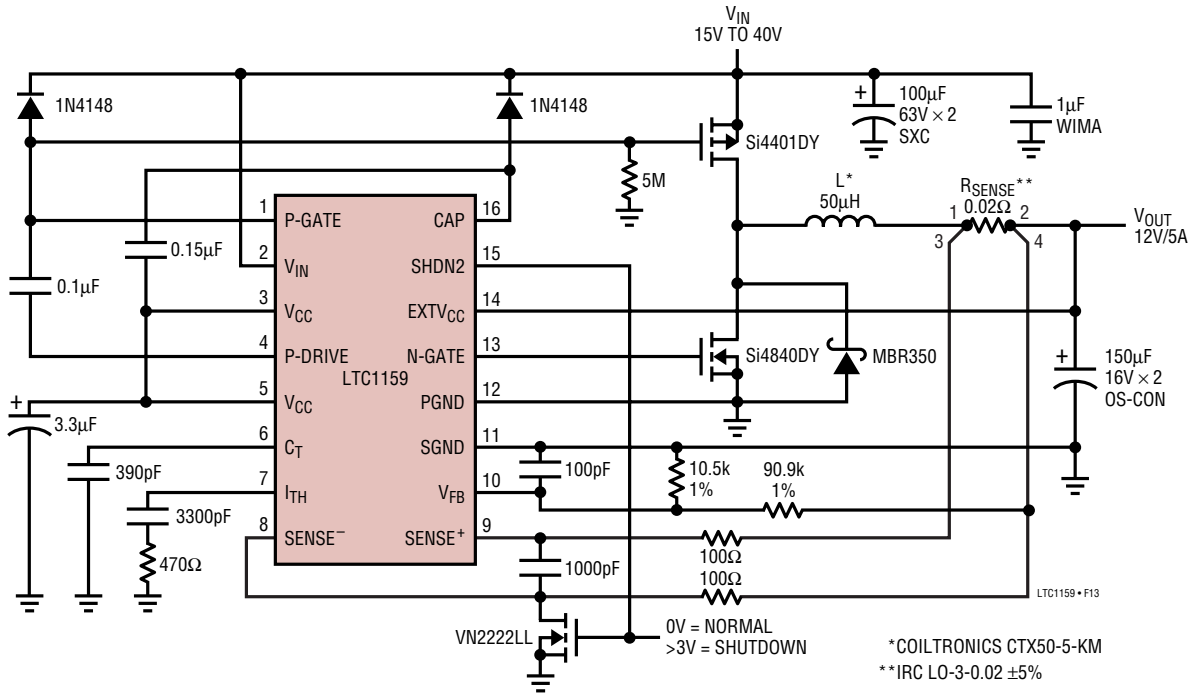


Figure 13. High Efficiency 15V to 40V Input 12V/5A Output Regulator

TYPICAL APPLICATIONS

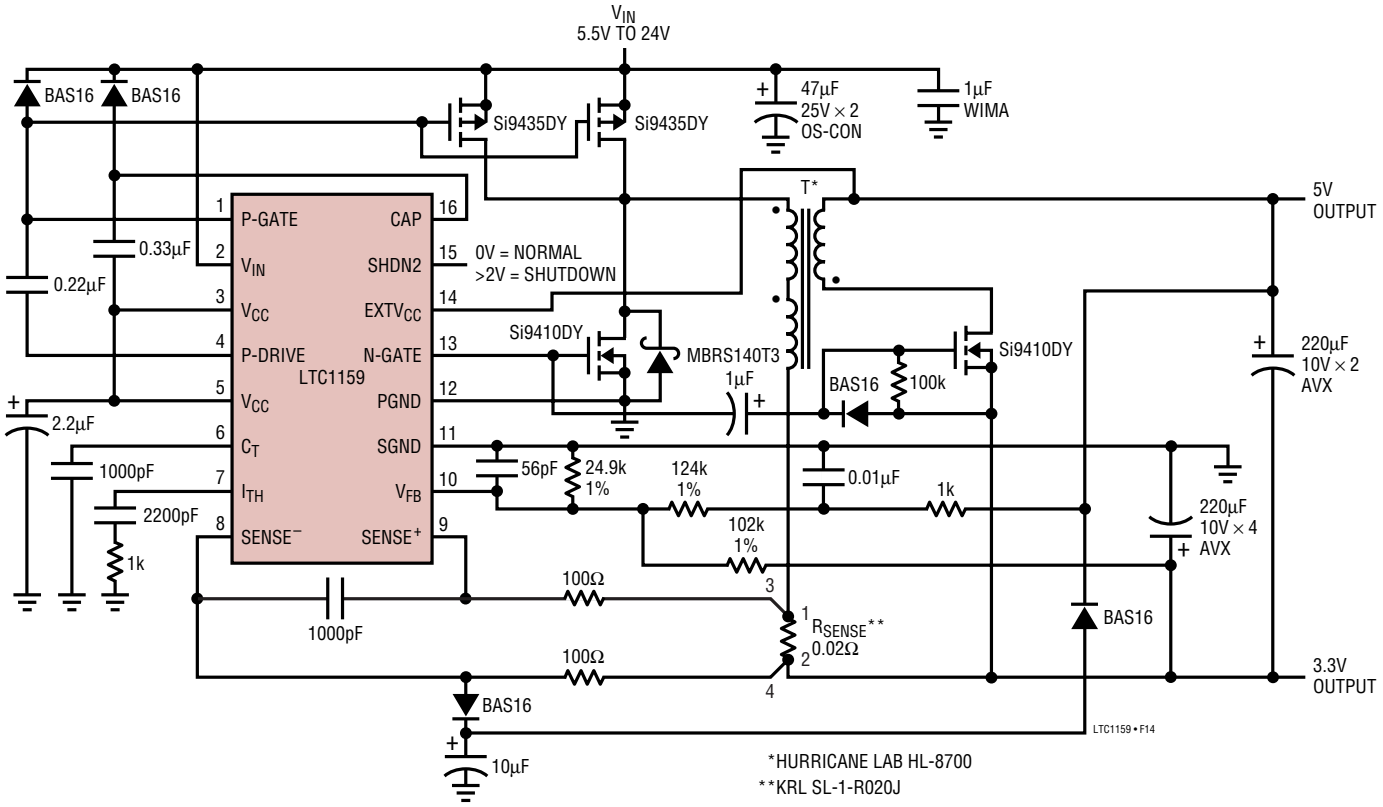
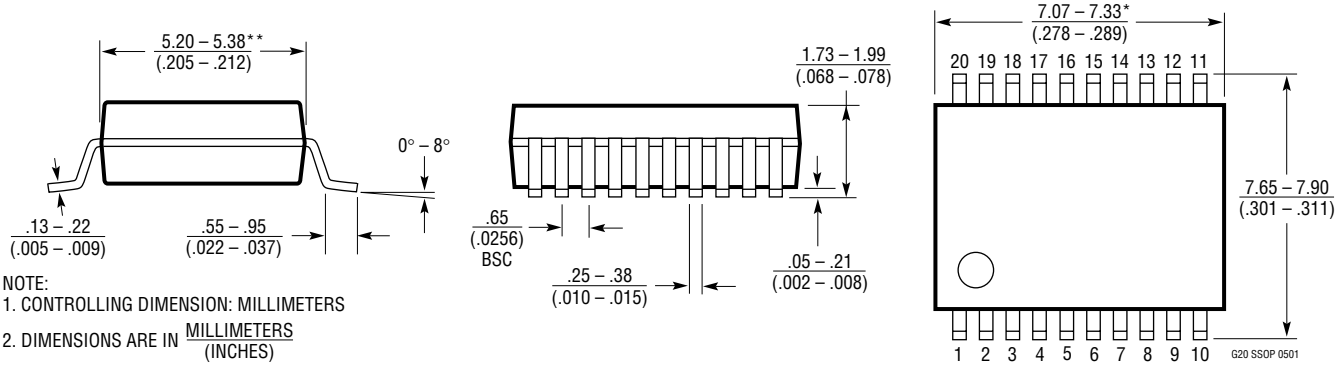


Figure 14. 17W Dual Output High Efficiency 5V and 3.3V Regulator

PACKAGE DESCRIPTION

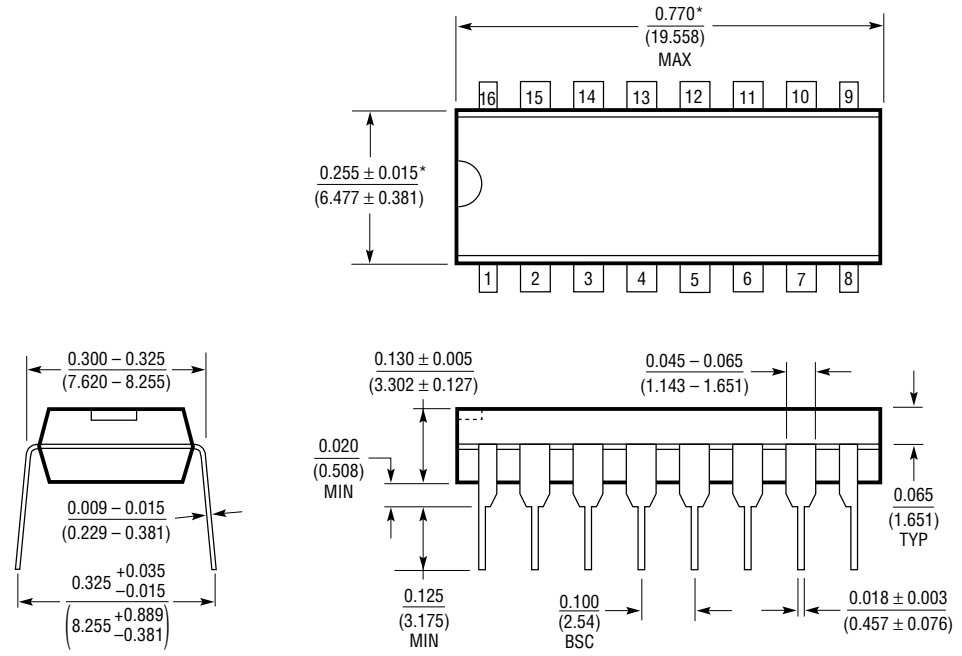
G Package
20-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

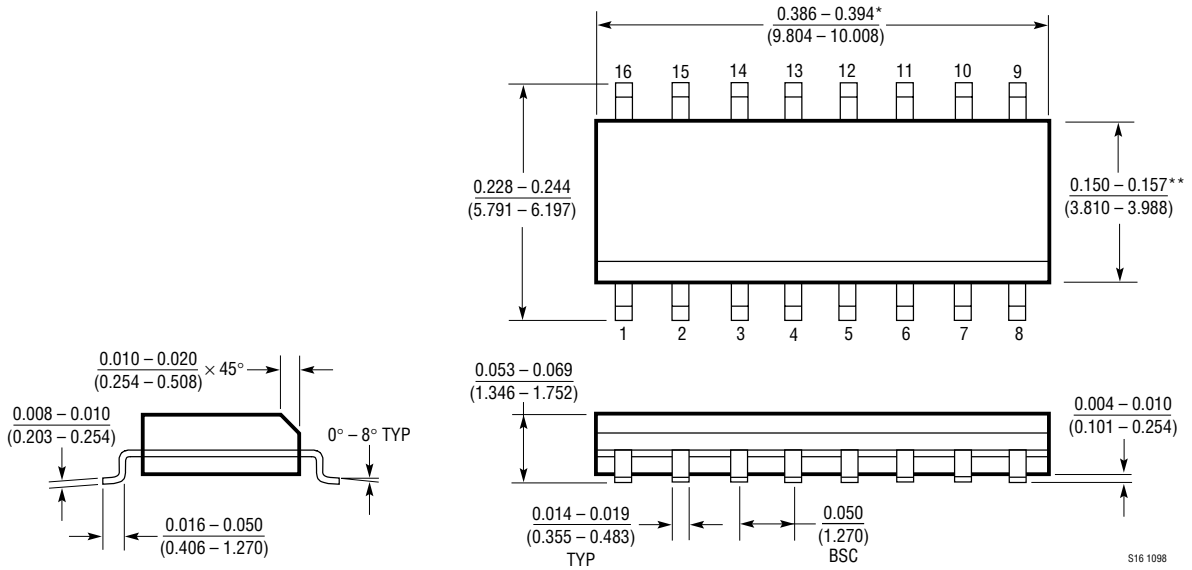
N Package
16-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1098

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



S16 1098

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

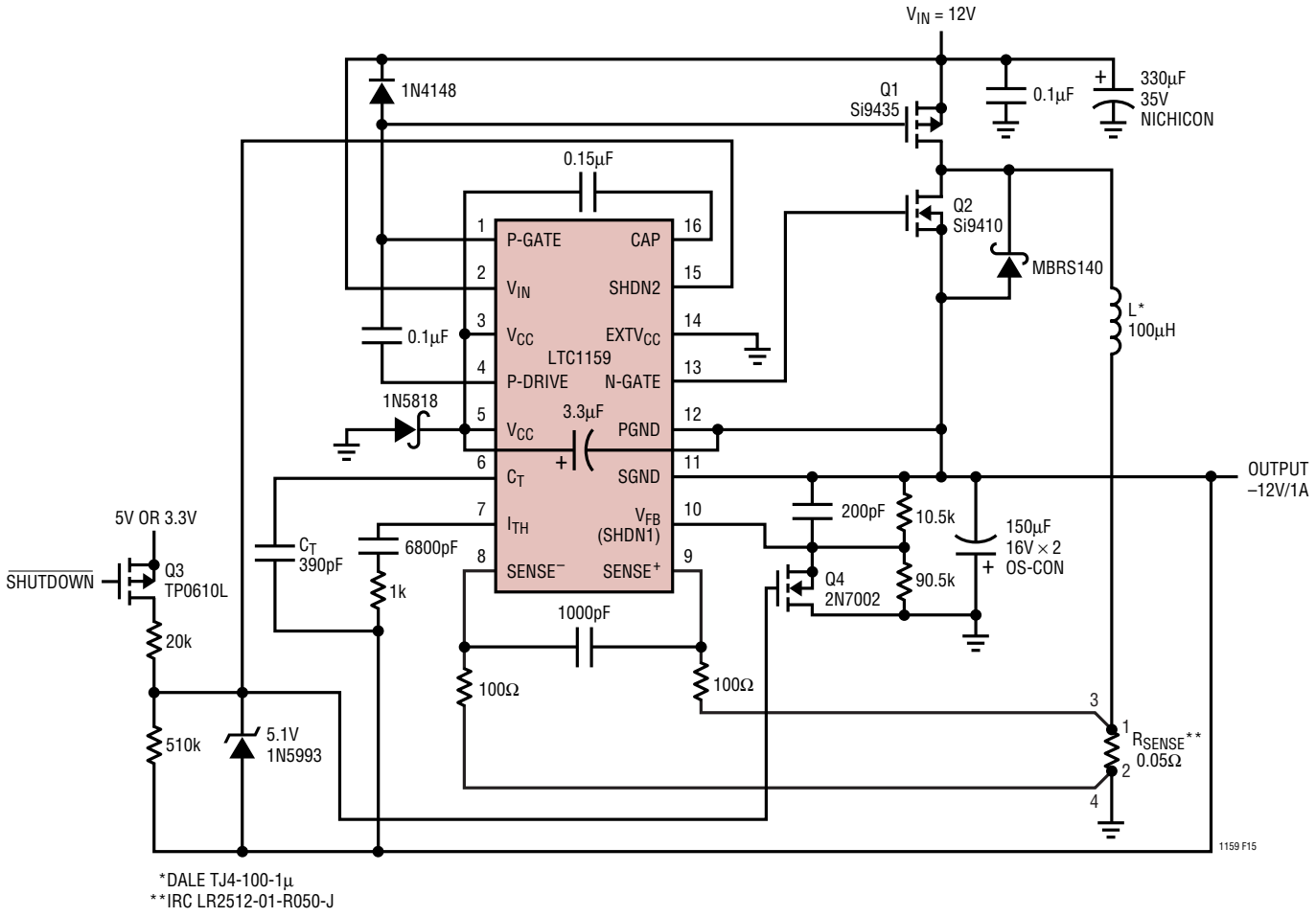


Figure 15. High Efficiency 12V to –12V 1A Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628	2-Phase, Dual Step-Down Controller	$V_{IN} \leq 36V$, Minimum C_{IN}, Current Mode
LTC1702	550kHz Dual, 2-Phase Step-Down Controller	Minimum C_{IN}, No Sense Resistor Required, $V_{IN} \leq 7V$
LTC1735	Synchronous Step-Down Controller	$3.5V \leq V_{IN} \leq 36V$, $0.8V \leq V_{OUT} \leq 6V$, Synchronizable
LTC1773	550kHz Synchronous Step-Down Controller	$2.65V \leq V_{IN} \leq 8.5V$, $0.8V \leq V_{OUT} \leq V_{IN}$, Synchronizable to 750kHz, MS10
LTC1778	No R_{SENSE}™ Step-Down Controller	No Sense Resistor Required, $t_{ON(MIN)} \leq 100ns$, Current Mode, GN16
LTC1876	Triple Output, 2-Phase Controller	Two, 2-Phase Step-Down Controllers and Step-Up DC/DC Converter in One IC

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