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PRODUCT DESCRIPTION

The Le87220 device is a low-power, dual xDSL differential line driver. It is part of Zarlink's family of integrated line drivers capable of operating from a standard negative battery supply. Its integration of feedback components and on-chip surge protection diodes makes it one of the most integrated line drivers on the market today.

The Le87220 device was designed on a high voltage, high bandwidth bipolar process in which fast slew rate and low distortion amplifiers were implemented. It requires one line transformer per line for isolation and for compliance with IEC60950-1, 2001 and UL60950 standards. The line driver amplifiers in the Le87220 device were designed with an optimized bandwidth for xDSL applications as well as for fast slew rates of 300 V/µs.

Lightning and Power Surges

The Le87220 device has built-in lightning and power surge protection. When used with the components listed in the *PCB Layout*, on page 8, it needs no other external protector to meet the requirements for ADSL line Cards.

Block Description

Refer to the datapath provider for the application circuit.

Downstream Path

The downstream signal is applied at the DDWNP/DDWNN pins, and is amplified by a fixed voltage gain (K_{DWN}) before being applied to the AY and BY pins. The amplifiers driving the AY and BY pins are DC biased to approximately one-half of the VBAT pin voltage. The typical differential output voltage swing between AY and BY pins is |VBAT| - 4 V. This allows the use of a step-down transformer for the line interface.

Control Logic

This block controls the bias currents of the input stage and the bias current of the output amplifiers as described in the *Device Operating Modes* section below.

DEVICE OPERATING MODES

The two lines of the Le87220 are completely independent and can be programmed to be in different operating modes. The logic signal level of pins DISCON1 an Pdown1 controls the operating mode of line 1, the logic signal level of pins DISCON2 and Pdown2 controls the operating mode of line 2.

Active Mode

In this mode, all stages are biased and operational.

PDown Mode

In this mode, the line driver amplifier's power consumption is reduced. The Bias current in the output stage drops to almost half full power stage. The part is ADSL compliant in this stage.

Disconnect Mode

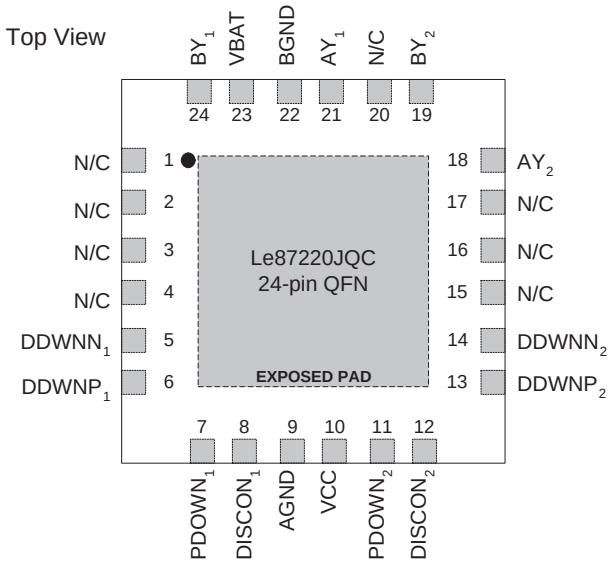
In this mode, the bias is turned OFF to all stages to save power. The device is not operational.

Operating Mode Control Decoding

$DISCON_1$	$Pdown_1$	Line 1 Operating Mode
0	0	Active
0	1	Pdown
1	x	Disabled

$DISCON_2$	$Pdown_2$	Line 2 Operating Mode
0	0	Active
0	1	Pdown
1	x	Disabled

CONNECTION DIAGRAM



Notes:

1. *Pin 1 is marked for orientation.*
2. *The Le87220 device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias, for proper heat dissipation (**See PCB Layout, on page 8.**).*

PIN DESCRIPTIONS

Pin	Pin Name	Type	Description
$Pdown_1$, $Pdown_2$	Control Bits	Input	Active/Pdown mode control bit.
$DDWNP_1$, $DDWNN_1$, $DDWNP_2$, $DDWNN_2$	Differential Downstream	Input	The differential downstream signal from the data AFE is AC coupled to these pins.
$DISCON_1$, $DISCON_2$	Disconnect	Input	Disables the line completely by pulling it to VCC.
AY_1, BY_1 AY_2, BY_2	A/B Line Driver	Output	Differential downstream line driver outputs.
VBAT	Negative Battery	Power	Negative power supply.
VCC	Power Supply	Power	+3.3 V analog power supply.
AGND	Analog Ground	Ground	Low voltage ground return.
BGND	Battery Ground	Ground	Battery ground return.
N/C	No Connect		Not connected.
EXPOSED PAD		Isolated	Exposed pad on underside of device must be connected to a heat spreading area. The AGND plane is recommended.

ABSOLUTE MAXIMUM RATINGS

Stresses above the values listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-55 \le T_A \le +150°C$
Ambient temperature, under bias	$-40 \le T_A \le +85°C$
V_{CC} with respect to AGND	–0.4 V to +6 V
V_{BAT} with respect to BGND	+0.4 V to -75 V
BGND with respect to AGND (1 ms)	–5.5 V to +0.2 V
Maximum Current into AY, BY	
Continuous	±200 mA
100 µs (F = 0.1 Hz)	±1 A
1 µs (F = 0.1 Hz)	±2.5 A
250 ns (F = 0.1 Hz)	±5.5 A
Peak current output, AY or BY pins	±200 mA
Pdown, DISCON pins with respect to AGND	–0.4 V to (V_{CC} + 0.4 V)
Maximum Power Dissipation, T_A = 85°C (See Notes 1 and 2)	2 W
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant
ESD Immunity (Charge Device Model)	Class C6 1500 - 2000 V

Notes:

1. *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. Continuous operation above 145°C junction temperature may degrade device reliability.*
2. *The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane (**See PCB Layout, on page 8.**).*

Thermal Resistance

The junction to air thermal resistance of the Le87220 device in a 24-pin QFN package is 30°C/W (measured with infinite external heat sinking). Please refer to Zarlink's *QFN Package* application note, available from http://www.zarlink.com , for layout and heat sinking guidelines.

Package Assembly

The standard (non-green) package devices are assembled with industry-standard mold compounds, and the leads possess a tin/lead (Sn/Pb) plating. These packages are compatible with conventional SnPb eutectic solder board assembly processes. The peak soldering temperature should not exceed 225°C during printed circuit board assembly.

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Zarlink guarantees the performance of this device over commercial (0°C to 70°C) and industrial (–40°C to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled with periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient temperature	-40°C to +85°C
V_{CC}	+3.3 V ± 5%
V_{BAT}	-42 V to -72 V
BGND with respect to AGND	-2 to +0.1VDC

The Le87220 is designed to operate with a standard telecom battery. The normal operating voltage of such batteries is -52 V, and the Le87220 is designed to give optimal performance in terms of power dissipation if used with the provided applications circuit. However, because the Le87220 is designed on Zarlink's proprietary high voltage, high bandwidth process, the part will continue to remain in operation without any degradation in data performance should the battery drop to as low as -42 V, or charge to as high as -72 V. Should there be a need to operate the part continuously at such voltages, a different applications circuit should be considered to achieve best power performance. Lower voltage operation can be achieved by adding a buck-boost regulator.

The Le87220 is designed to operate with the T1.315 specified telecom battery, without any need for changes in the reference design.

ELECTRICAL CHARACTERISTICS

V_{BAT} = -52 V, V_{CC} = +3.3 V, T_A = 25°C unless otherwise specified.

Supply Currents and Power Consumption

Values listed in the table below are per line, and include the load power.

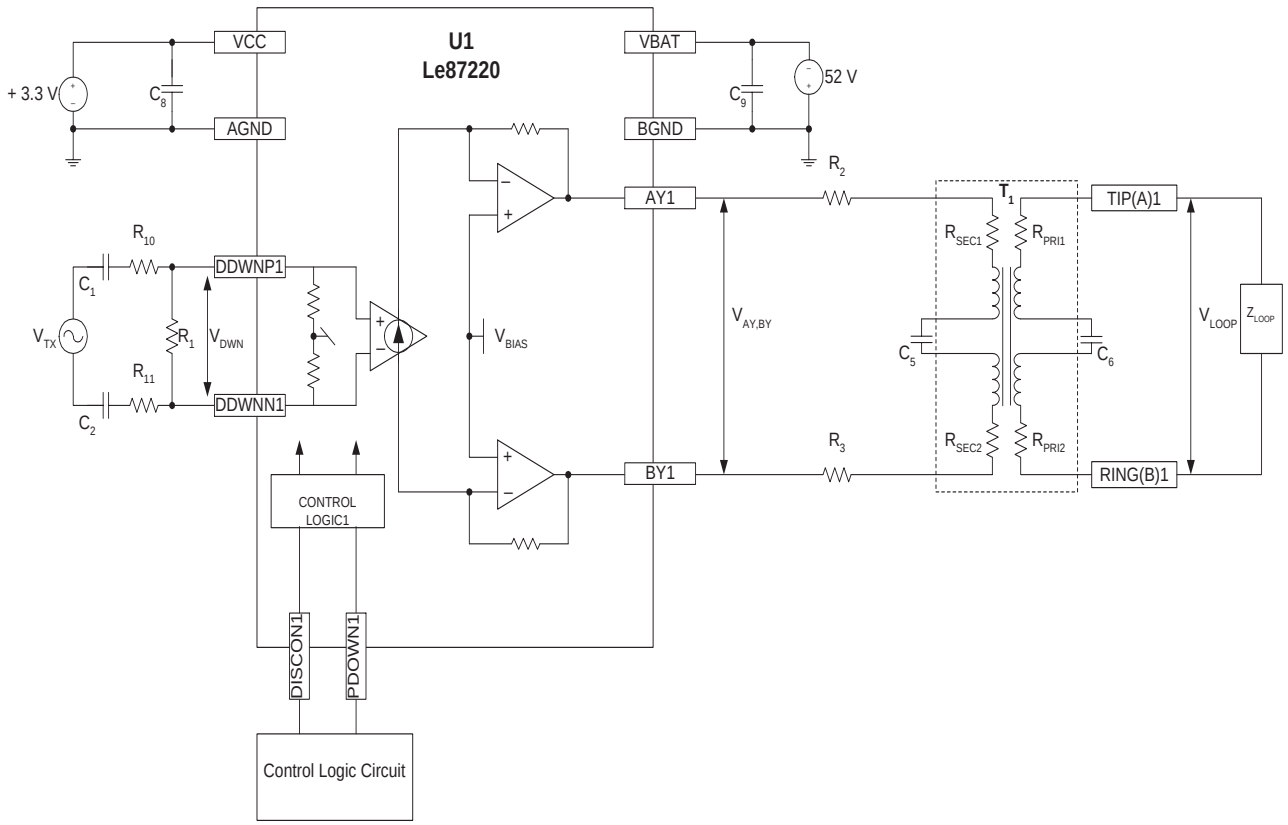
Operational State	Condition	T_A	V_{BAT} (mA)			V_{CC} (mA)			Device Power (mW)			Note
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Active	Training at 5 kft 26 AWG cable	25°C		16			5.3			850		1.
	Showtime at 5 kft 26 AWG cable, 19.85 dBm	25°C		15.5			5.3			824		
	19.85 dBm signal into 100 Ω load with 2.45:1 transformer	25°C		15.5			5.3			824		
		Full range		15.5			5.6			826		
Pdown		25°C		14.5			5.3			772		
		Full range		14.5			5.3			772		
Disconnect		Full range		1			5.3			65		

Note:

1. In the Active state, 96.6 mW is dissipated in the loop and 7.5 mW is dissipated in the transformer plus the series drive resistors. For device power dissipation, subtract these values from the numbers listed in the table above.

TEST CIRCUIT

Only one of two channels is shown.



Note:

1. Component values are the same as those listed in the PCB Layout, on page 8 unless otherwise noted.

SPECIFICATIONS

Device Specifications

Typical Conditions: V_{BAT} = –52 V, V_{CC} = 3.3 V, Transformer Turns Ratio = 2.45:1

Min/Max Parameters: T = –40 to +85°C; Typ, T_A = 25°C

Note:

Parameters in the following "Device Specifications" tables are guaranteed by characterization. Refer to Test Circuit, on page 6.

Table 1. Pdown = 0 (Full Power)

Specification	Condition	Min	Typ	Max	Unit	Note
AC Characteristics						
Vn_{DWN}	Output Differential Noise Voltage, at (AY, BY) V_{TX}=0 V, 25 kHz to 2208 kHz		0.6	1.0	$\frac{\mu V}{\sqrt{Hz}}$	
R_{DDWN}	Differential Input Impedance DDWNP to DDWNN	28k	40k	52k	kΩ	
V_{AYDC}, V_{BYDC}	AY, BY DC bias voltage	$\frac{V_{BAT}}{2} - 0.25$	$\frac{V_{BAT}}{2} + 0.75$	$\frac{V_{BAT}}{2} + 1.75$	V	
$PSRR_{VCC}$	VCC to AY, BY, All operating Modes: 20 kHz	–38			dB	
	400 kHz	–26				
	800 kHz	-24				
	2 MHz	–20				
$PSRR_{VBAT}$	VBAT to AY, BY, All operating Modes: 20 kHz	–50				
	400 kHz	–44				
	800 kHz	-37				
	2 MHz	–32				
$PSRR_{BDND}$	BGND to AY, BY, All operating Modes: 20 kHz	–50				
	400 kHz	–50				
	800 kHz	-50				
	2 MHz	–50				
Crosstalk between lines	Xtalk fc=100 kHz, Vout=2Vpp	70	80		dB	1., 2.
	fc=2208 kHz, Vout=2Vpp	50	60			
$V_{IN, DWN}$	Input Amplitude, AC coupled			1.0	V	
Iout, max	Iout max into 100 ohm load			95	mA	
Logic Inputs (Pdown1, Pdown2, DISCON1 and DISCON2)						
V_{IH}	Logic 1, High level Input voltage	2		VCC	V	
V_{IL}	Logic 0, Low level Input voltage	AGND		0.8		
I_{IH}	Pdown = VCC			100	µA	
I_{IL}	Pdown = AGND			-100		
I_{IH}	DISCON = VCC			100		
I_{IL}	DISCON = AGND			-100		
Device Performance						
S_R	Slew Rate at $V_{AY–BY}$	250	300		V/µs	
HD2	fc=1MHz, RL=100Ohms, Vout=2Vp-p		-70		dBc	3.
HD3	fc=1MHz, RL=100Ohms, Vout=2Vp-p		-70		dBc	
MTPR	Downstream multitone power ratio ITU, G.992.1 MTPR test peak to rms ratio = 5.8		70		dB	
K_{DWN}	$K_{DWN} = V_{AY,BY}/V_{DWN}$ 25 kHz to 2208 kHz	46	48	50	V/V	
K_{DWN} vs. frequency	-3 dB	5			MHz	

Table 2. Pdown = 1 (Power Down)

Specification	Condition	Min	Typ	Max	Unit	Note
AC Characteristics						
Vn_{DWN}	Output Differential Noise Voltage, at (AY, BY) V_{TX}=0 V, 25 kHz to 1104 kHz		0.6	1.0	$\frac{\mu V}{\sqrt{Hz}}$	
R_{DDWN}	Differential Input Impedance DDWNP to DDWNN	28k	40k	52k	kΩ	
V_{AYDC}, V_{BYDC}	AY, BY DC bias voltage	$\frac{V_{BAT}}{2} - 0.25$	$\frac{V_{BAT}}{2} + 0.75$	$\frac{V_{BAT}}{2} + 1.75$	V	
Crosstalk between lines	Xtalk fc=100 kHz, Vout=2Vpp	70	80		dB	1., 2.
	fc=1104 kHz, Vout=2Vpp	50	60			
$V_{IN, DWN}$	Input Amplitude, AC coupled			1.0	V	
Iout, max	Iout max into 100 ohm load			80	mA	
Device Performance						
S_R	Slew Rate at $V_{AY–BY}$	200	250		V/µs	
HD2	fc=1MHz, RL=100Ohms, Vout=2Vp-p		-67.5		dBc	3.
HD3	fc=1MHz, RL=100Ohms, Vout=2Vp-p		-67.5		dBc	
MTPR	Downstream multitone power ratio ITU, G.992.1 MTPR test peak to rms ratio = 5.8		67.5		dB	
K_{DWN}	$K_{DWN} = V_{AY,BY}/V_{DWN}$ 25 kHz to 1104 kHz	46	48	50	V/V	
K_{DWN} vs. frequency	-3 dB	4			MHz	

Notes:

1. *Crosstalk is measured with one line transmitting signal, the other line is enabled but V_{TX} is set to 0 V.*
2. *Crosstalk:* $\text{Xtalk(dB)} = 20\log\left(\frac{V_{(AY, BY)1}}{V_{(AY, BY)2}}\right)$
3. *Measured with a 2.45:1 transformer and a 100-Ω load.*

APPLICATION CIRCUIT

Refer to the datapath reference design.

PCB Layout

The Le87220 device contains high gain and high bandwidth amplifiers. The amplifier inputs of each line are connected to the DDWNP/DDWNN pins, the output are connected to the AY and BY pins. To prevent coupling of the high level output signals into the low level DDWNP/DDWNN pins, PCB tracks and components connected to AY, BY, and going to the TIP (A) and RING (B) terminals must be well separated from tracks connected to DDWNP/DDWNN pins. The components C1, C2, R1, R10, and R11 (and the corresponding components of line 2) should be as close as practical to DDWNP/DDWNN pins. The Le87220 device provides an analog ground pin (AGND) as a return for low level currents and a battery ground pin (BGND) as a return for high level currents.

The differential drivers of the Le87220 device do not produce any load current into the AGND leads, but the amplifier currents are still circulating in the VBAT and BGND pins. A bypass capacitor between VBAT and BGND is required to be close to the device. AGND and BGND tracks should only be tied together at a single point, close to the power connector of the card.

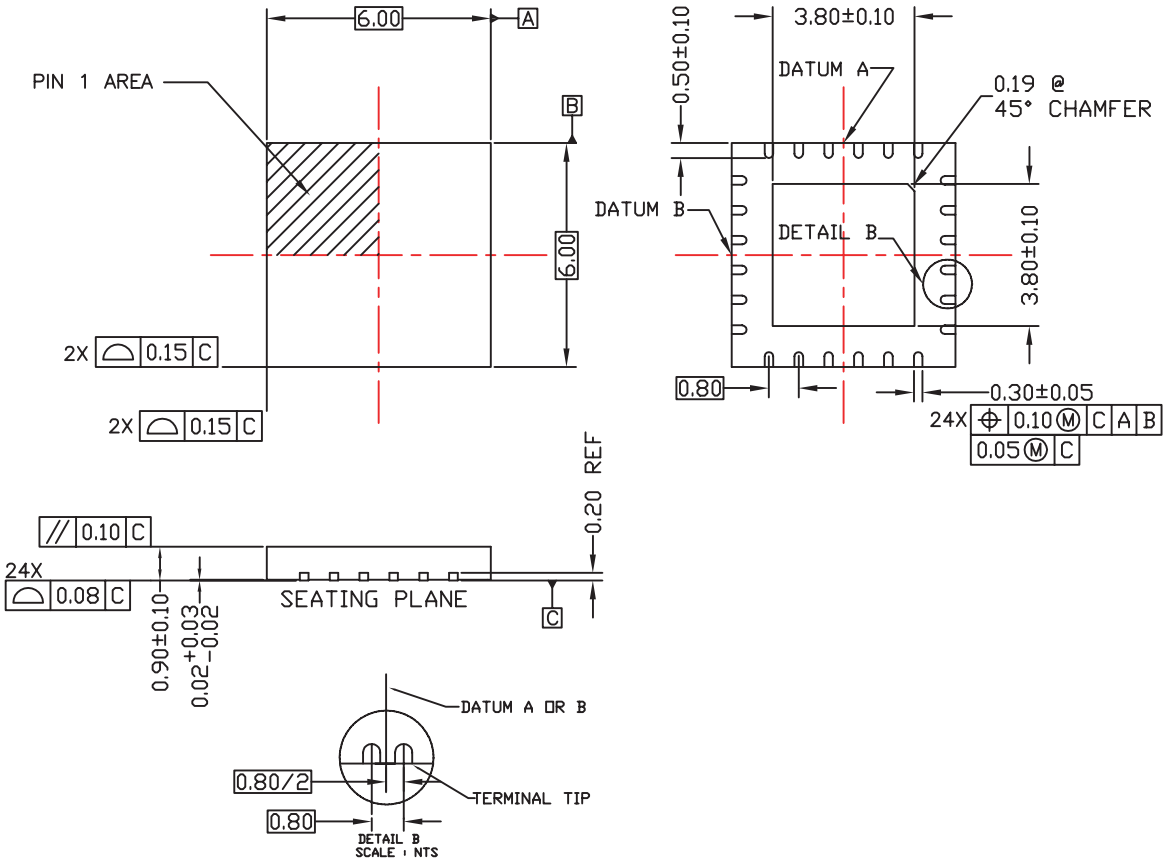
The Le87220 device uses a thermally enhanced package equipped with an exposed pad on the bottom side. The printed circuit board surface must have a copper pad covering the full surface of the thermal pad. The copper pad must be fitted with a minimum of 16 thermal transfer vias on a 1 mm pitch with a via diameter of 0.3 to 0.33 mm, and be connected to a large internal copper plane for proper heat dissipation. The AGND plane is recommended. The thermal transfer vias should be connected to the thermal pad and to the AGND plane without thermal relieve tracks. The AGND plane should be the second layer from the top of the PCB for the best power dissipation.

In multi-line applications, the Le87220 devices must be positioned in the layout to ensure a minimum distance of 1 inch (center to center) between devices. Passive non-heat producing components can be placed between the Le87220 devices.

PHYSICAL DIMENSIONS

24-Pin QFN

24 Lead QFN with Chamfer



Symbol	24 LEAD QFN		
	Min	Nom	Max
A	0.80	0.90	1.00
A2		0.57 REF	
b	0.18	0.23	0.38
D		6.00 BSC	
D2	3.70	3.80	3.90
E		6.00 BSC	
E2	3.70	3.80	3.90
e		0.80 BSC	
L	0.30	0.40	0.50
N		24	
A1	0.00	0.02	0.05
A3		0.20 REF	
aaa		0.15	
bbb		0.10	
ccc		0.10	

NOTES:
1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. ⌖ is in degrees.
3. N is the total number of terminals.
4. The Terminal #1 identifier and terminal numbering convention shall conform to JEP 95-1 and SSP-012. Details of the Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
5. Coplanarity applies to the exposed pad as well as the terminals.
6. Reference Document: JEDEC MO-220.
7. Lead width deviates from the JEDEC MO-220 standard.

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

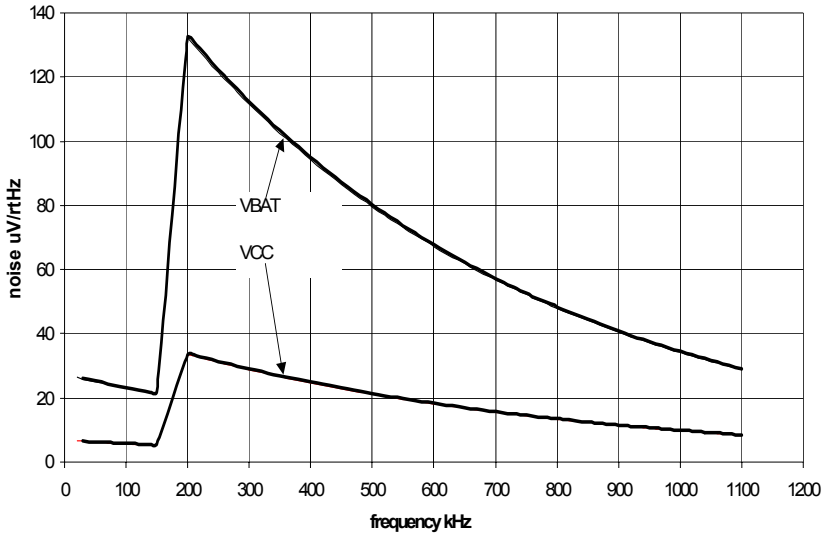
DEVICE OPERATIONAL NOTES

Power Supplies

The Le87220 device is implemented in a high-voltage process that allows direct powering from the –42 V to –72 V battery supply without the need for DC to DC converters. This saves significant power that would otherwise be wasted in the DC to DC converter.

The noise on (referenced to AGND) the battery supply (VBAT pin) and on the +3.3 V supply (VCC pin) should be below the limits as shown in Figure 1, in order not to affect the data performance.

Figure 1. Allowed Noise on Power Supply Pins (Referenced to AGND)



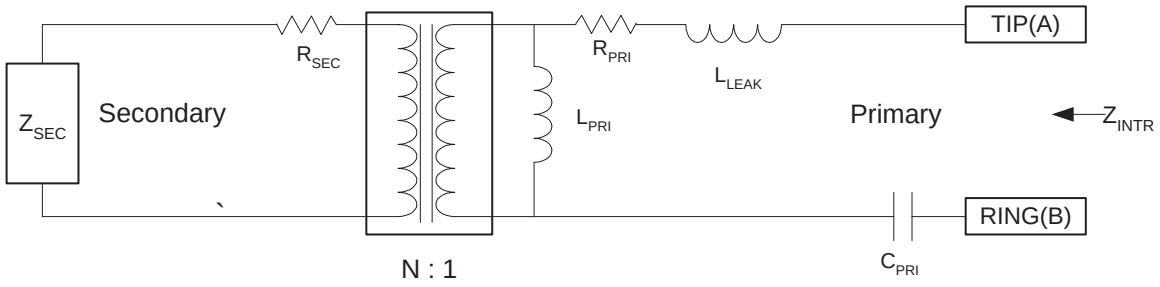
Line Transformer

A step-down transformer is used to interface the Le87220 device with the TIP (A) and RING (B) line terminals. The transformer injects the data signal onto the loop and provides dielectric isolation and impedance matching between the loop and the line driver. The turn ratio of the transformer can be optimized to match the loop signal level to the driver output swing (see *Transformer Turns Ratio*, on page 11).

Transformer Specifics

Figure 2 represents a simplified transformer model in which the boxed block is an ideal transformer with an infinite bandwidth.

Figure 2. Le87220 Transformer



Transformer Turns Ratio

The transformer turns ratio N is restricted by the maximum peak differential signal at AY/BY pins, which must stay within the Le87220 device's dynamic range. The output voltage range is typically equal to $|V_{BATmin}| - 4$ V.

The maximum peak voltage (across 100 Ω at TIP (A) and RING (B) leads of a FDM ADSL signal using 224 downstream carriers for a combined rms power of 19.85 dBm and a peak-to-rms ratio of 5.8) is 36.05 V_{PP} differential. To account for the voltage drop across Z_{SEC}, this voltage must be scaled up by a factor of 1.086. The required peak differential signal at the AY/BY pins would be 39.15 V_{PP} or 19.6 V_{PP} per driver if the transformer had a 1:1 turn ratio. Using this information the transformer turns ratio can be calculated as

$$N = \frac{|V_{BAT}| - 4V}{19.6V}.$$

The transformer turns ratio for a nominal battery voltage of –52 V is then **N=2.45:1**.

The Le87220 device is designed to operate with battery voltage in the range of –42 V to –72 V. The data transformer turns ratio can be optimized for the specific battery voltage range, but the turns ratio must be limited to less than 2.7:1 secondary to primary (where the primary side is connected to TIP (A) and RING (B)) if 19.85 dBm needs to be produced at the output. This limitation is imposed by the Le87220 device internal bias levels.

Downstream Filtering

The input differential impedance (R_{DDWN}) of the DDWNP/DDWNN pins can vary by as much as ± 30%, and consequently a lower value external resistor R_1 is used to set the differential input impedance (refer to the data path reference design).

A high-pass filter with a –3 dB corner frequency of

$$f_{DWNHPF} = \frac{1}{2\pi R_{IN} C_{IN}}$$

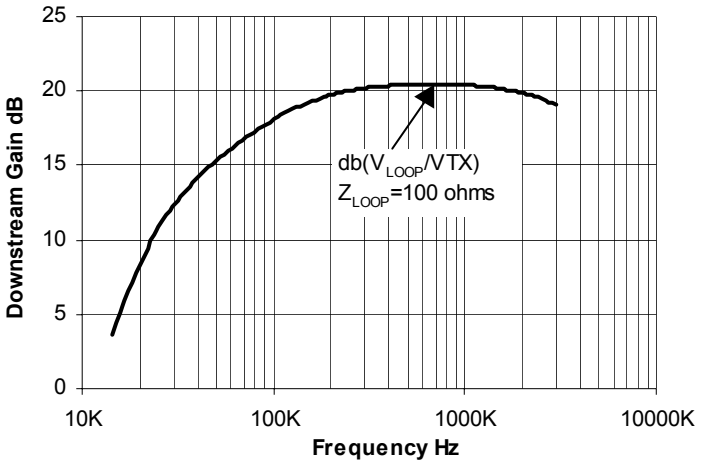
is formed by C_1 and C_2 in conjunction with R_{IN} to attenuate the low frequency noise of the downstream signal where

$$R_{IN} = R_{10} + R_{11} + (R_1 \,||\, R_{DDWN})$$

$$C_{IN} = \frac{C_1 \cdot C_2}{C_1 + C_2}.$$

In addition to rejecting the low frequency signals from the data AFE, the input capacitors also block DC currents from flowing between DDWNP/DDWNN and the data AFE outputs. With the recommended R_1 value of 5.49 kΩ, $R_{10} = R_{11}$ = 2.67 kΩ and $C_1 = C_2$ = 1.5 nF provides a corner frequency of around 25 kHz. Resistors R_{10}, R_{11} and R_1 can be used to adjust the downstream signal level.

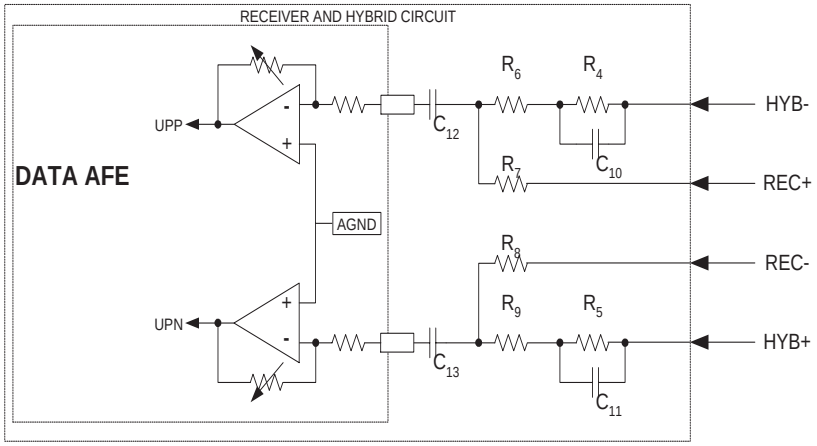
Figure 3. Downstream Gain of the *Application Circuit*, on page 8



RECEIVER AND HYBRID CIRCUIT

The receive and hybrid circuit architecture depends greatly on the data AFE being used in the design. Some data AFEs have built-in input differential amplifiers for the receive circuits. These amplifiers should be used to implement the receive and hybrid functions. If the AFE does not have such amplifiers, then external low noise amplifiers are required to implement these functions. Figure 4 shows a typical implementation of the receive and hybrid functions.

Figure 4. Receive and Hybrid Circuit



COMPONENTS SELECTION

The DC blocking capacitor C_6 is required on the primary or line side of the transformer in order to avoid applying a DC short across TIP (A) and RING (B) terminals. The value of the line side capacitor depends on transformer primary inductance chosen to give desired –3 dB high pass point. According to T1.413, the impedance measured across TIP (A) and RING (B) at 4 kHz must be greater than 1100 Ω, which requires a capacitance of less than 35 nF for the series combination of C_6 and any external DC blocking capacitor.

The minimum transformer primary inductance required is dictated by the low end of the upstream frequency band, which is typically around 25-30 kHz. Since the transformer primary inductance shunts the line, it should be relatively high to avoid signal attenuation and maintain an acceptable match across the desired bandwidth. A high impedance can be obtained by using a transformer with a high primary side inductance while maintaining relatively low DC resistance for minimum insertion loss. Besides using it for its isolation and high common-mode rejection it is also used as part of the high-pass splitter function.
If the -3 dB point is chosen to be around 20 kHz, the minimum primary (line side) inductance required would be

$$L_{PRI} = \frac{|Z_{LOOP}|}{2\pi(20\ \text{kHz})} = \frac{100}{2\pi(20\ \text{kHz})} \approx 796\ \mu\text{H}\ .$$

For the Le87220 device, a transformer primary side inductance of >800 µH is recommended

REVISION HISTORY

Revision A1 to B1

- Removed 8 x 8 QFN package data

Revision B1 to C1

- Added OPN for green package in *Ordering Information*, on page 1
- Added column and note to *Ordering Information*, on page 1 to indicate packing system
- Revised 24-lead QFN drawing in *Physical Dimensions*, on page 9 to show chamfer

Revision C1 to C2

- Enhanced format of package drawing in *Physical Dimensions*, on page 9
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at

www.zarlink.com