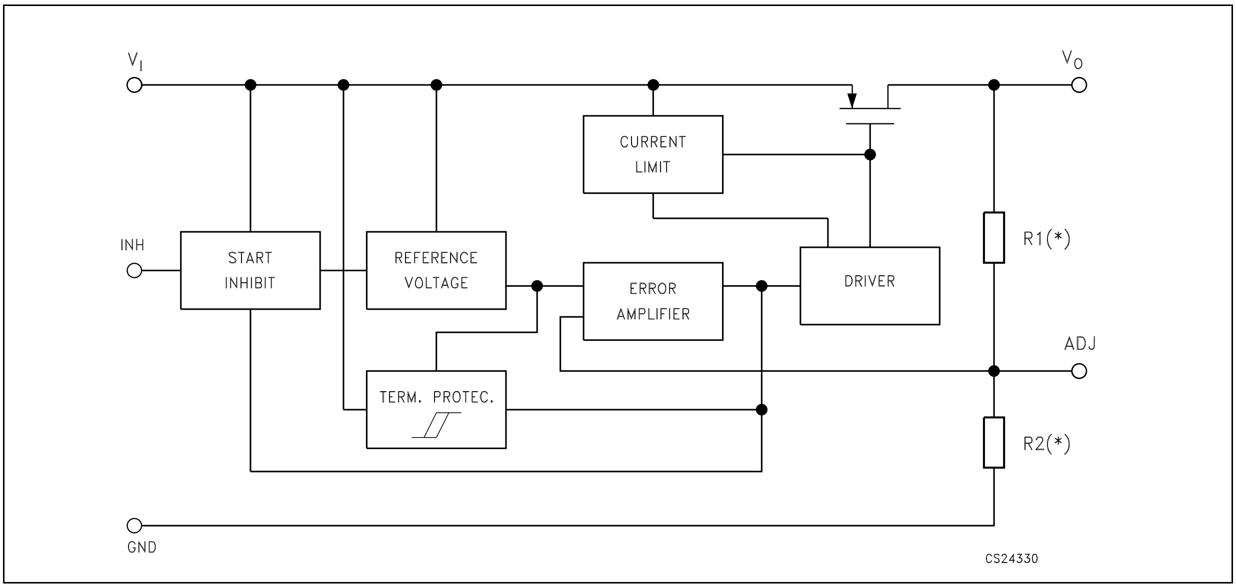
Contents

1 Diagram

Figure 1. Block diagram



(*) Not present on ADJ versions

2 Pin configuration

Figure 2. Pin connections (top view for DPAK and PPAK)

PPAK **DPAK**

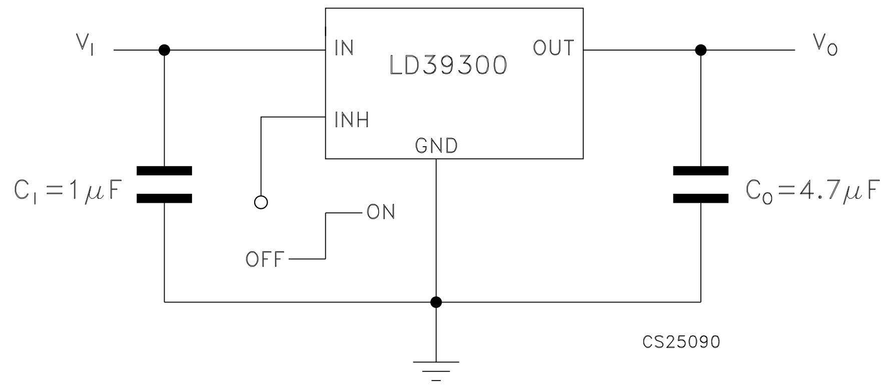
Table 2. Pin description

PIn N°		Symbol	Note
PPAK	DPAK		
5		V_{SENSE}/N.C.	For fixed versions: Not Connected on PPAK
		ADJ	For adjustable version: Error Amplifier Input pin for V_O from 1.22 to 5.0V
2	1	V_I	LDO Input Voltage; V_I from 2.5V to 6V, C_I=1µF must be located at a distance of not more than 0.5'' from input pin.
4	3	V_O	LDO Output Voltage pins, with minimum C_O=4.7µF needed for stability (also refer to C_O vs. ESR stability chart)
1		V_{INH}	Inhibit Input Voltage: ON MODE when $V_{INH} \geq 2V$, OFF MODE when $V_{INH} \leq 0.3V$ (Do not leave floating, not internally pulled down/up)
3	2	GND	Common ground
TAB		GND	Tab is connected to GND

3 Typical application circuits

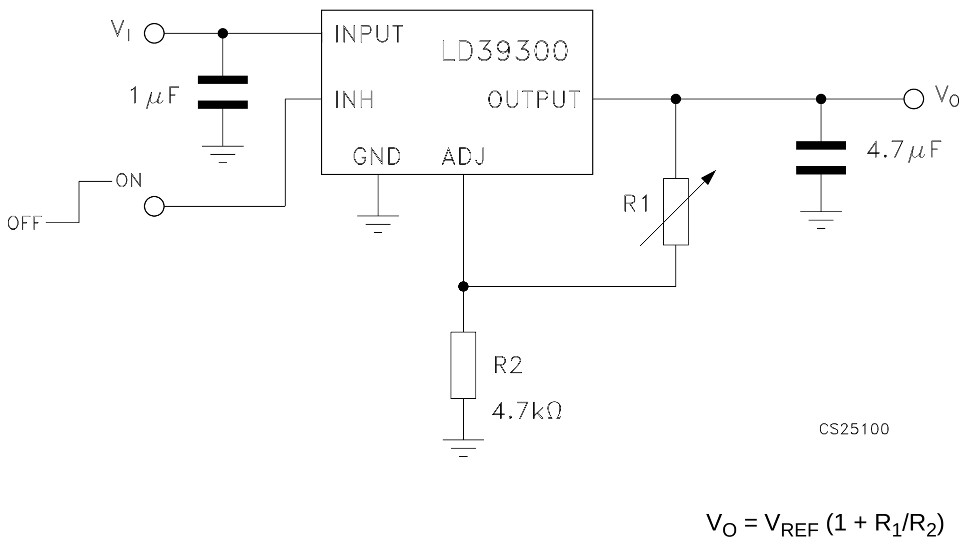
C_I and C_O Capacitors must be placed as close as possible to the IC pins.

Figure 3. LD39300 fixed version with inhibit



1 *Inhibit Pin is not internally pulled down/up then it must not be left floating. Disable the device when connected to GND or to a positive voltage less than 0.3 V*

Figure 4. LD39300 adjustable version



2 *Set R2 as close as possible to 4.7 KΩ*

Figure 5. LD39300 DPAK

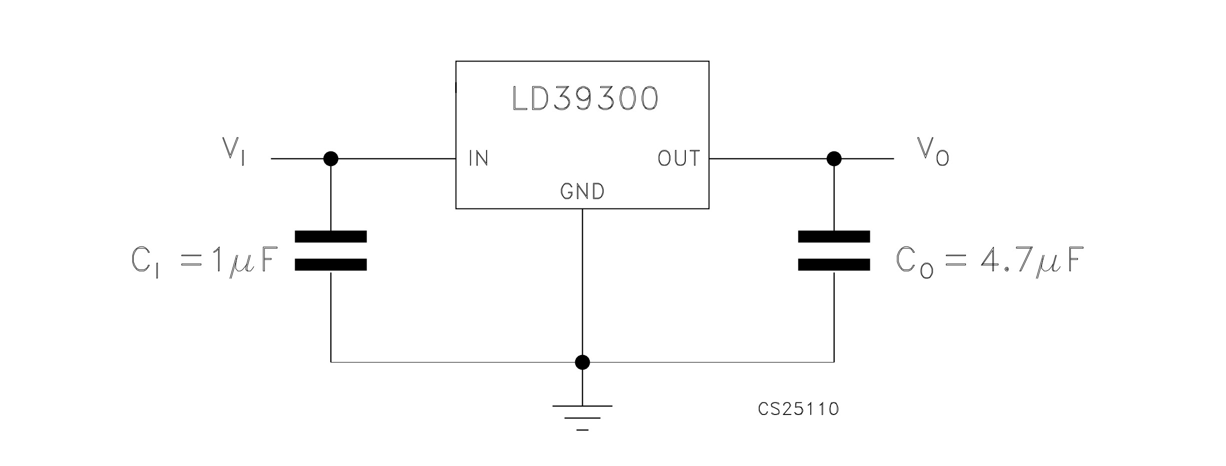
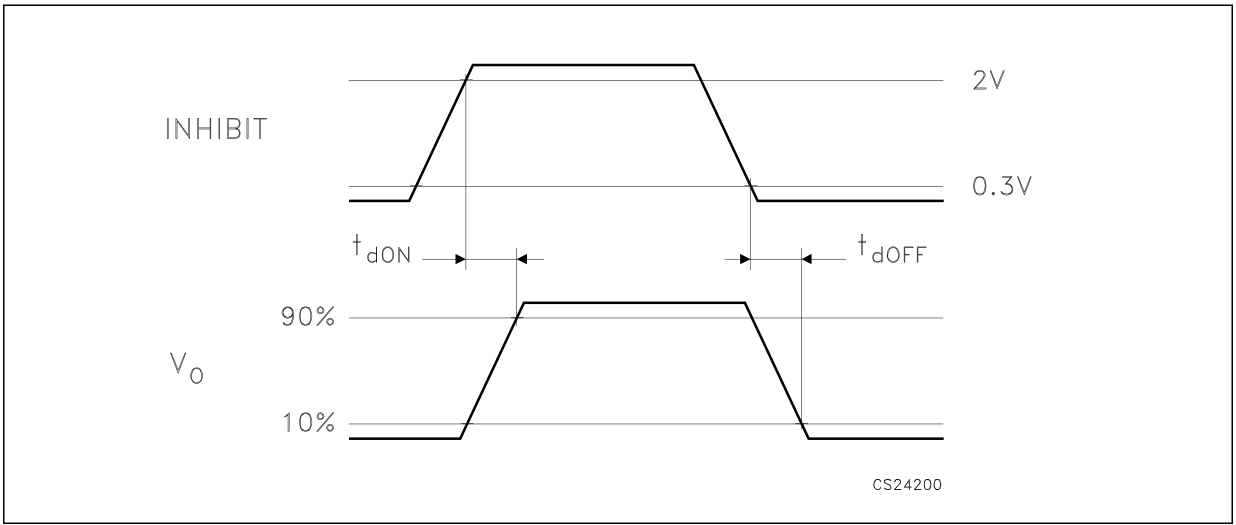


Figure 6. Timing diagram



4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	-0.3 to 6.5	V
V_{INH}	INHIBIT input voltage	-0.3 to V_I +0.3 (6.5V max)	V
V_O	DC output voltage	-0.3 to V_I +0.3 (6.5V max)	V
V_{ADJ}	ADJ pin voltage	-0.3 to V_I +0.3 (6.5V max)	V
I_O	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	-50 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	PPAK	DPAK	Unit
R_{thJA}	Thermal resistance junction-ambient	100	100	°C/W
R_{thJC}	Thermal resistance junction-case	8	8	°C/W

5 Electrical characteristics

T_J = 25°C, V_I = V_O+1 V, C_I = 1 µF, C_O = 4.7 µF, I_{LOAD} = 10 mA, V_{INH} = 2 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Parameter	Min.	Typ.	Max.	Unit
V_I	Operating input voltage		2.5		6	V
V_O	Output voltage tolerance	V_I = V_O+1V, I_{LOAD} = 10mA to 3A	-1.5		1.5	% of $V_{O(NOM)}$
		V_I = V_O+1V to 6V, I_{LOAD} = 10mA to 3A T_J = -40 to 125°C	-3		3	
V_{REF}	Reference voltage			1.22		V
ΔV_O	Output voltage LINE regulation	V_I = V_O+1V to 6V		0.04		%
		V_I = V_O+1V to 6V, T_J = -40 to 125°C		0.1	0.2	%
$\Delta V_O/\Delta I_{LOAD}$	Output voltage LOAD regulation	I_{LOAD} = 10mA to 3A		0.06		%/A
		I_{LOAD} = 10mA to 3A, T_J = -40 to 125°C		0.2	0.4	
V_{DROP}	Dropout voltage (V_I - V_O)	I_{LOAD} = 600mA, T_J=-40 to 125°C		40	80	mV
		I_{LOAD} = 3A, T_J = -40 to 125°C		200	400	
I_Q	Quiescent current: ON MODE	I_{LOAD} = 10mA to 3A, V_{INH} = 2V T_J = -40 to 125°C		1.2	2.5	mA
	Quiescent current: OFF MODE	V_{INH} = 0.3V			1	µA
		V_{INH} = 0.3V, T_J = -40 to 125°C			5	
Short Circuit Protection						
I_{SC}	Short circuit protection	R_L = 0		6		A
Inhibit Input						
V_{INH}	Inhibit threshold LOW	V_I = 2.5 to 6V OFF T_J = -40 to 125°C			0.3	V
	Inhibit threshold HIGH		2			
T_{D-OFF}	Current limit	I_{LOAD} = 3A, V_O = 3.3V		20		µs
T_{D-ON}	Current limit	I_{LOAD} = 3A, V_O = 3.3V		20		
I_{INH}	Inhibit input current (1)	V_I = 6V, V_{INH} = 0 to 6V		±0.1	±1	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Parameter		Min.	Typ.	Max.	Unit
AC Parameters							
SVR	Supply voltage rejection	$V_I = 4.5 \pm 1V$, $V_O = 3.3V$, $I_{LOAD} = 10mA$,	f = 120Hz		65		dB
			f = 1kHz		55		
e_N	Output noise voltage	B_W = 10Hz to 100kHz, $C_O = 4.7\mu F$, $V_O = 2.5V$			100		μV_{RMS}
T_{SHDN}	Thermal shutdown OFF				170		°C
	Hysteresis				10		

1. Guaranteed by design

6 Typical performance characteristics

(T_J = 25°C, V_I = V_O+1V, C_I = 1µF, C_O = 4.7µF, I_{LOAD} = 10mA, V_{INH} = V_I, unless otherwise specified)

Figure 7. Output voltage vs temperature

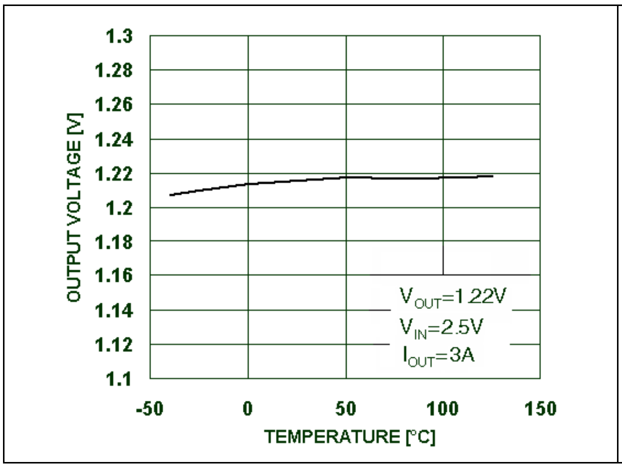


Figure 8. Dropout voltage vs temperature

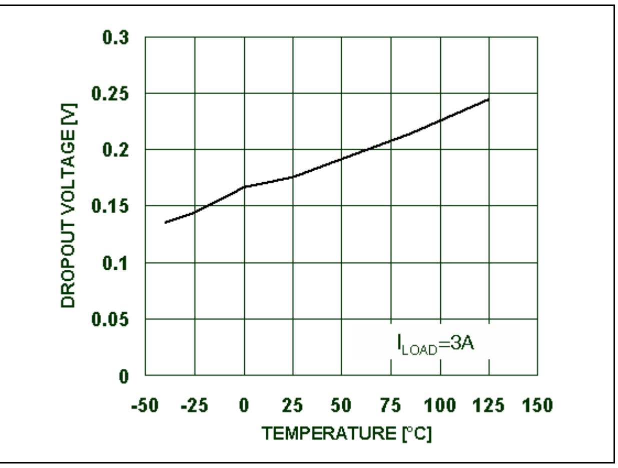


Figure 9. Dropout voltage vs output current

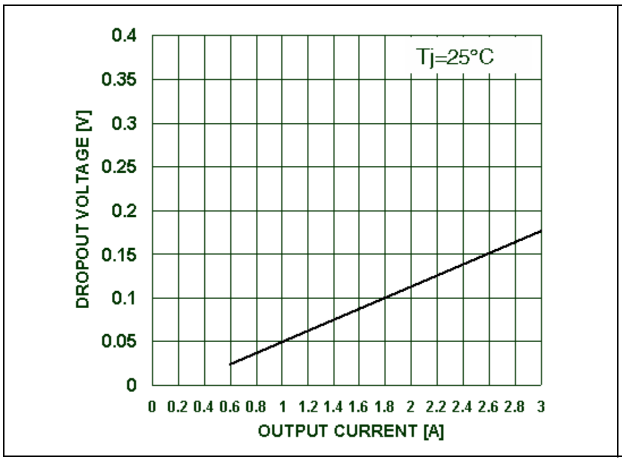


Figure 10. Quiescent current vs temperature (I_{out} = 10 mA)

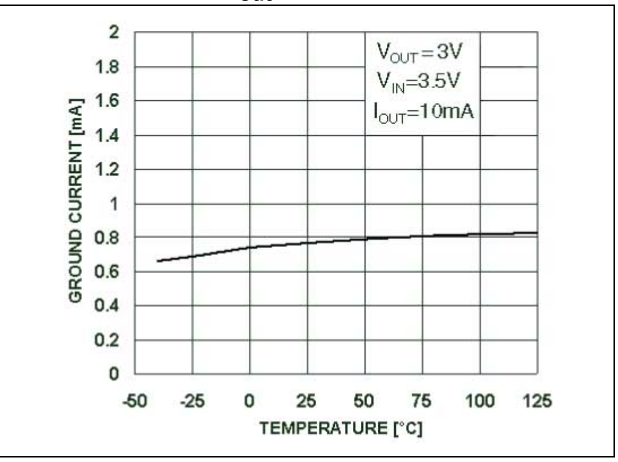


Figure 11. Quiescent current vs temperature (I_{out} = 3 A)

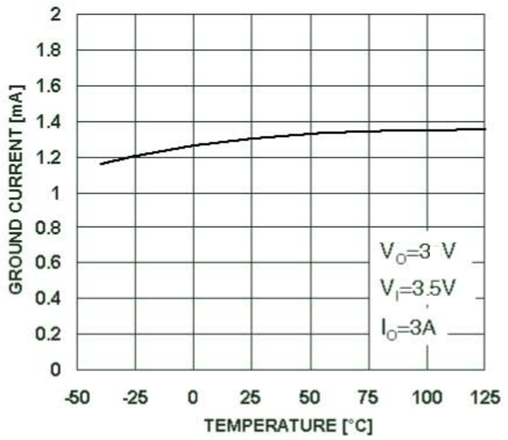


Figure 12. Short circuit current vs temperature

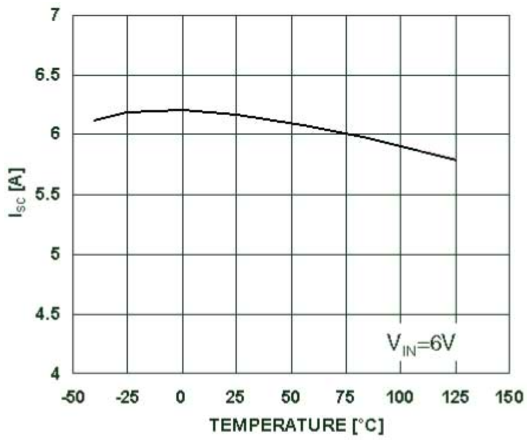


Figure 13. Output voltage vs input voltage

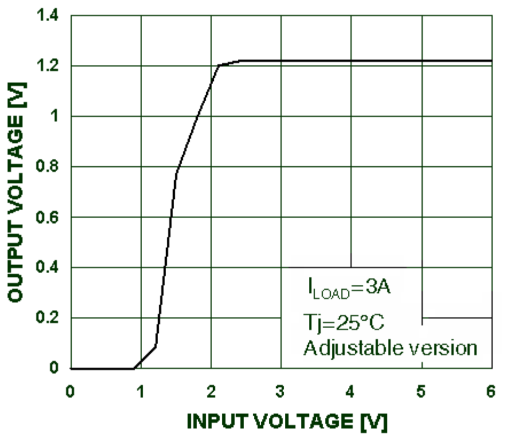


Figure 14. Stability region vs C_O & ESR

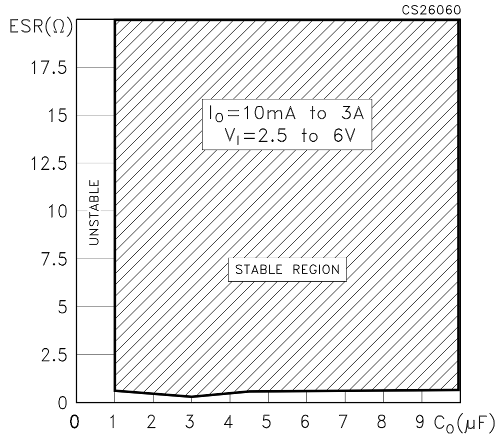


Figure 15. Stability region vs C_O & ESR (low ESR zoom area)

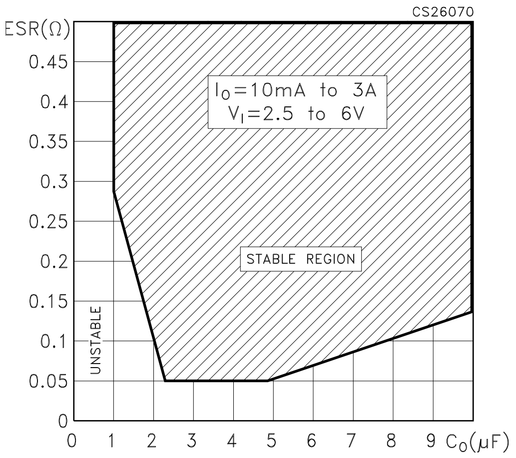
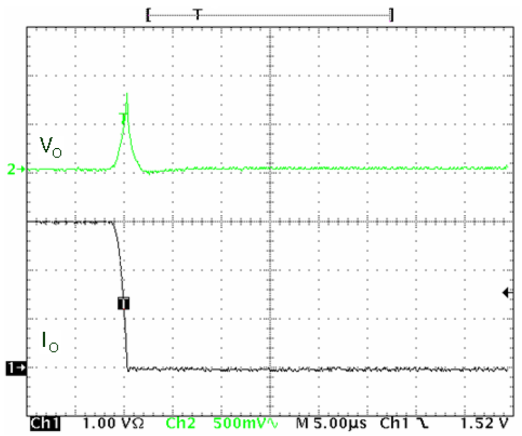
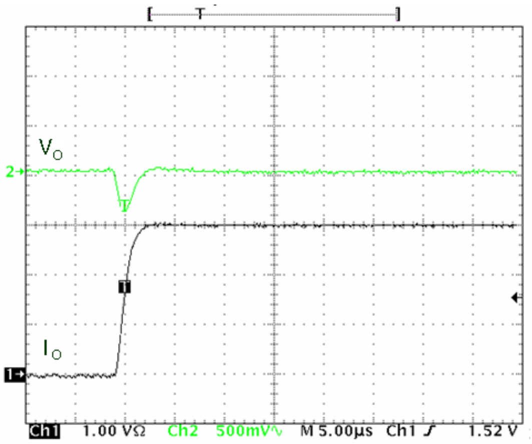


Figure 16. Load transient (fall time)



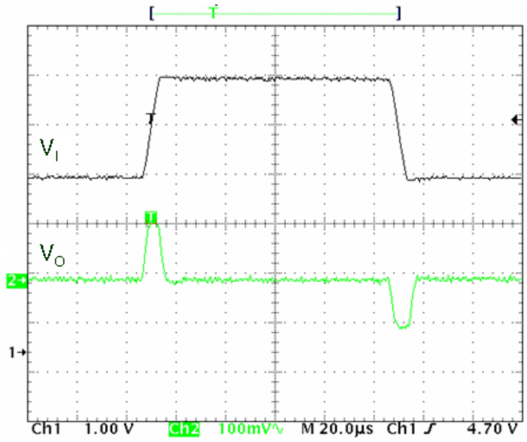
V_I = 5V, V_O = 3.3V, I_O = 10mA to 3A, C_I = 1µF, C_O = 4.7µF

Figure 17. Load transient (rise time)



V_I = 5V, V_O = 3.3V, I_O = 10mA to 3A, C_I = 1µF, C_O = 4.7µF

Figure 18. Line transient



V_I = 3.5V to 5.5V, V_O = 3.3V, I_{LOAD} = 10mA, C_O = 4.7µF

7 Application notes

7.1 External capacitors

The LD39300 requires external capacitors for regulator stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance (see *Figure 14.*and *Figure 15.*). The input/output capacitors must be located less than 1cm from the relative pins and connected directly to the input/output ground pins using traces which have no other currents flowing through them. Any good quality of Ceramic or Electrolytic capacitors can be used.

7.2 Input capacitor

An input capacitor whose minimum value is 1 µF is required with the LD39300 (amount of capacitance can be increased without limit). This capacitor must be located a distance of not more than 1 cm from the input pin of the device and returned to a clean analog ground. Any good quality ceramic, tantalum or film capacitors can be used for this capacitor.

7.3 Output capacitor

It is possible to use Ceramic or Tantalum capacitors but the output capacitor must meet the requirement for minimum amount of capacitance and E.S.R. (equivalent series resistance) value. A minimum capacitance of 4.7 µF is a good choice to guarantee the stability of the regulator. Anyway, other C_O values can be used according to the (*Figure 14.* and *Figure 15.*) showing the allowable ESR range as a function of the output capacitance. This curve represents the stability region over the full temperature and I_O range.

7.4 Thermal note

The output capacitor must maintain its ESR in the stable region over the full operating temperature range to assure stability. Also, capacitors tolerance and variation with temperature must be kept in consideration in order to assure the minimum amount of capacitance at all times.

7.5 Inhibit input operation

The inhibit pin can be used to turn OFF the regulator when pulled down, so drastically reducing the current consumption down to less than 1 µA. When the inhibit feature is not used, this pin must be tied to V_I to keep the regulator output ON at all times. To assure proper operation, the signal source used to drive the inhibit pin must be able to swing above and below the specified thresholds listed in the electrical characteristics section (V_{IH} V_{IL}). The inhibit pin must not be left floating because it is not internally pulled down/up.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 19. DPAK drawing

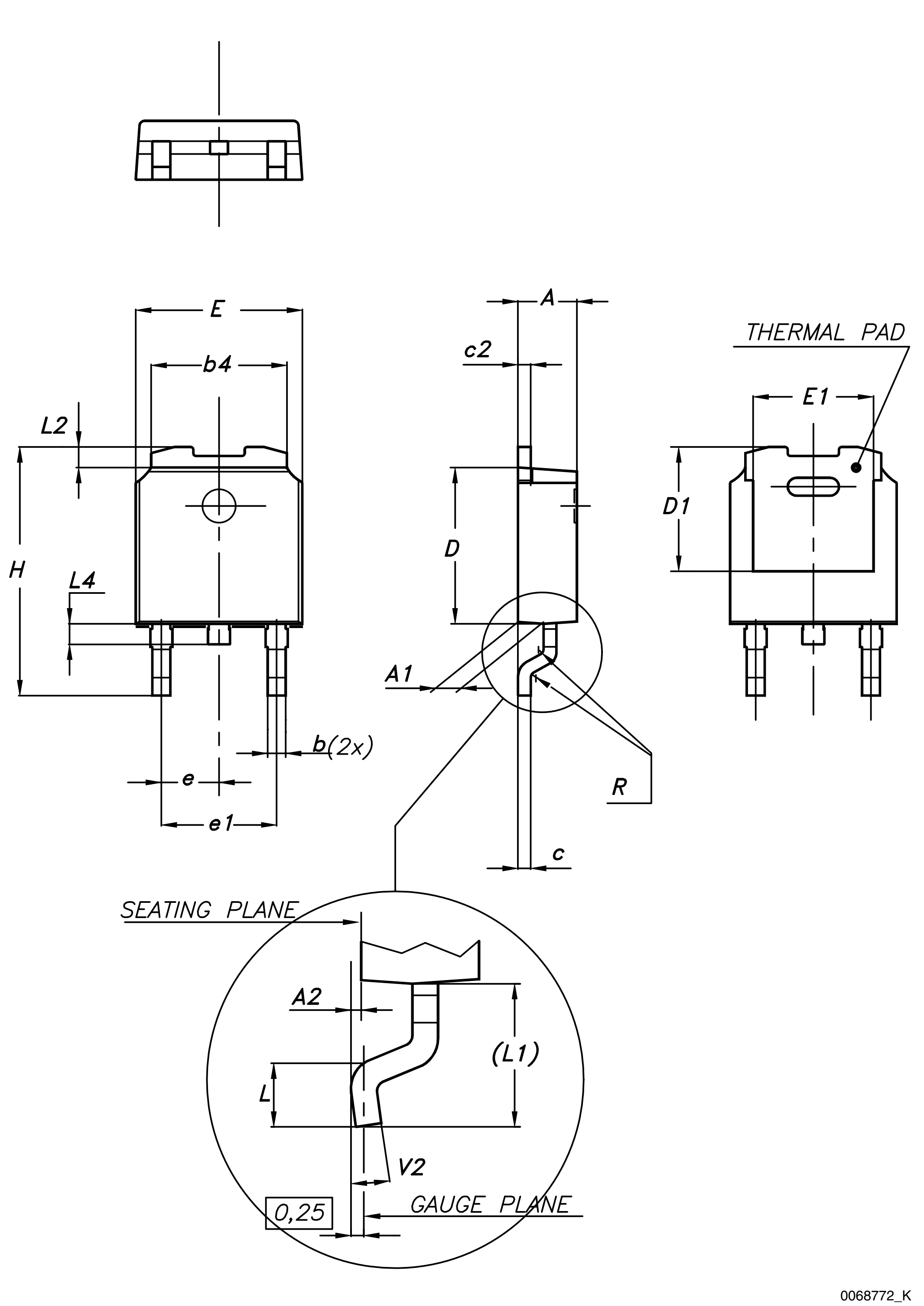
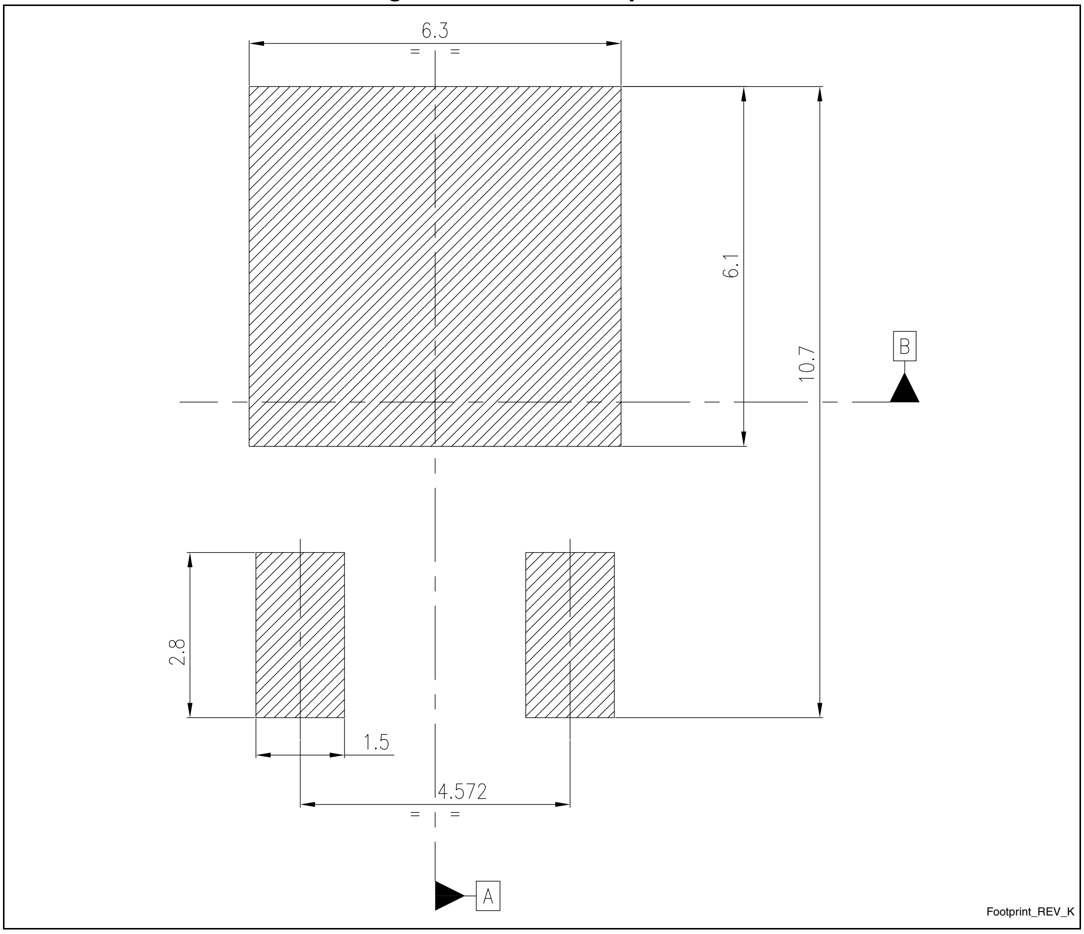


Table 6. DPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK footprint [(a)]



a. All dimensions are in millimeters.

Figure 21. PPAK drawing

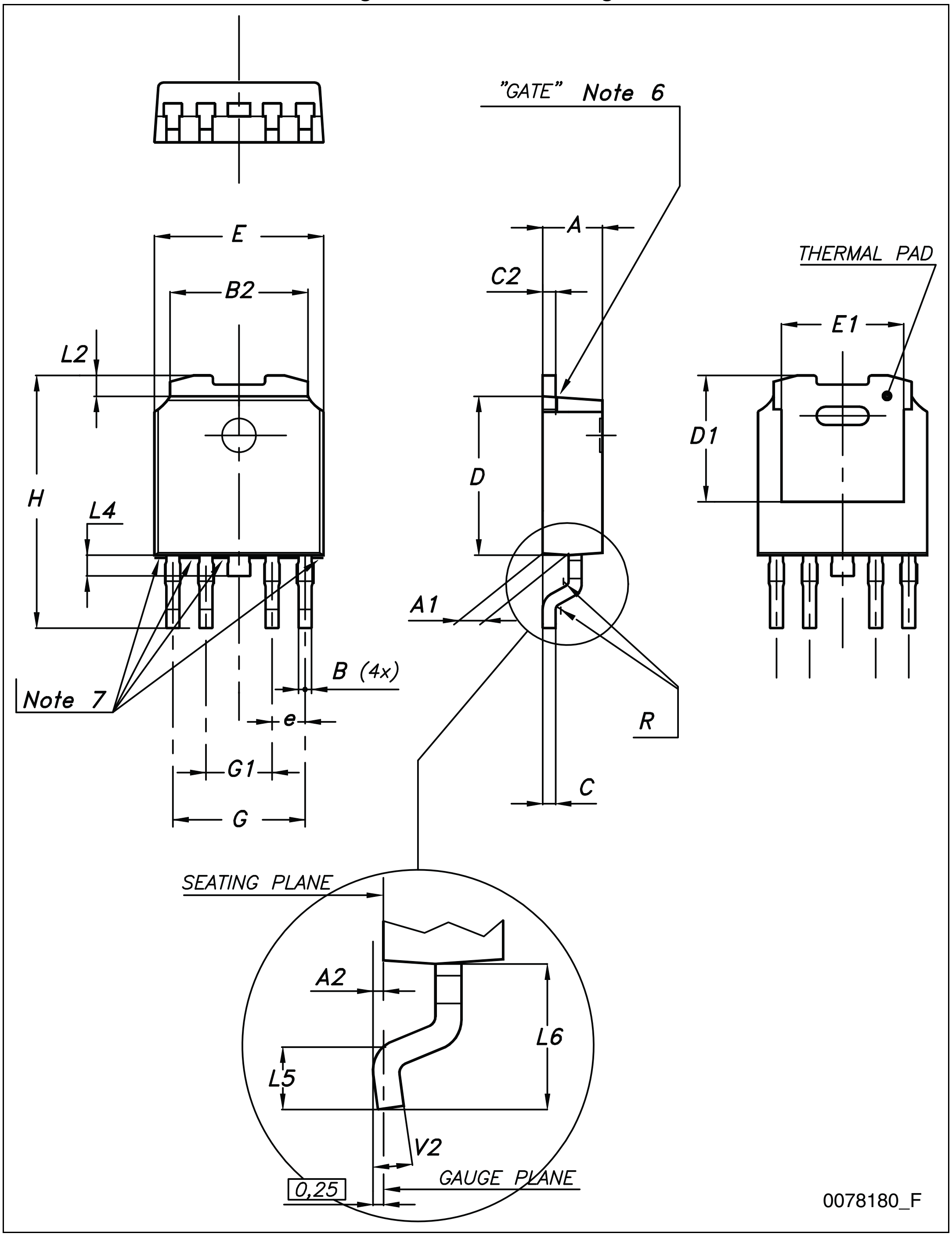


Table 7. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

9 Packaging mechanical data

Figure 22. PPAK and DPAK tape

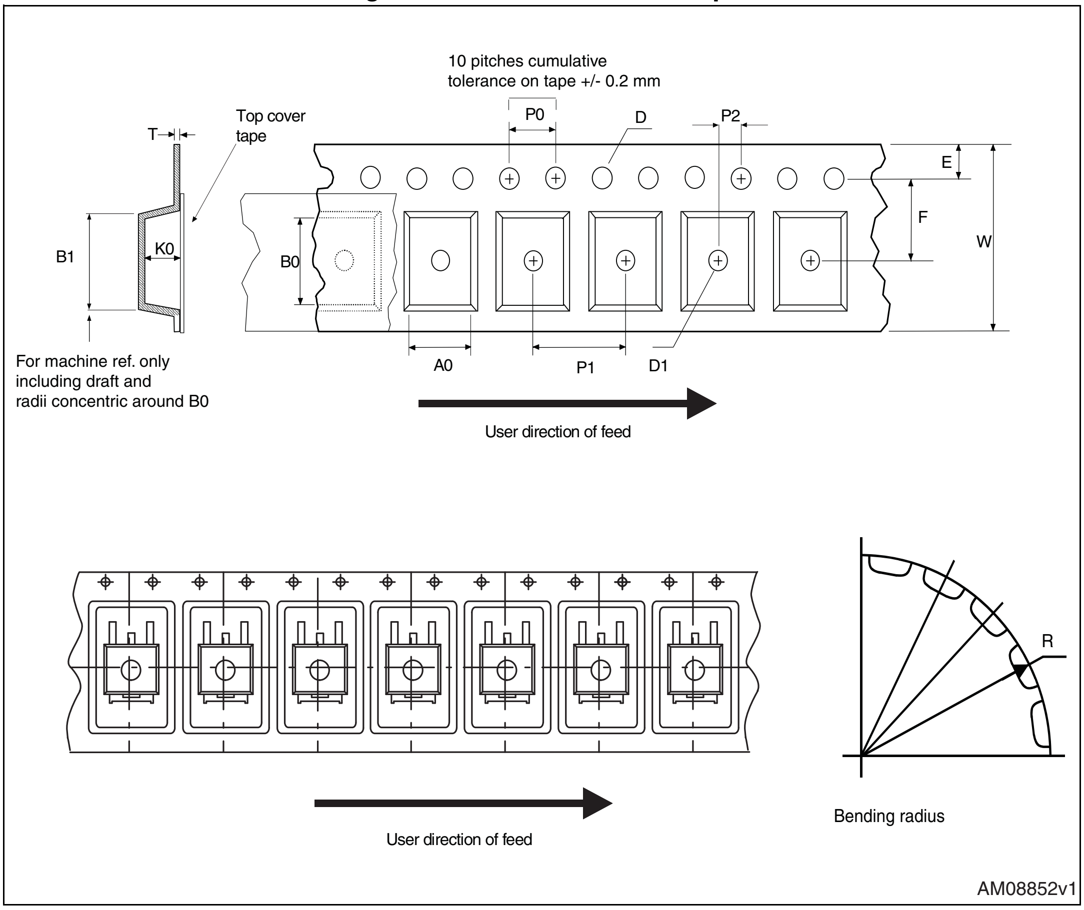


Figure 23. PPAK and DPAK reel

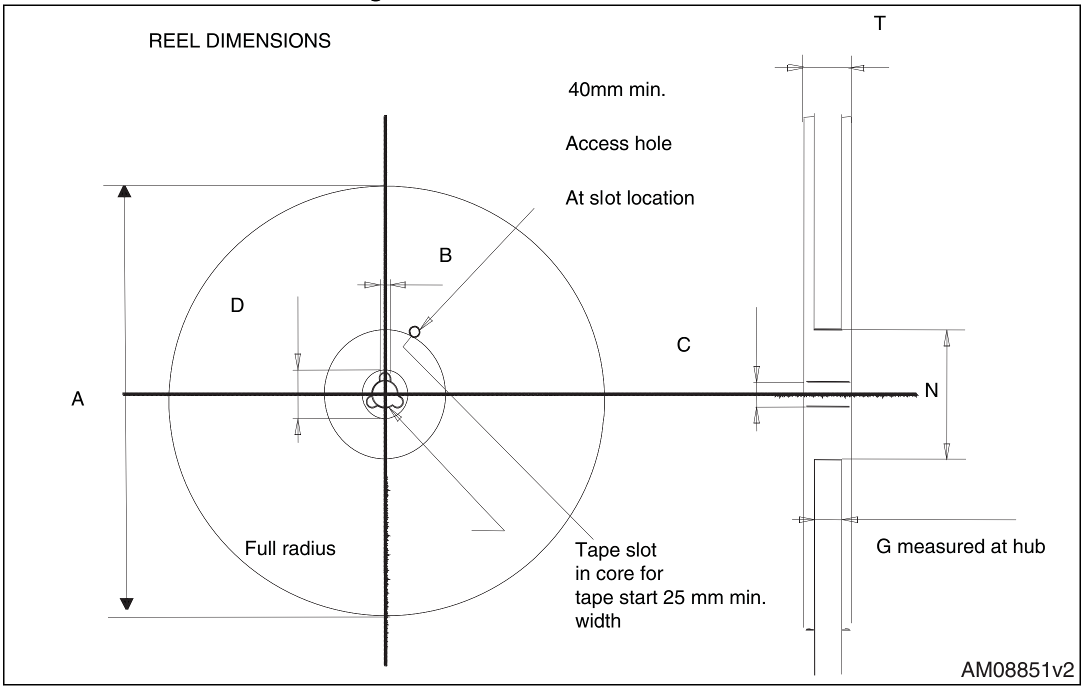


Table 8. PPAK and DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

10 Revision history

Table 9. Document revision history

Date	Revision	Changes
26-Jan-2007	1	Initial release.
04-Jun-2014	2	Updated *Table 1: Device summary*, *Table 2: Pin description* and *Section 8: Package mechanical data*. Added *Section 9: Packaging mechanical data*. Minor text changes.