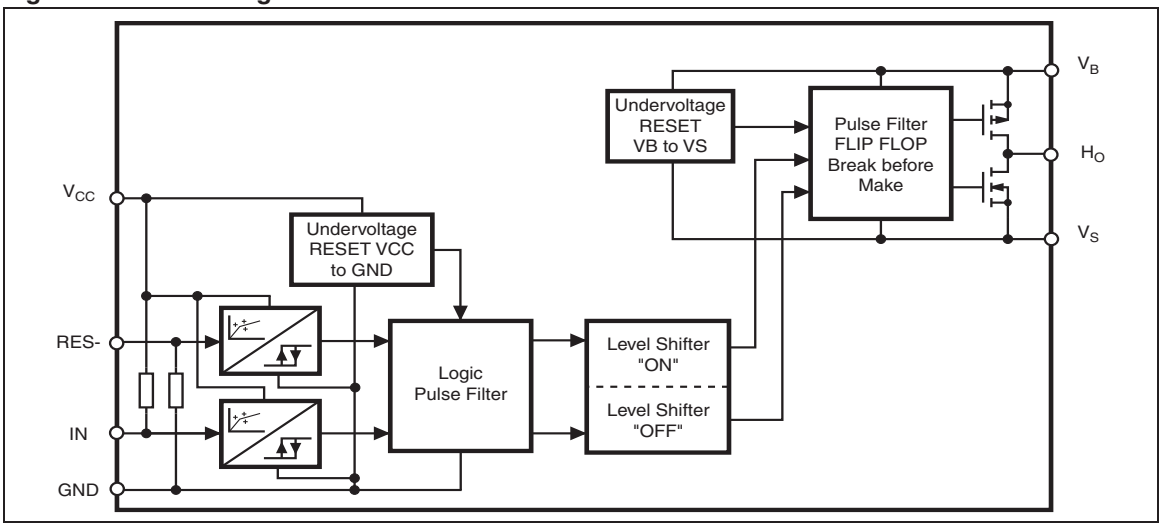
Content

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

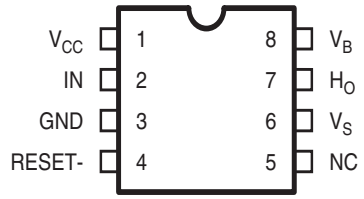


Table 2. Pin function

Pin #	Pin name	Description
1	V_{CC}	Driver supply, typically 17V
2	IN	Driver control signal input (positive logic)
3	GND	Ground
4	RESET-	Driver enable signal input (negative logic)
5	NC	No connection (no bondwire)
6	V_S	MOSFET source connection
7	H_O	MOSFET gate connection
8	V_B	Driver output stage supply

2 Electrical specifications

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
$R_{th(j\text{-}amb)}$	Thermal resistance junction-to-ambient	Max.	150	°C/W

2.2 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. This is a stress only rating and operation of the device at these or any conditions exceeding those indicated in the operational sections of this specifications is not implied.

Table 4. Absolute maximum ratings

Parameter		Value		Units
Symbol	Definition	Min.	Max.	
V_{BS}	High side floating supply voltage	-0.3	20	V
V_B	High side driver output stage voltage	-0.3	300	V
V_S	High side floating supply offset voltage	V_B – 20	300	V
VH_O	Output voltage gate connection	V_S - 0.3	V_B + 0.3	V
V_{CC}	Supply voltage	-0.3	20	V
V_{IN}	Input voltage	-0.3	V_{CC} + 0.3	V
I_{IN}	Input injection current. Full function, no latch-up; (guaranteed by design). Test at 10 V and 17 V on eng. samples.	-	+1	mA
V_{RES}	Reset input voltage	-0.3	V_{CC} + 0.3	V
V_{esd}	Electrostatic discharge voltage (human body model)	2k	-	V
V_{CDM}	Charge device model CDM, EOS/ESD ass. std 5.3. number of discharges per pin: 6	500	-	V
dV/dt	Allowable offset voltage slew rate	-50	50	V/nsec
T_j	Junction temperature	-55	150	°C
T_{stg}	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds) 3 times Bosch soldering profil acc. to Bosch soldering conditions, gen. spec.	-	300	

2.3 Recommended operating conditions

For proper operations the device should be used within the recommended conditions.

Table 5. Recommended operating conditions

Parameter		Value		Units
Symbol	Definition	Min.	Max.	
V_B	High side driver output stage voltage -5 V transient 0.1µs	VS+10 (1)	VS+18	V
V_S	High side floating supply offset voltage - 20 V transient 0.1µs	-5	300	V
V_{HO}	Output voltage gate connection	V_S	V_B	V
V_{CC}	Supply voltage	10	18	V
V_{IN}	Input voltage	0	V_{CC}	V
V_{RES}	Reset input voltage	0	V_{CC}	V
F_S	Switching frequency	-	200	kHz
T_{amb}	Ambient temperature	-40	125	°C

1. Reset-Logic functional for V_B-V_S=2V, independent from VCC-level

2.4 Electrical characteristics

Unless otherwise specified, V_{CC} = 15 V, V_{BS} = 15 V, V_S = 0 V, IN = 0 V, RES = 5 V, load R = 50 Ω, C = 2.5 nF. Unless otherwise noted, these specifications apply for an operating junction temperature range of -40 °C ≤ T_j ≤ 125 °C

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC} supply						
V_{CCUV}	V_{CC} supply undervoltage	V_{CC} rising from 0 V V_{CC} dropping from 10 V	7.2	-	9.6	V
$V_{CCUVHYS}$	V_{CC} supply undervoltage lockout hysteresis	-	0.02	0.2	0.4	V
td_{UVCC}	Undervoltage lockout response time	V_{CC} steps either from 10 V to 6 V or from 6 V to 10 V	0.5	-	20	µs
I_{QCC}	V_{CC} supply current	-	-	-	400	µA
V_{BS} supply						
V_{BSUV}	V_{BS} supply undervoltage	V_{BS} rising from 0 V V_{BS} dropping from 10 V	7.2	-	9.6	V
td_{UVBS}	Undervoltage lockout response time	V_{BS} steps either from 10 V to 6 V or from 6 V to 10 V	0.5	-	20	µs

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{BSUVHYS}$	V_{BS} supply undervoltage lockout hysteresis	-	0.02	0.2	0.4	V
I_{QBS1}	V_{BS} supply current	static mode, V_{BS} = 10 V, IN = 0 V or 5 V	-	-	100	µA
I_{QBS2}		static mode, V_{BS} = 18 V, IN = 0 V or V_{CC}	-	-	200	µA
ΔV_{BS}	V_{BS} drop due to output turn-on	V_{BS} = 17 V, C_{BS} = 1 µF, td_{IG-IN} = 3 µs, t_{TEST} = 100 µs	-	-	210	mV
Gate driver characteristics						
I_{PKSo1}	Peak output source current	V_{BS} = 10 V , T_j = 25 °C PW ≤ 10 µs	120	250	-	mA
I_{PKSo2}		V_{BS} = 10 V PW ≤ 10 µs	70	150	-	
I_{PKSo3}		V_{BS} = 17 V, T_j = 25 °C PW ≤ 10 µs	250	500	-	
I_{PKSo4}		V_{BS} = 17 V, PW ≤ 10 µs	150	300	-	
$I_{HOH,off}$	HOH off-state leakage current	Guaranteed by design	-	-	1	µA
t_{r1}	Output rise time	V_{BS} = 10 V, T_j = 25°C	-	0.2	0.4	µs
t_{r2}		V_{BS} = 10 V	-	0.3	0.5	
t_{r3}		V_{BS} = 17 V, T_j = 25 °C	-	0.1	0.2	
t_{r4}		V_{BS} = 17 V	-	0.15	0.3	
I_{PKSi1}	Peak output sink current	IN = V_{CC}, T_j = 25 °C V_{BS} = 10 V, PW < 10 µs	120	250	-	mA
I_{PKSi2}		IN = V_{CC}, V_{BS} = 10V , PW < 10 µs	70	150	-	
I_{PKSi3}		IN = V_{CC}, T_j = 25 °C V_{BS} = 17 V, PW < 10 µs	250	500	-	
I_{PKSi4}		IN = V_{CC}, V_{BS} = 17 V, PW < 10 µs	150	300	-	
t_{f1}	Output fall time	V_{BS} = 10 V, T_j = 25 °C	-	0.2	0.4	µs
t_{f2}		V_{BS} = 10 V	-	0.3	0.5	
t_{f3}		V_{BS} = 17 V, T_j = 25 °C	-	0.1	0.2	
t_{f4}		V_{BS} = 17 V	-	0.15	0.3	
t_{plh}	Input-to-output turn-on propogation delay (50 % input level to 10 % output level)	-	-	0.1	0.3	µs

Table 6. Electrical characteristics (continued)

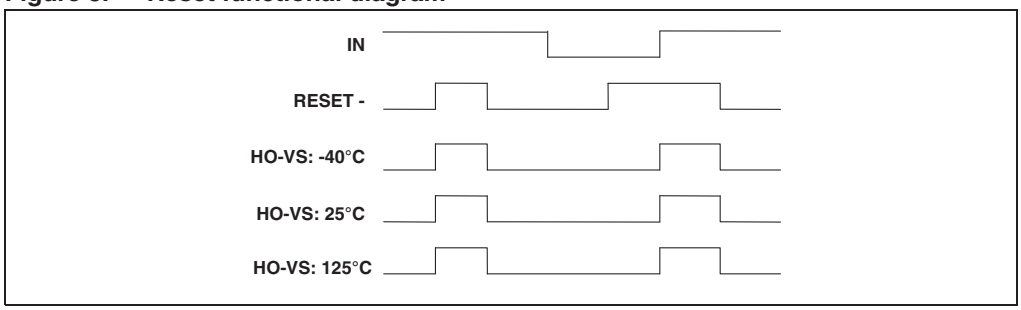
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{phl}	Input-to-output turn-off propogation delay (50 % input level to 90% output level)	-	-	0.1	0.2	µs
t_{phl_res}	RES-to-output turn-off propogation delay (50% input level to 90% output levels)	-	-	0.1	0.3	
t_{plh_res}	RES-to-output turn-on propogation delay (50% input level to 10% output levels)	-	-	0.1	0.8	
Input characteristics						
V_{INH}	High logic level input threshold	-	9.5	-	-	V
V_{INL}	Low logic level input threshold	-	-	-	6	
R_{IN}	High logic level input resistance (Pull-down resistor)	-	60	-	300	kΩ
I_{IN}	Low logic level input current	V_{IN} = 0	-	-	5	µA
V_{H_RES}	High logic level RES input threshold	Reset signal comes from a 5 V system!	3.5	-	-	V
V_{L_RES}	Low Logic Level RES input threshold	R eset signal comes from a 5V system!	-	-	1.4	
R_{RES}	High logic level RES input resistance (Pull-down resistor)	Reset signal comes from a 5 V system with pull-up resistor 3.8 kΩ to 5 V. (1)	60	-	300	kΩ
I_{RES}	Low logic level input current	V_{RES} = 0	-	-	5	µA

1. 4 HS-driver reset- inputs and other IC with their input pull-down resistors are connected in parallel with the RESET wire. The enable input RES- is an active low input, that means a logic low turns the external Power MOSFET off. The input circuitry has to make sure, that the MOSFET is off, when the pin is open or floating. In the application the RES- pin is tied to a bipolar open collector transistor or MOSFET open drain transistor with pull-up resistor 3.8K to +5V together with other RES- inputs of other IC.

2.5 Reset functional diagram

The diagram is guaranteed for the following condition.
V_{CC} = 10 V; V_{BS} = 10 V @ -40 °C, V_{CC} = 17 V; V_{BS} = 17 V @ +25 °C and 125 °C

Figure 3. Reset functional diagram



3 Timing diagrams

Figure 4. Input/output timing diagram

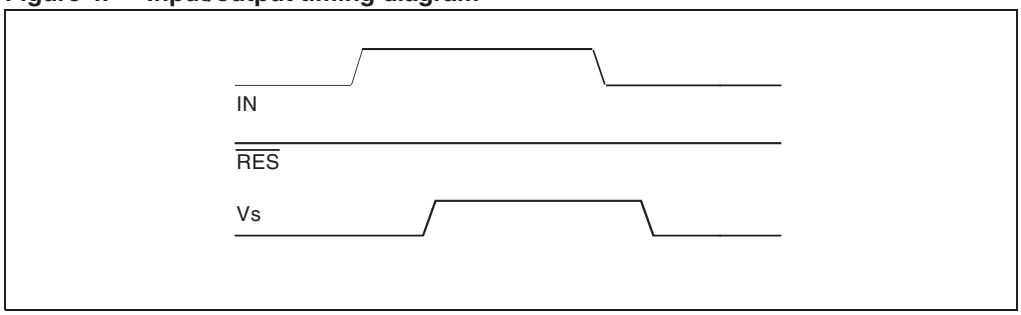
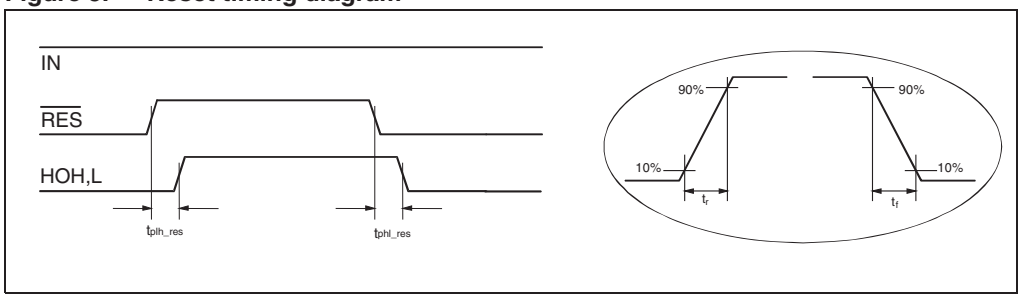


Figure 5. Reset timing diagram



4 Package information

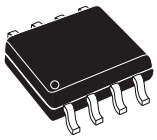
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 6. SO-8 mechanical data and package dimensions

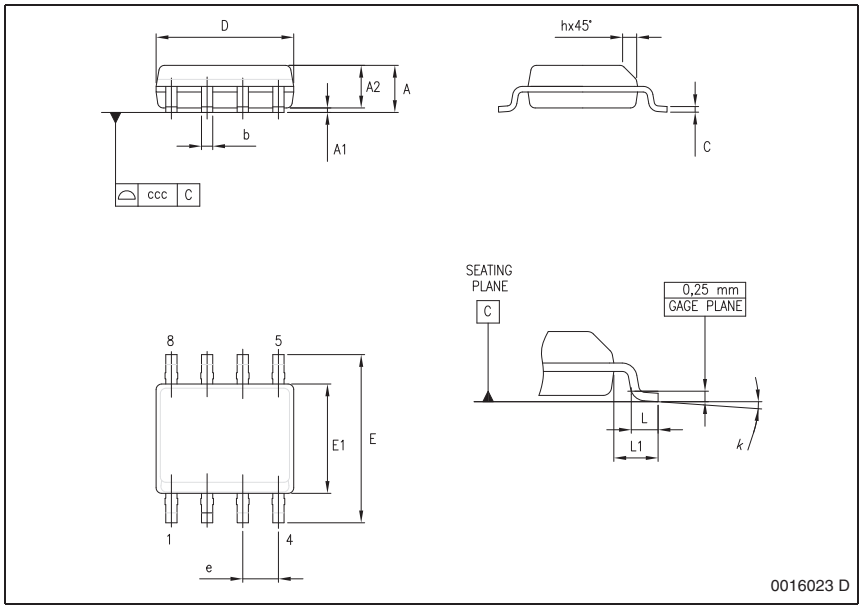
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D (1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(2)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.100			0.0039

Notes: 1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

OUTLINE AND MECHANICAL DATA



SO-8



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
20-Nov-2006	1	Initial release.
07-Oct-2009	2	Updated *Table 1: Device summary*.
17-Sept-2013	3	Updated Disclaimer

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