

Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

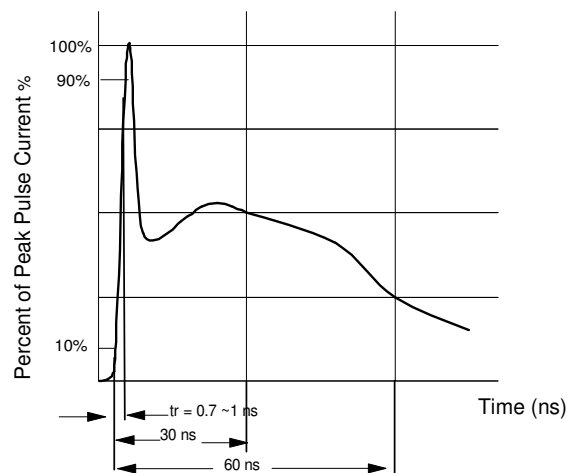


Figure 2. ESD pulse waveform according to IEC 61000-4-2

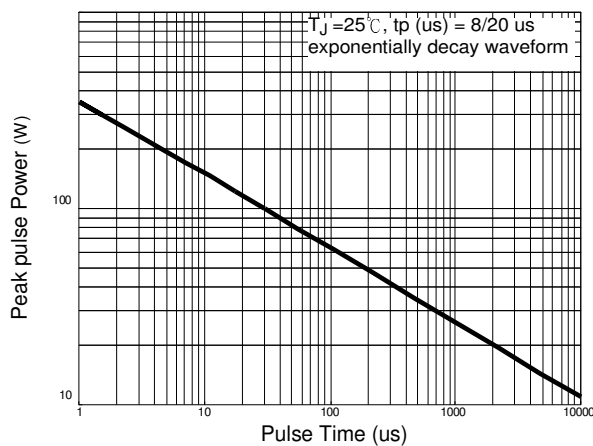


Figure 3. Power Dissipation versus Pulse Time

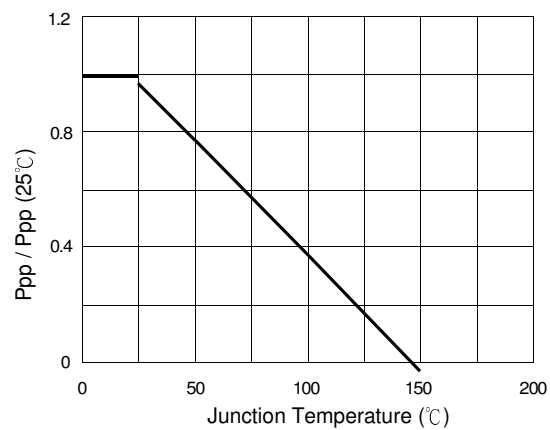


Figure 4. Peak pulse power versus  $T_J$

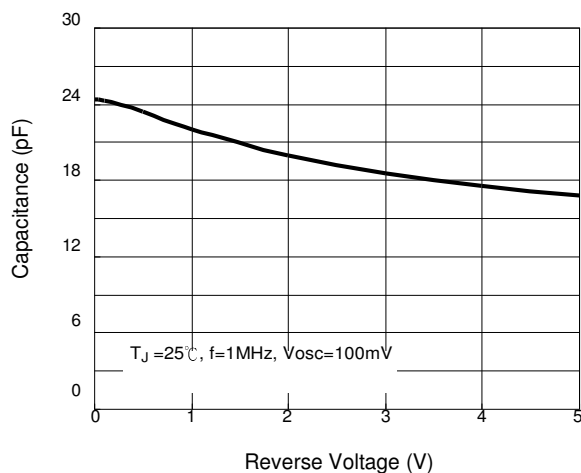


Figure 5. Typical Junction Capacitance

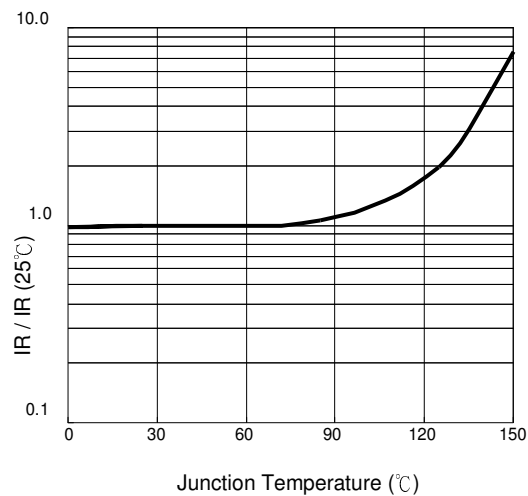


Figure 6. Reverse Leakage Current versus  $T_J$

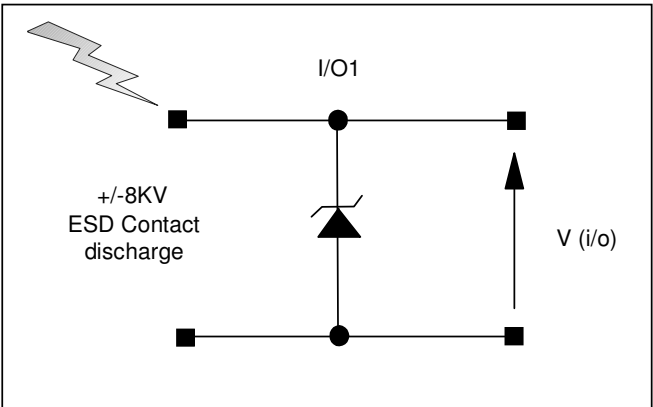


Figure 7. ESD Test Configuration

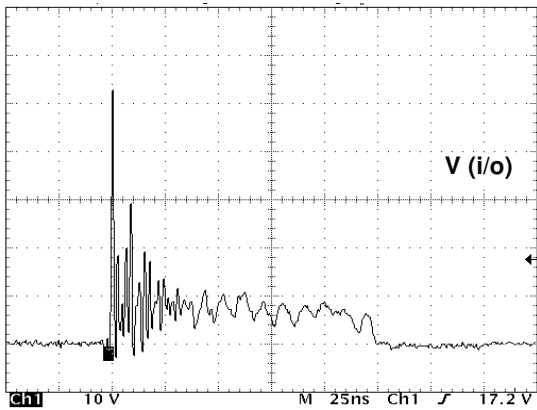


Figure 8. Clamped +8 kV ESD voltage waveform

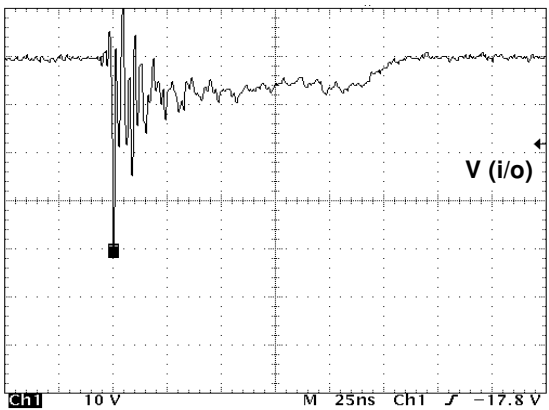
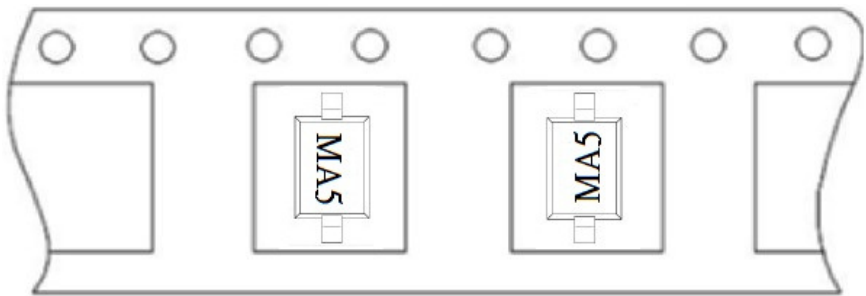


Figure 9. Clamped -8 kV ESD voltage waveform

Marking & Orientation

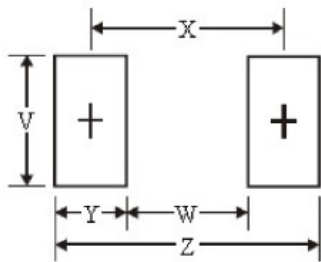


Note: Marking is none direction

Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L35ESD5V0CA2	3000	7	45000	90K/180K

SOD-523 Soldering Pad Layout



Dim.	Millimeters	Inches
Z	2.30	0.090
X	1.50	0.059
W	0.70	0.027
Y	0.80	0.031
V	0.60	0.023

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