

IRFR/U3412

International
IR Rectifier

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C , $I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.025	Ω	$V_{GS} = 10V, I_D = 29A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.5	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 95V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	25	—	—	S	$V_{DS} = 50V, I_D = 29A$
Q_g	Total Gate Charge	—	59	89	nC	$I_D = 29A$
Q_{gs}	Gate-to-Source Charge	—	21	32		$V_{DS} = 50V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	17	26		$V_{GS} = 10V, \text{④}$
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	$V_{DD} = 50V$
t_r	Rise Time	—	68	—		$I_D = 29A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	37	—		$V_{GS} = 10V, \text{④}$
C_{iss}	Input Capacitance	—	3430	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	270	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	150	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	1040	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	170	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	270	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V \text{ ⑤}$

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	160	mJ
I_{AR}	Avalanche Current①	—	29	A
E_{AR}	Repetitive Avalanche Energy①	—	14	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.38mH$, $R_G = 25\Omega$, $I_{AS} = 29A$, (See Figure 12a)
- ③ $I_{SD} \leq 29A$, $di/dt \leq 420A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

* When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

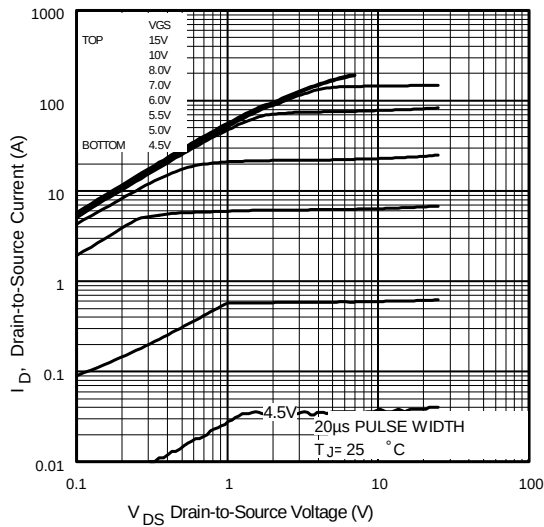


Fig 1. Typical Output Characteristics

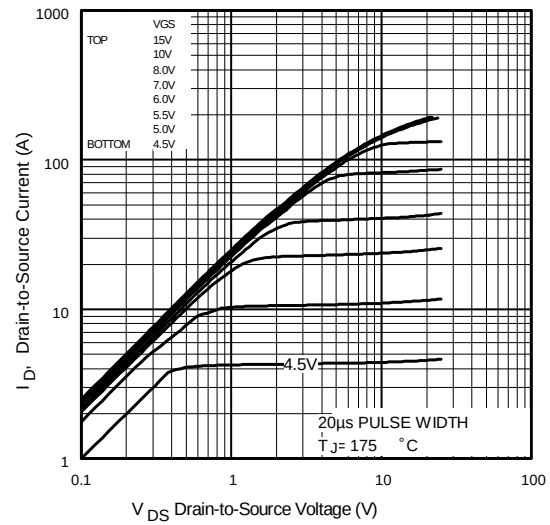


Fig 2. Typical Output Characteristics

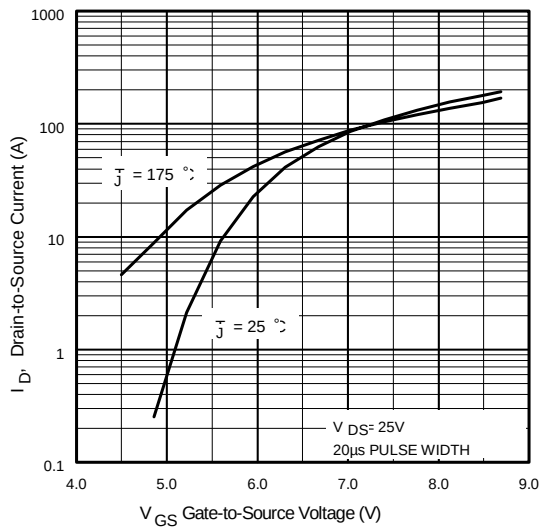


Fig 3. Typical Transfer Characteristics

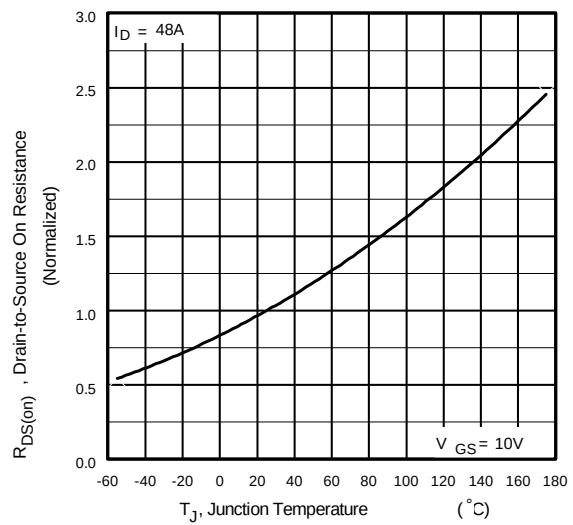


Fig 4. Normalized On-Resistance Vs. Temperature

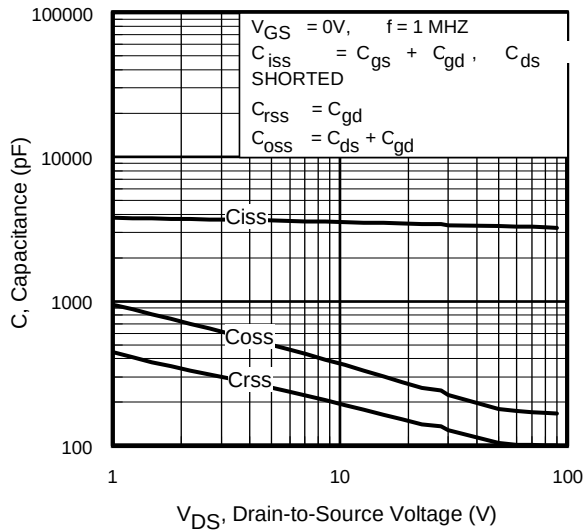


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

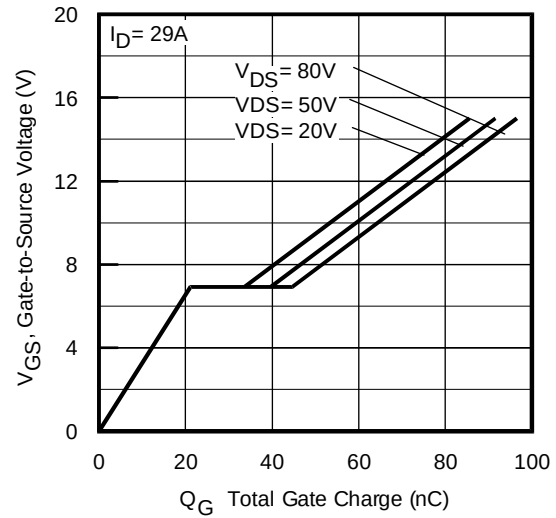


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

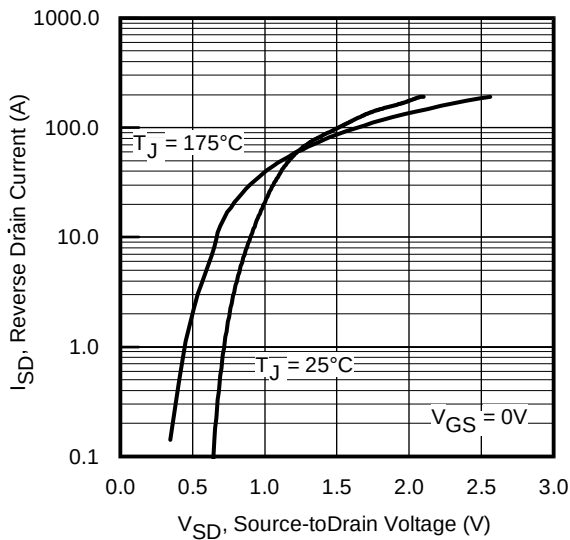


Fig 7. Typical Source-Drain Diode Forward Voltage

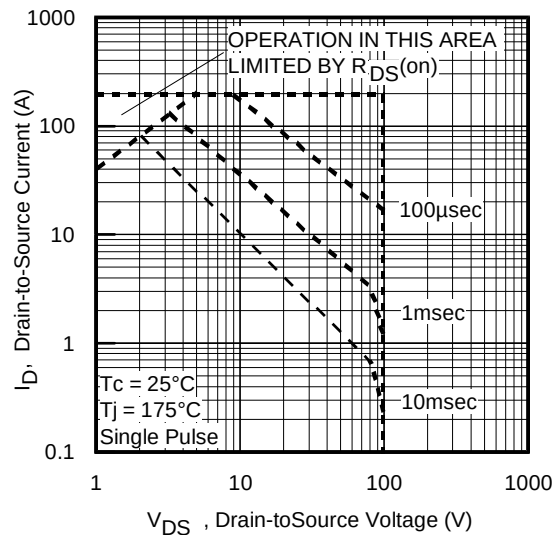


Fig 8. Maximum Safe Operating Area

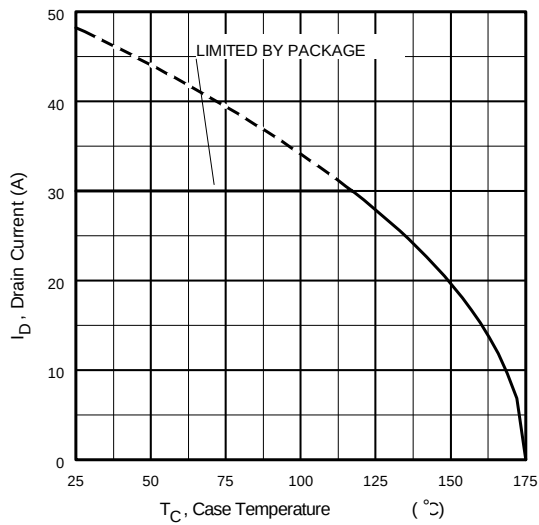


Fig 9. Maximum Drain Current Vs. Case Temperature

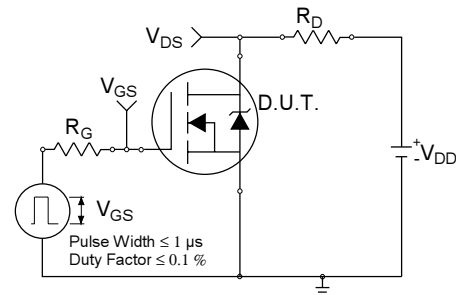


Fig 10a. Switching Time Test Circuit

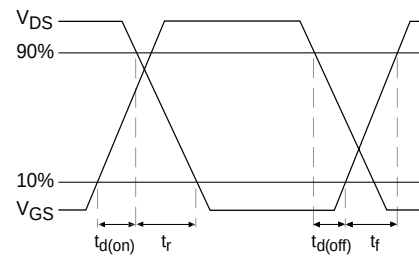


Fig 10b. Switching Time Waveforms

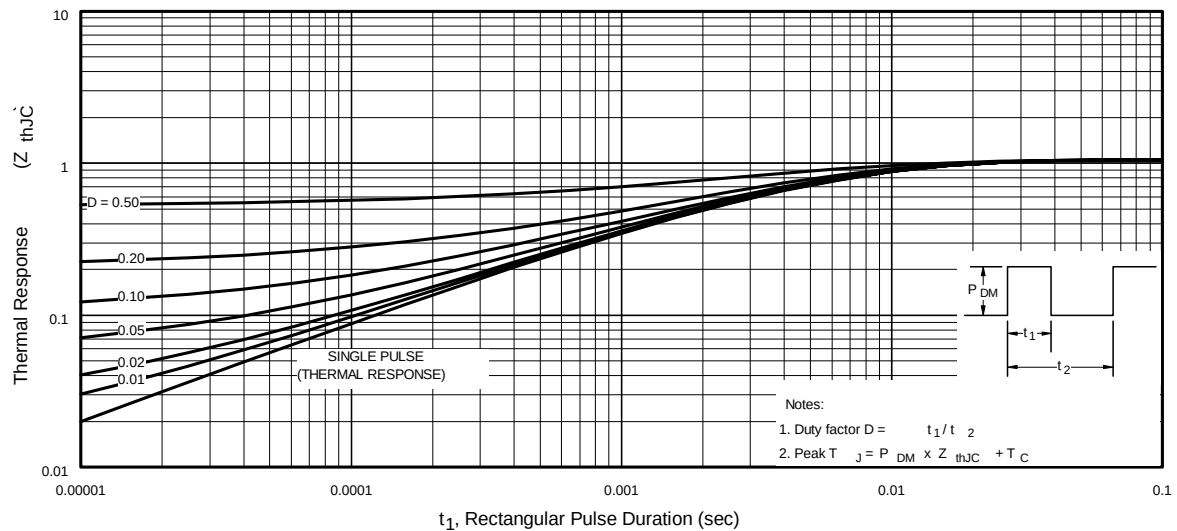


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

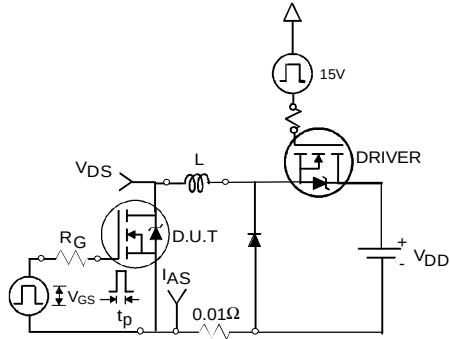


Fig 12a. Unclamped Inductive Test Circuit

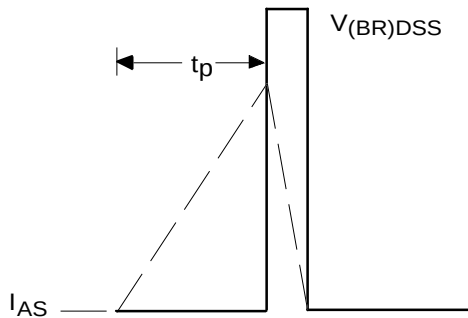


Fig 12b. Unclamped Inductive Waveforms

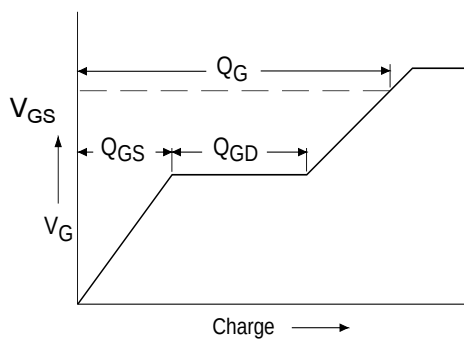


Fig 13a. Basic Gate Charge Waveform

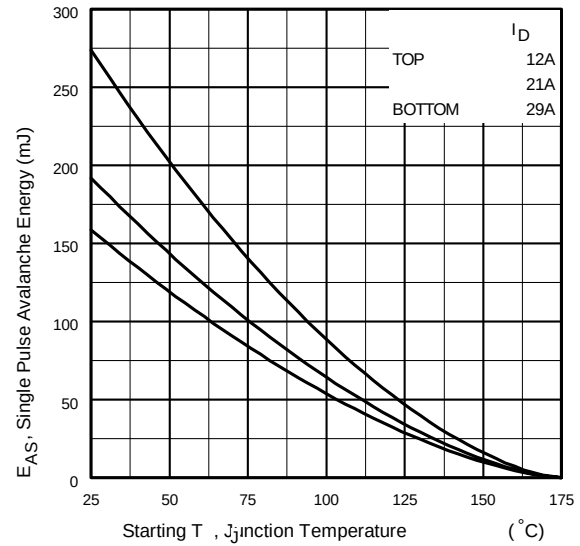


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

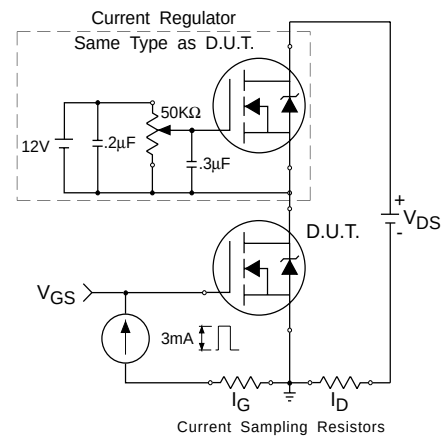
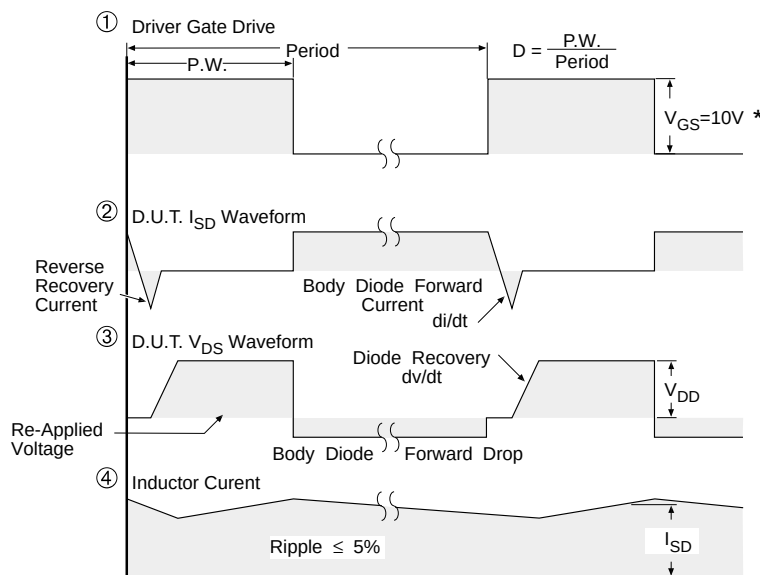
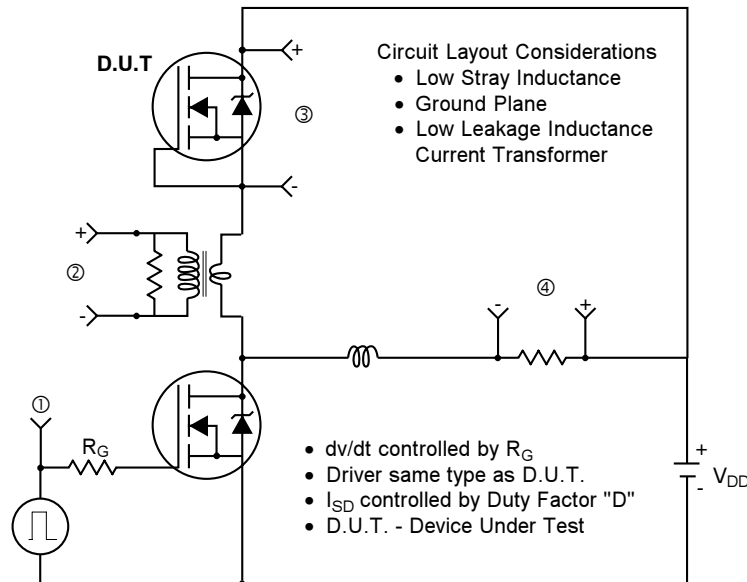


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

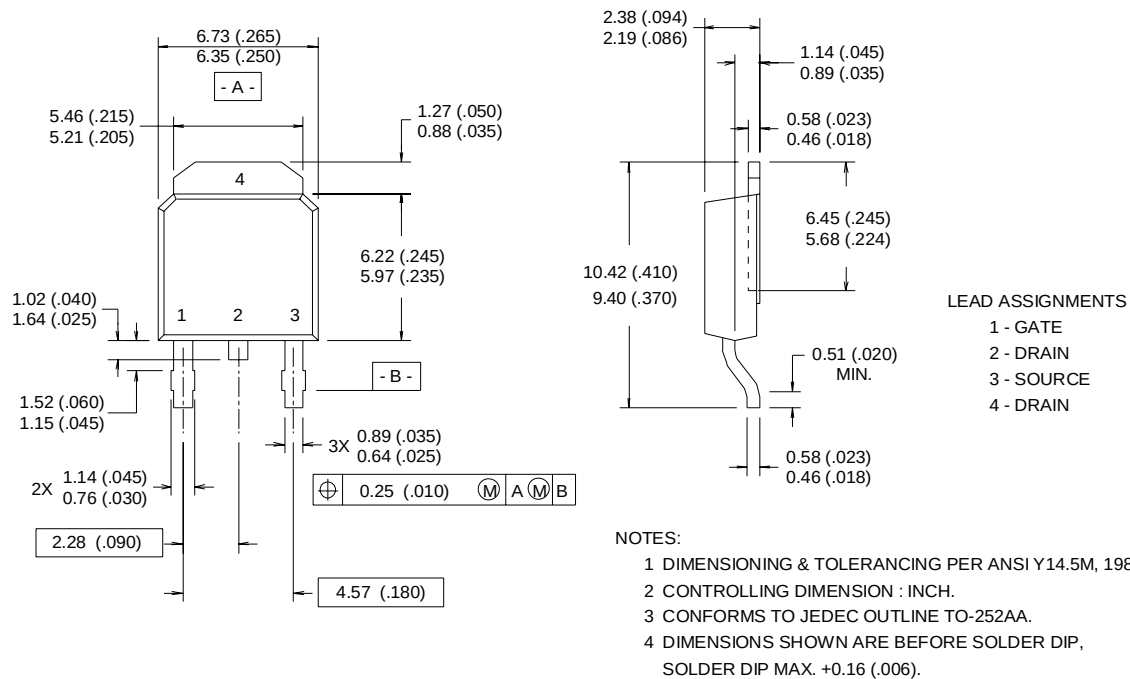


* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

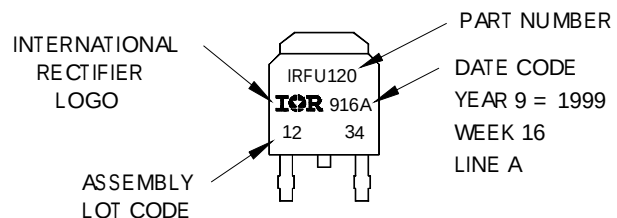
TO-252AA (D-Pak) Package Outline

Dimensions are shown in millimeters (inches)



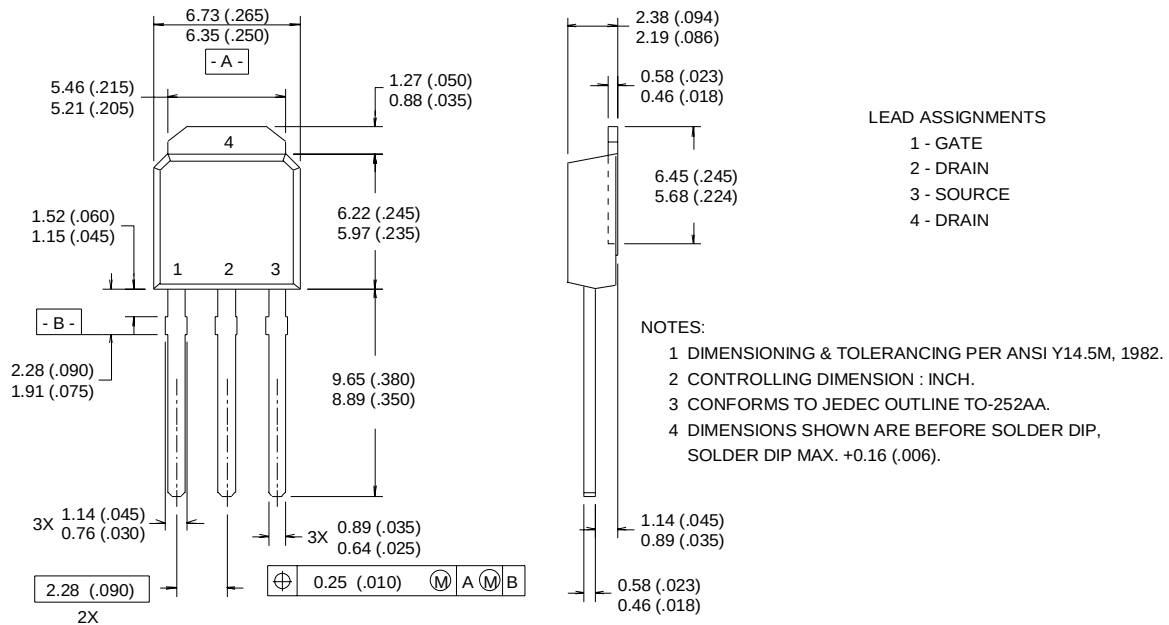
TO-252AA (D-Pak) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



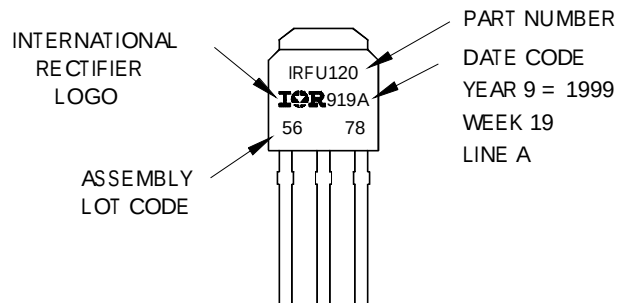
TO-251AA (I-Pak) Package Outline

Dimensions are shown in millimeters (inches)



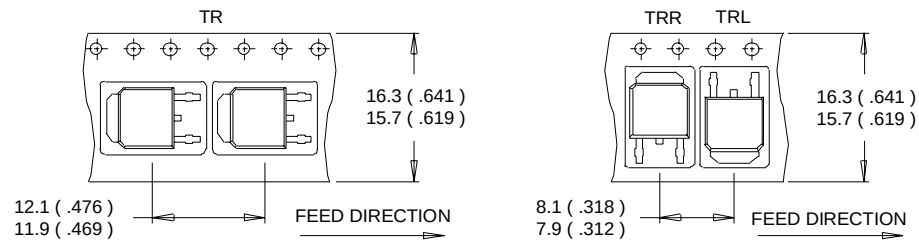
TO-251AA (I-Pak) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"



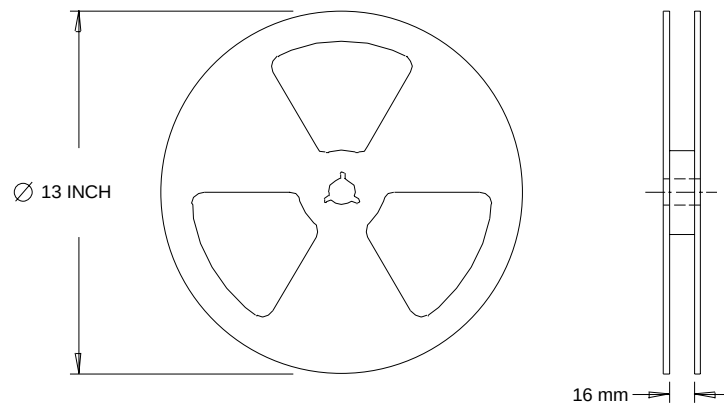
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
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Visit us at www.irf.com for sales contact information.1/02

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>