ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (Referenced to GND)
VDD:.....3.9V
All other Analog and Digital pins.....3.9V

Operating Junction Temperature....-10°C to 150°C
Storage Temperature Range.....-65°C to 150°C
ESD Rating .....HBM Class 2 JEDEC Standard
MSL Rating .....Level 2
Reflow Temperature ..... 260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply: VDD = 3.3V ± 5%, 0°C ≤ T_J ≤ 125°C, 0.5 ≤ Vo ≤ 1.8 V, and operation in the typical application circuit. See notes following table.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
BIAS SUPPLY					
VDD Turn-on Threshold, VDD_{UP}				3.10	V
VDD Turn-off Threshold, VDD_{DN}		2.4			V
VDD UVLO Hysteresis	DI output low when off	75			mV
VDD Operating Current, ICC			350	450	µA
VOLTAGE REFERENCE					
V_{RT} Voltage	R_T = 25.5k Ω	1.452	1.493	1.535	V
R_T resistance range	Note 1		25.5		kΩ
ΔΣ CONVERTER					
Vo common mode range		0.5		1.8	V
Duty Ratio Accuracy	V_{DCR}=20 mV, V_O=1V, R_T=25.5kΩ, R_{CS1}+R_{CS2}=600 Ω T_j=65°C, Note 1			2.5	%
Duty Ratio Accuracy	V_{DCR}=20 mV, V_O=1V, R_T=25.5kΩ, R_{CS1}+R_{CS2}=600 Ω, Note 1			4	%
Sampling frequency, f_{CLK}		435	512	589	kHz
Comparator Offset		-0.5		+0.5	mV
CS pin input current, I_{CS}	DI output low	-250		+250	nA
DIGITAL OUTPUT					
VK pin voltage range		0.5		1.8	V
DI source resistance		1250	2000	3000	Ω

NOTES:
1. Guaranteed by design

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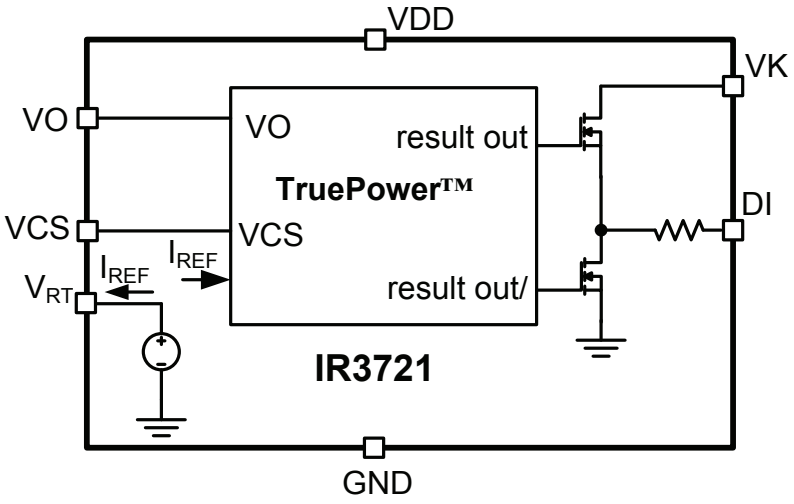
BLOCK DIAGRAM



IC PIN DESCRIPTION

NAME	NUMBER	I/O LEVEL	DESCRIPTION
VCS	1	Analog	Current sensing input, connect through resistor to sensing node
VO	2	Analog	Current sensing reference connect to output voltage
VRT	3	Analog	R_T thermistor network from this pin to GND programs thermal monitor
GND	4		Bias return and signal reference
VDD	5	3.3V	IC bias supply
GND	6		Connect to pin 4
GND	7		Connect to pin 4
DI	8	Analog	Power Monitor output; connect to output filter
VK	9	1.8V	Connect to fixed voltage or VO, multiplied by DI to become analog output
VDD	10	3.3V	Connect to pin 5
BASE PAD			Connect to pin 4

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IC PIN FUNCTIONS

VDD PINS

These pins provide operational bias current to circuits internal to the IR3721. Bypass them with a high quality ceramic capacitor to the GND pins.

GND PINS

These pins return operational bias current to system ground. VO is measured with respect to GND. The GND pin sinks reference current established by the external resistor R_T.

VO PIN

Since this pin measures DCR voltage drop it is critical that it be Kelvin connected to the buck inductor output. Power accuracy may be degraded if the voltage at this pin is below VO_{min}.

VCS PIN

A switched current source internal to the IR3721 maintains the average voltage of this pin equal to the voltage of the VO pin. The average current into this pin is therefore proportional to buck inductor current.

VRT PIN

A voltage reference internal to the IR3721 drives the V_{RT} pin while the pin current is monitored and used to set the amplitude of the current monitor switched current source I_{REF}. Connect this pin to GND through a precision resistor network R_T. This network may include provision for canceling the positive temperature coefficient of the buck inductor's DC resistance (DCR).

VK PIN

The voltage of the VK pin is used to modulate the amplitude of the DI pin. This is one of the terms used to determine the product of the multiplier output. If VK is connected to a fixed voltage then the output of the multiplier is proportional to current. If VK is connected to the buck converter output voltage then the output of the DI driven RC filter is proportional to power.

DI PIN

The DI pin output has a duty ratio proportional to the current into VCS, and an amplitude equal to the voltage at the VK pin. The DI pin is intended to drive an external low pass filter. The output of this filter is the product of the current and voltage terms.

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FUNCTIONAL DESCRIPTION

Please refer to the Functional Description Diagram below. Power flow from the buck converter inductor is the product of output voltage times the current I_L flowing through the inductor.

Power is measured with the aid of International Rectifier's proprietary TruePower™ circuit. Current is converted to a duty ratio that appears at the DI pin. The duty ratio of the DI pin is

$$DI_{DUTYRATIO} = \frac{I_L \cdot DCR}{(R_{CS1} + R_{CS2})} \cdot \frac{R_T}{V_{RT}}$$

Equation 1

The full-scale current that can be measured corresponds to a duty ratio of one.

The amplitude of the DI pin is the voltage appearing at pin VK. If a fixed voltage is applied to VK then the output of the RC filter driven by DI will be proportional to inductor current I_L.

If VO is applied to V_K as shown in the figure then the output of the DI driven RC network will be proportional to power. The full-scale voltage that can be measured is established on the chip to be 1.8V.

The full scale power P_{FS} that can be measured is the product of full-scale voltage and full scale current.

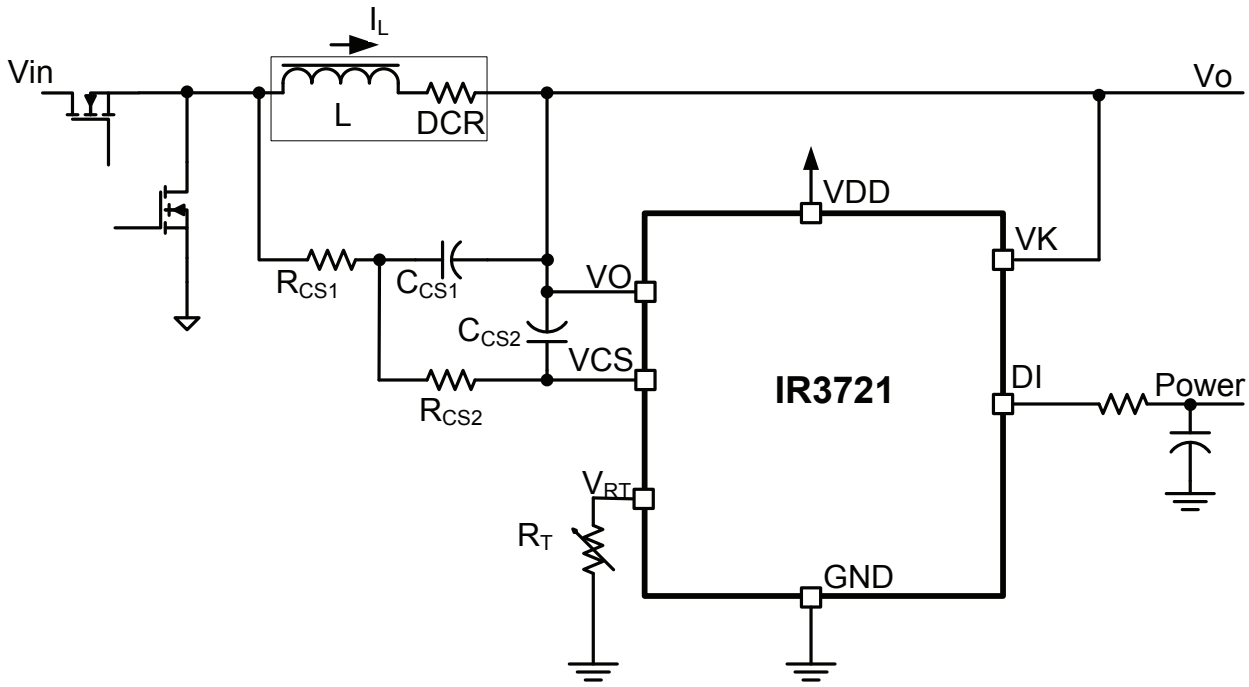

Figure 1 Functional Description Diagram

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THERMAL COMPENSATION FOR INDUCTOR DCR CURRENT SENSING

The positive temperature coefficient of the inductor DCR can be compensated if R_T varies inversely proportional to the DCR. DCR of a copper coil, as a function of temperature, is approximated by

$$DCR(T) = DCR(T_R) \cdot (1 + (T - T_R) \cdot TCR_{Cu})$$

Equation 2

T_R is some reference temperature, usually 25 °C, and TCR_{Cu} is the resistive temperature coefficient of copper, usually assumed to be 0.39 %/°C near room temperature. Note that equation 2 is linearly increasing with temperature and has an offset of $DCR(T_R)$ at the reference temperature.
If R_T incorporates a negative temperature coefficient thermistor then temperature effects of DCR can be minimized. Consider a circuit of two resistors and a thermistor as shown below.

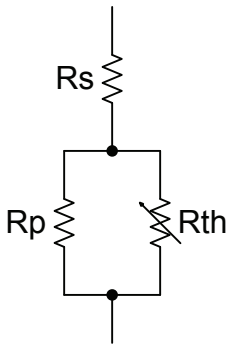

Figure 2 R_T Network

If Rth is an NTC thermistor then the value of the network will decrease as temperature increases. Unfortunately, most thermistors exhibit far more variation with temperature than copper wire. One equation used to model thermistors is

$$R_{th}(T) = R_{th}(T_0) \cdot e^{\left(\beta \left(\frac{1}{T} - \frac{1}{T_0}\right)\right)}$$

Equation 3

where $R_{th}(T)$ is the thermistor resistance at some temperature T, $R_{th}(T_0)$ is the thermistor resistance at the reference temperature T_0, and β is the material constant provided by the thermistor manufacturer. Kelvin degrees are used in the exponential term of equation 3. If R_S is large and R_P is small, the curvature of the equivalent network resistance can be reduced from the curvature of the thermistor alone. Although the exponential equation 3 can never compensate linear equation 2 at all temperatures, a spreadsheet can be constructed to minimize error over the temperature interval of interest. The equivalent resistance R_T of the network shown as a function of temperature is

$$R_T(T) = R_s + \frac{1}{\frac{1}{R_p} + \frac{1}{R_{th}(T)}}$$

Equation 4

using $R_{th}(T)$ from equation 3.
Equation 2 may be rewritten as a new function of temperature using equations 2 and 4 as follows:

$$I_{FS}(T) = \frac{V_{RT}}{R_T(T)} \cdot \frac{(R_{CS1} + R_{CS2})}{DCR(T)}$$

Equation 5

With Rs and Rp as additional free variables, use a spreadsheet to solve equation 5 for the desired full scale current while minimizing the $I_{FS}(T)$ variation over temperature.

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TYPICAL 2-PHASE DCR SENSING APPLICATION

The IR3721 is capable of monitoring power in a multiphase converter. A Two Phase DCR Sensing Circuit is shown below. The voltage output of any phase is equal to that of any and every other phase because they are electrically connected and monitored at VO as before.

Output current is the sum of the two inductor currents (I_{L1} + I_{L2}). Superposition is used to derive the transfer function for multiphase sensing. The voltage on R_{CS2} due to I_{L1} is

$$I_{L1} \cdot DCR_1 \cdot \frac{(R_{CS2} \parallel R_{CS3})}{R_{CS1} + (R_{CS2} \parallel R_{CS3})}$$

Likewise, the voltage on RCS2 due to IL2 is

$$I_{L2} \cdot DCR_2 \cdot \frac{(R_{CS2} \parallel R_{CS1})}{R_{CS3} + (R_{CS2} \parallel R_{CS1})}$$

The current through R_{CS2} due to both inductor currents is I_{CS}. From the two equations above

$$I_{CS} = \frac{I_{L1}DCR_1R_{CS3} + I_{L2}DCR_2R_{CS1}}{R_{CS1}R_{CS2} + R_{CS1}R_{CS3} + R_{CS2}R_{CS3}}$$

The duty ratio of DI is

$$DI_{DUTYRATIO} = \frac{I_{CS} \cdot R_T}{V_{REF}}$$

If DCR1=DCR2, and RCS1=RCS3, then I_{CS} can be simplified to

$$I_{CS} = \frac{(I_{L1} + I_{L2}) \cdot DCR_1}{R_{CS1} + 2R_{CS2}}$$

and the DI duty ratio simplifies to

$$DI_{DUTYRATIO} = \frac{(I_{L1} + I_{L2}) \cdot DCR \cdot R_T}{(R_{CS1} + 2R_{CS2}) \cdot V_{RT}}$$

Full scale current occurs when DI duty ratio becomes one.

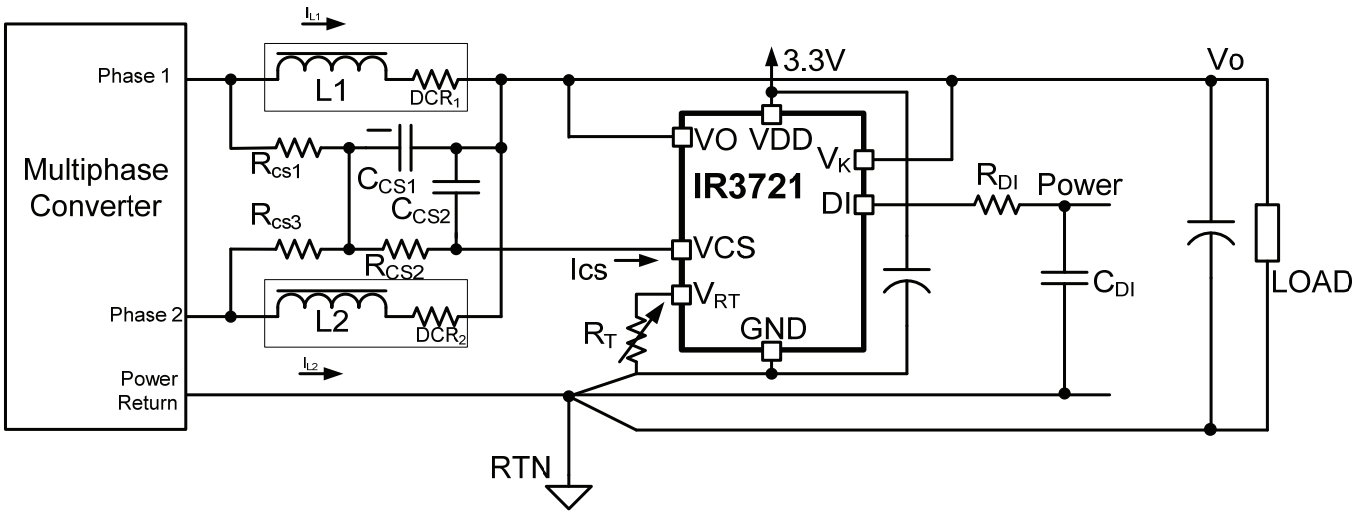

Figure 3 Two Phase DCR Sensing Circuit

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RESISTOR SENSING APPLICATION

The Resistor Sensing Circuit shown below is an example of resistive current sensing. Because the voltage on the shunt resistor is directly proportional to the current I_L through the inductor, R_{CS2} and C_{CS2} do not need to match the L / DCR time constant.

Because the value of the shunt resistance does not change with temperature as the inductor DCR does, R_T can be a fixed resistor.

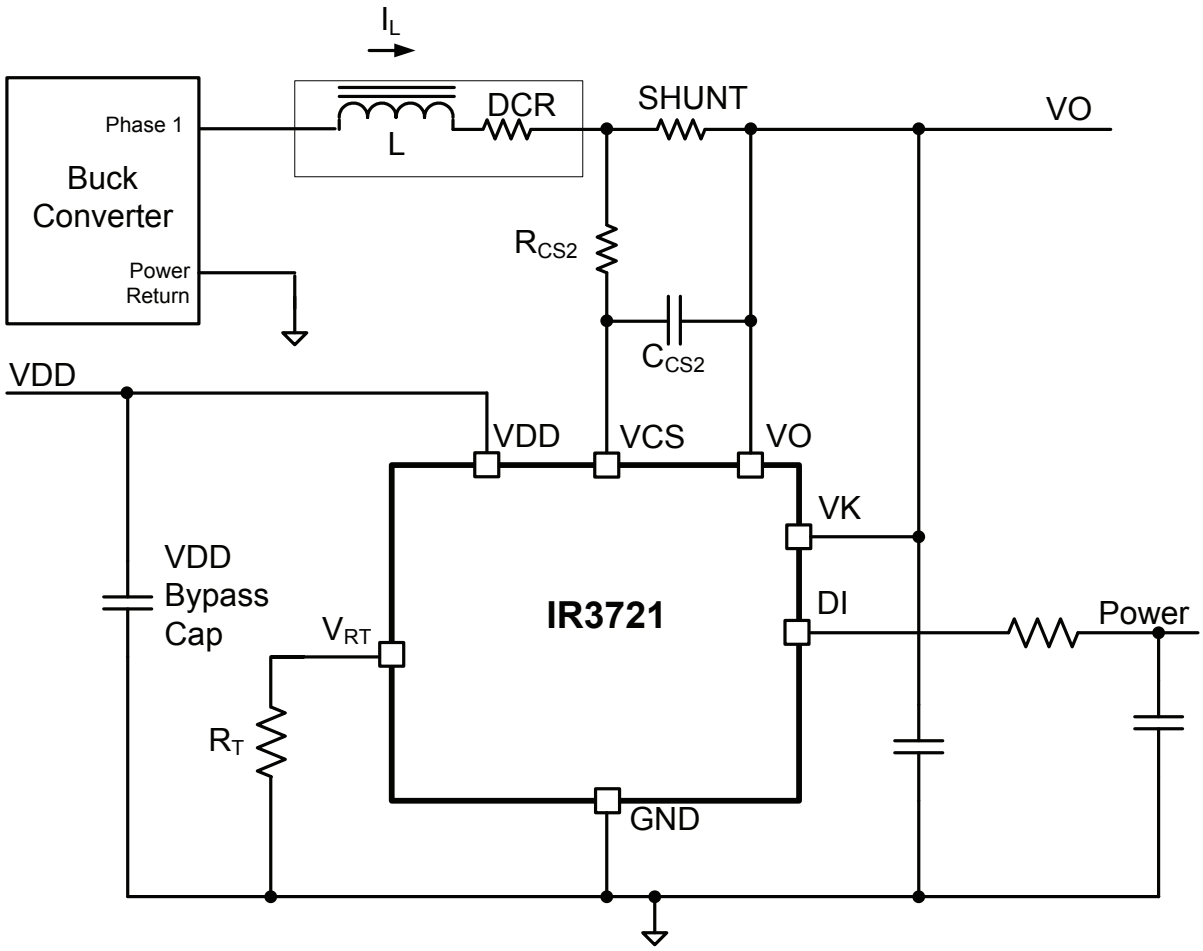

Figure 4 Resistor Sensing Circuit

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COMPONENT SELECTION GUIDELINES

Use a 0.1 µF, 6.3V, X7R ceramic bypass capacitor from VDD to GND and from VK to GND.
Filter the DI output with an RC filter to give a stable analog representation of the current or power. Some of the DI source resistance of this filter is internal to the IR3721 and specified in the electrical specifications table. Add twenty thousand to fifty thousand additional ohms externally to minimize resistance variation. As the DI source resistance increases beyond these guidelines, the voltage measurement error caused by non-ideal voltmeter conductance will increase.
Select a filter capacitor that limits 512 kHz sampling frequency ripple to an acceptable value. Sampling frequency ripple will appear as an error, but can be reduced 20 dB for each decade that the filter corner frequency is below 512 kHz. Select a capacitor value that achieves the desired balance between low sampling frequency ripple and adequate bandwidth.

Resistor current sensing

For resistor current sensing select a precision resistor for R_T inside the R_T resistance range limits specified in the Electrical Specifications table, such as 25.5kΩ and 1% tolerance.
Next, select a shunt resistor that will provide the most current sensing voltage while also considering the allowable power dissipation limitations. The DI output will saturate to the VK voltage when full scale current I_{FS} flows through this shunt. Recommended maximum current sensing voltage range is 5 to 150 mV. Maximum sensing voltages less than 5 mV will cause comparator input offset voltage errors to dominate, and voltages larger than 150 mV will cause comparator leakage current, I_{CS}, errors to dominate.
Select R_{CS2} to be the next higher standard value resistor from $(R_{SHUNT} \cdot I_{FS} \cdot R_T) / V_{RT}$ in order to accommodate full scale current I_{FS}.
Bypass VCS to VO with capacitor C_{CS2}. The value of this capacitor limits the bandwidth, but is required because it is the integrator of the delta sigma modulator. Consider selecting the value of C_{CS2} to place a filter corner frequency at 5 kHz, which will reduce sampling ripple by 40 dB.

DCR current sensing

Select an R_T network resistance between 20kΩ and 45.3kΩ. Consider the R_T network of Figure 5 for DCR current sensing.

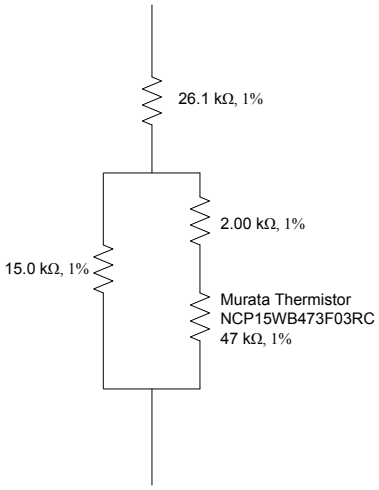

Figure 5 R_T network

The resistance of the network above at 25°C, $R_T(25)$, is 37.58kΩ. Over temperature $R_T(T)$ is multiplied by copper resistance, $DCR(25) \cdot (1+(T-25) \cdot 0.0039)$, divided by $(DCR(25) \cdot (R_T(25))$ to normalize the results, and plotted as nominal error in Figure 6.

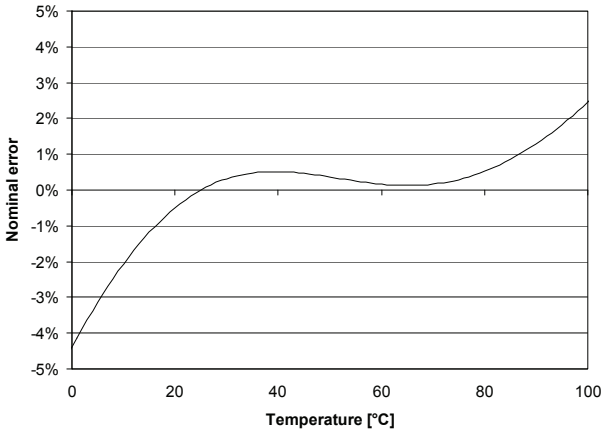

Figure 6 Nominal error vs. Temperature

Note that the error due to temperature compensation at 25°C is zero, assuming ideal R_T components. At other temperatures the results are over or under reported by the factor in percent indicated.
Proceed to calculate R_{SUM}, defined as the sum of R_{CS1} plus R_{CS2}, as follows.

$$R_{SUM}=I_{FS} \cdot DCR(25) \cdot R_T(25) / V_{RT}$$

Again, I_{FS} is full scale current and V_{RT} is the reference voltage establishing the current in R_T.
Estimate the capacitance C_{CS1} with the following equation.

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$$C_{CS1} > \frac{4 \cdot L}{DCR\,(25) \cdot R_{SUM}}$$

Choose a standard capacitor value larger than indicated by the right hand side of the inequality above.

Calculate the equivalent resistance R_{eq}.

$$R_{eq} = L / (DCR(25) \cdot C_{CS1})$$

We now have two equations, $R_{SUM} = R_{CS1} + R_{CS2}$ and $Req = (R_{CS1} \cdot R_{CS2}) / (R_{CS1} + R_{CS2})$. Calculate R_{CS1} and R_{CS2} using the following two equations.

$$R_{CS1} = R_{SUM} \cdot \left(\frac{1 + \sqrt{1 - 4 \cdot \frac{R_{eq}}{R_{SUM}}}}{2} \right) \text{ and}$$

$$R_{CS2} = R_{SUM} \cdot \left(\frac{1 - \sqrt{1 - 4 \cdot \frac{R_{eq}}{R_{SUM}}}}{2} \right)$$

Use the next higher standard 1% value than indicated in the equations above. This will insure that full scale current can be measured.
Bypass VCS to VO with capacitor C_{CS2}. The value of this capacitor limits the bandwidth, but is required because it is the integrator of the delta sigma modulator. Consider selecting the value of C_{CS2} to place a filter corner frequency at 5 kHz, which will reduce sampling ripple by 40 dB.

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LAYOUT GUIDELINES

Refer to figures 7 through 11 for guidance laying out the IR3721. These guidelines also apply to resistive current sensing. The following guidelines will minimize sources of noise and error, which is required because millivolt level signals correspond to amps of inductor current.

1. Place the capacitor Ccs2 close to the VO and VCS pins of the IR3721. Treat VO and VCS as a differential signal pair back to the IC as shown in the elliptical area designated #1 of figure 8.
2. Sense the inductor (or shunt) Kelvin style at its terminals. Route the leads back as a differential pair. Refer to area #2 of figure 8.
3. Route signal VOUT back to the IC VK pin on its own dedicated trace. Refer to area #3 of figure 8.
4. Place the thermistor near the inductor. Refer to area #4 of figure 8. Route the thermistor leads back to the rest of the network using differential traces. Mount the rest of the thermistor network consisting of Rs, Rp, and R1 close to the IC.
5. Use an isolated dedicated ground plane connected only to components associated with the IR3721 that connect to GND as shown in figure 9. Connect this dedicated ground plane at one location only to the ground of the monitored voltage. The thermally relived via in figure eight illustrates this connection.
6. Bypass IC VDD pin 5 to GND pin 4 with a high quality 0.1 µF ceramic capacitor. Refer to area #6 of figure 8.
7. Bypass the IC VK pin to GND with a high quality 0.1 µF ceramic capacitor. Refer to area #7 of figure 8.

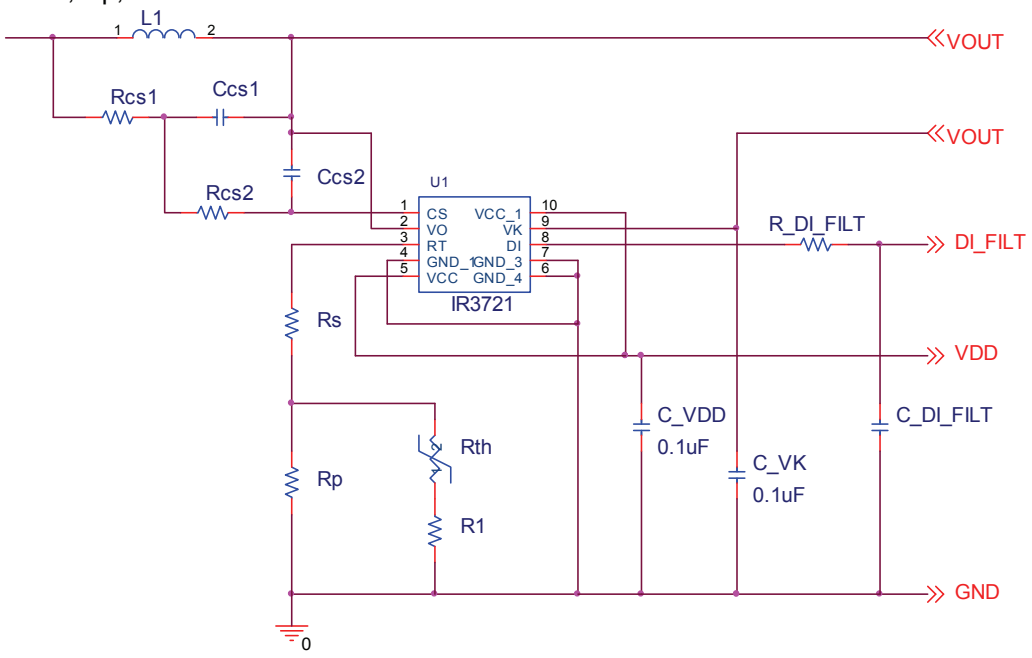

Figure 7 Example schematic

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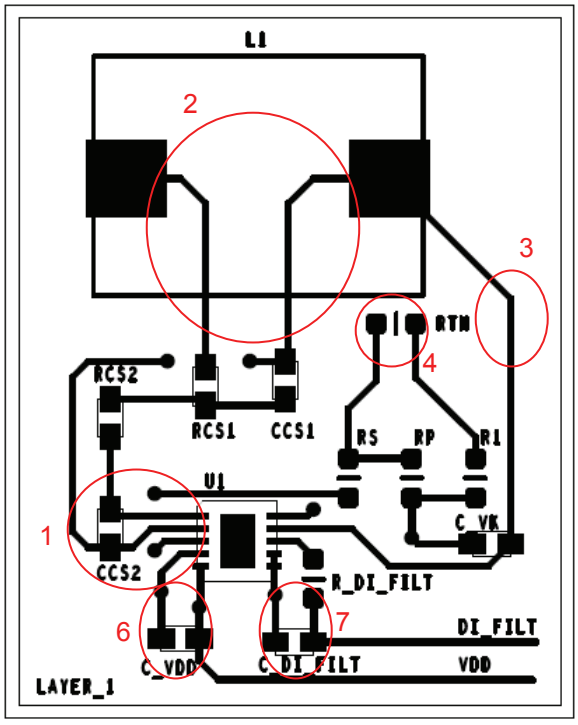

Figure 8 Layer 1

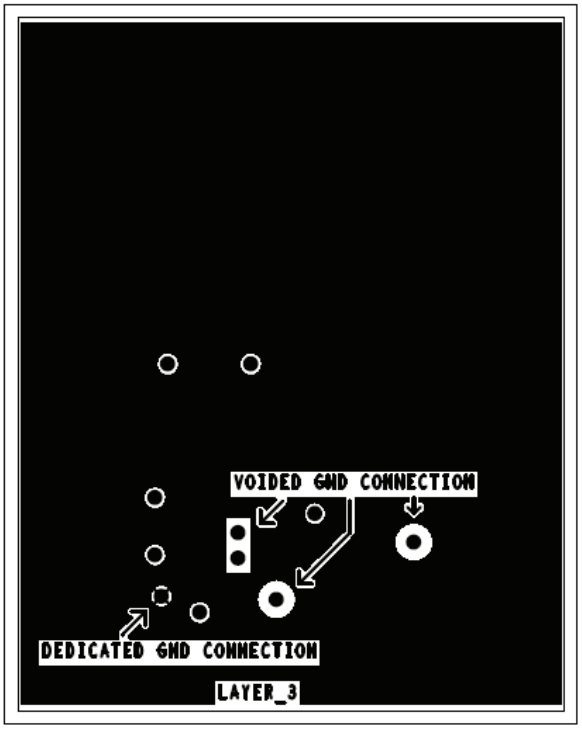

Figure 10 Layer 3

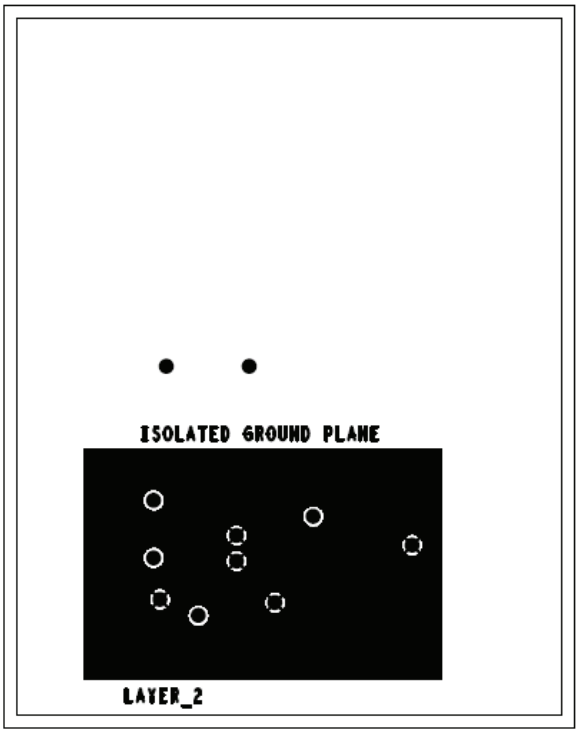

Figure 9 Layer 2

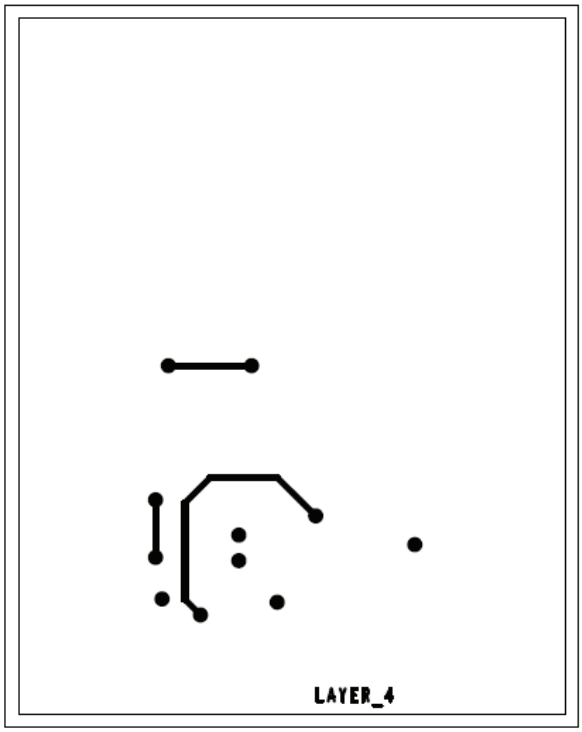

Figure 11 Layer 4

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PCB PAD AND COMPONENT PLACEMENT

Figure 12 below shows suggested pad and component placement.

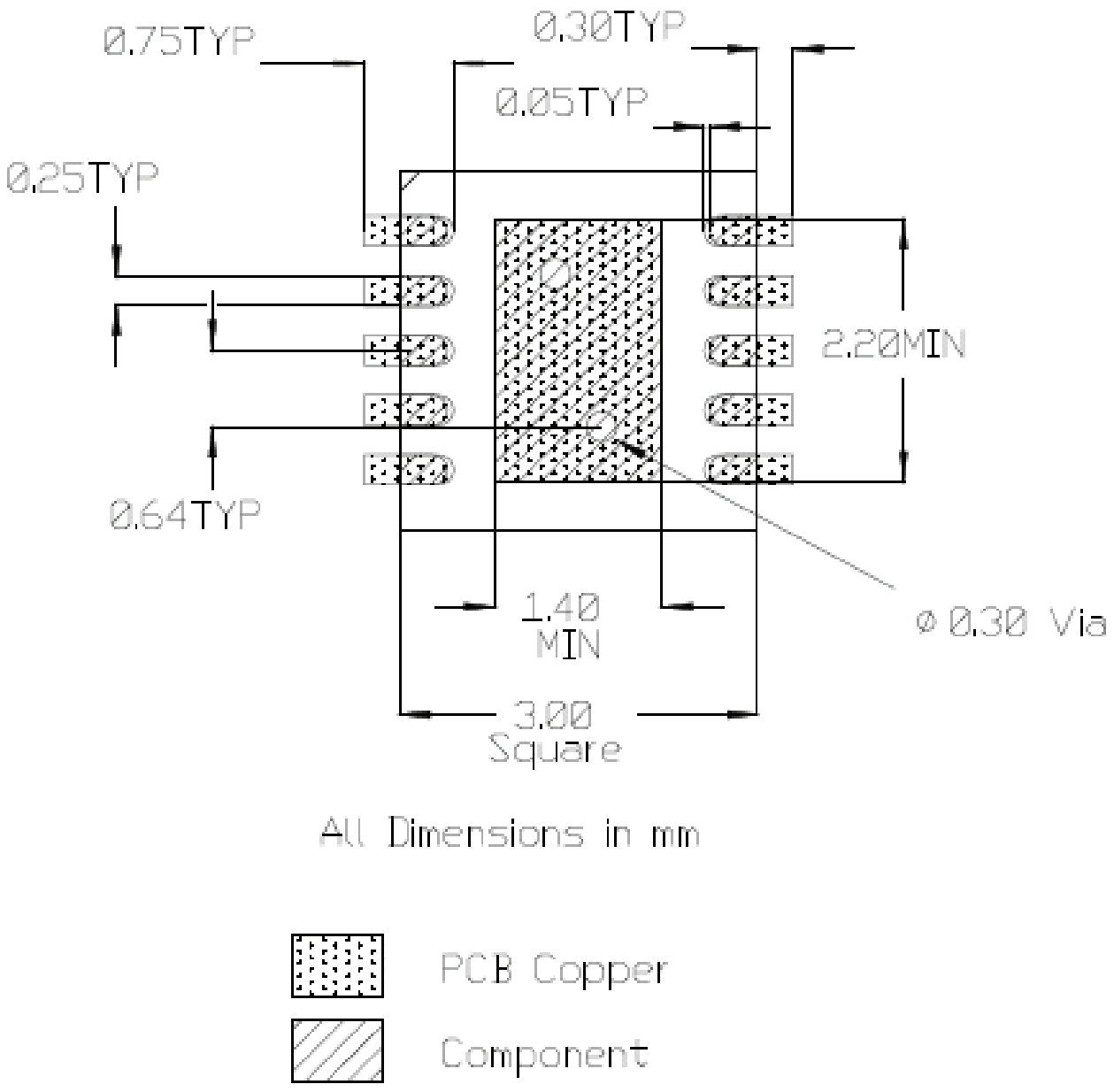

Figure 12 Pad placement

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SOLDER RESIST

Figure 13 below shows suggested solder resist placement.

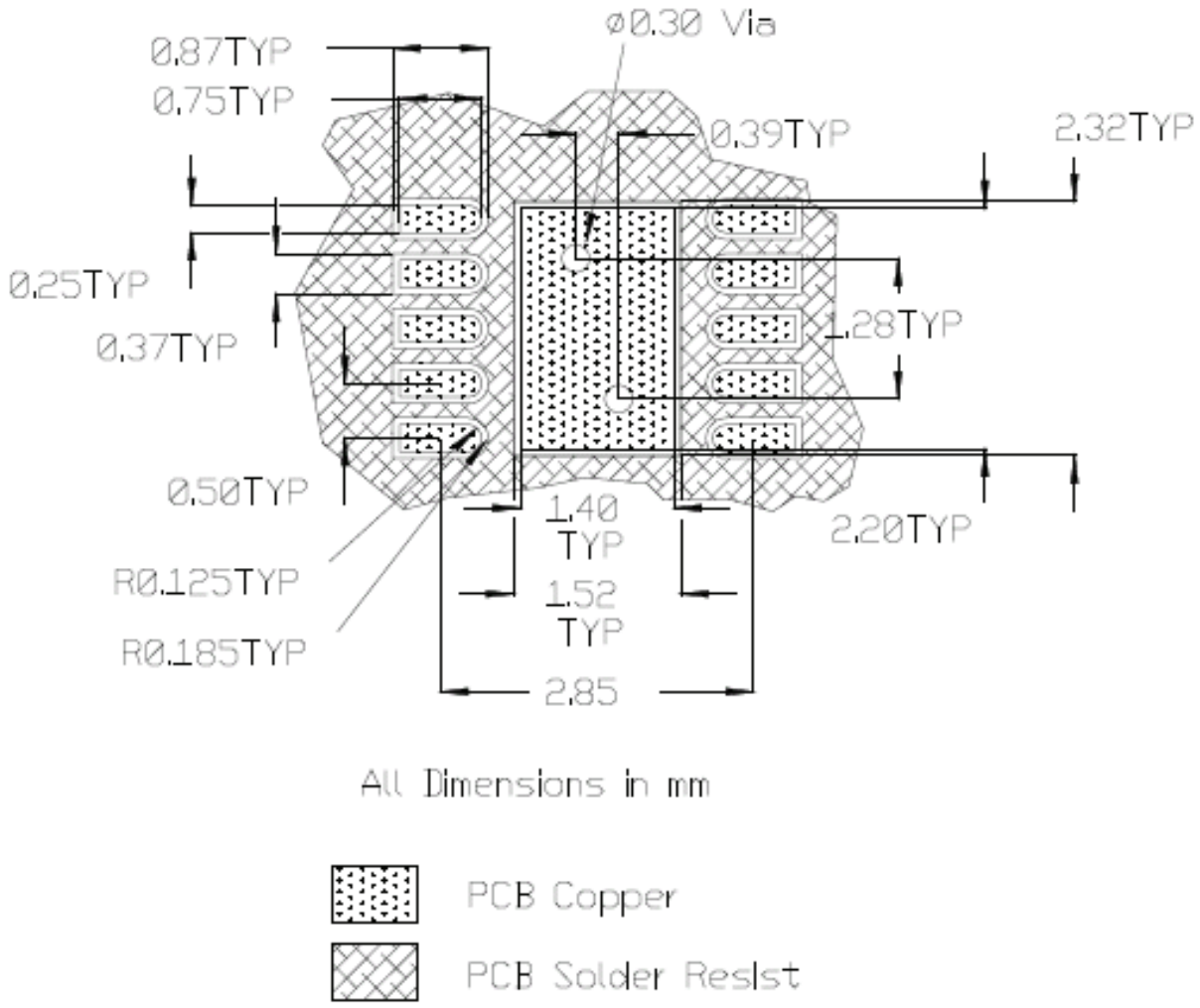

Figure 13 Solder resist

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STENCIL DESIGN

Figure 14 below shows a suggested stencil design.

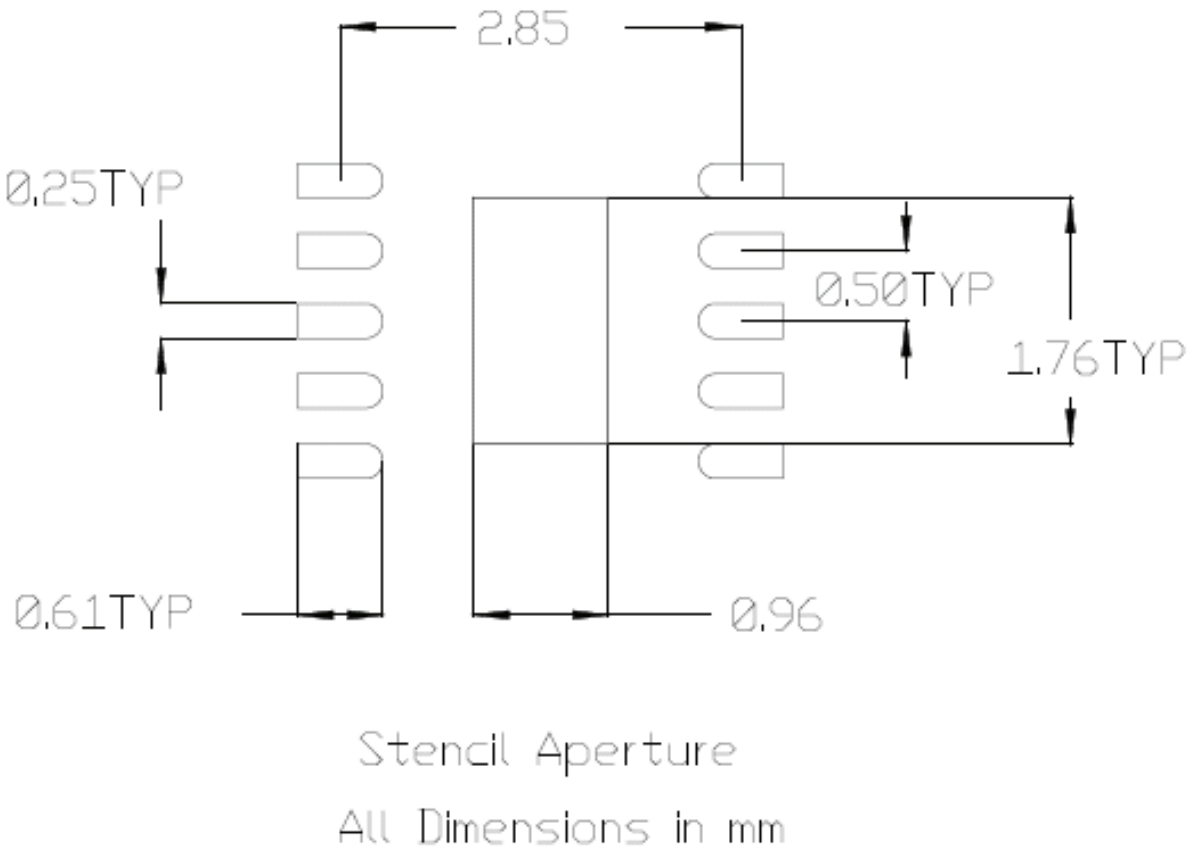

Figure 14 Stencil design

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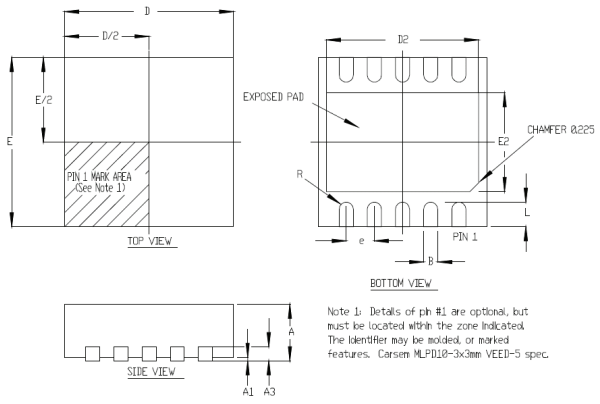
PACKAGE INFORMATION

3 X 3 MM 10L DFN LEAD FREE



SYMBOL	10 PIN 3X3 MM		
DESIGN	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		3.00 BSC	
D2	2.20	---	2.70
E		3.00 BSC	
E2	1.40	---	1.75
e		0.50 BSC	
L	0.30	0.40	0.50
R	0.09	---	---

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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