

HMC859* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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EVALUATION KITS

- HMC859LC3 Evaluation Board

DOCUMENTATION

Data Sheet

- HMC859: 26 GHz, Divide-By-8 with Reset & Programmable Output Voltage Data Sheet

DESIGN RESOURCES

- HMC859 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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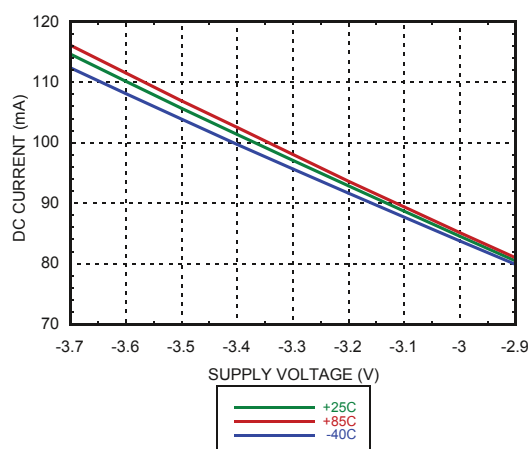
26 GHz, DIVIDE-BY-8 WITH RESET & PROGRAMMABLE OUTPUT VOLTAGE

Electrical Specifications (continued)

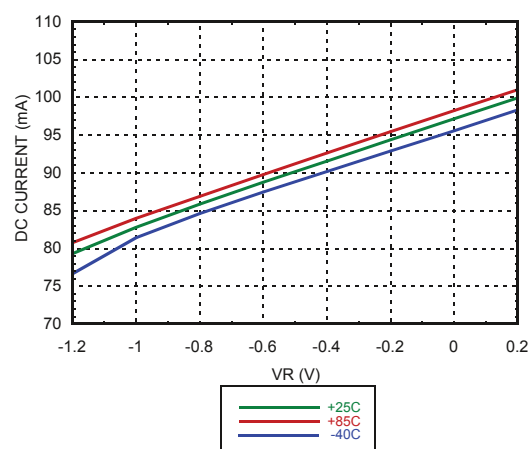
Parameter	Conditions	Min.	Typ.	Max	Units
Output Rise / Fall Time	Differential, 20% - 80%		19 / 17		ps
Output Return Loss	Frequency <14 GHz		10		dB
Random Jitter Jr	rms ^[1]		0.09	0.13	ps rms
Propagation Delay Clock to Q, t _{cd}			146		ps
Propagation Delay Reset to Q, t _{dr}			158		ps
VR Pin Current	VR = 0.0 V		3		mA
VR Pin Current	VR = 0.4 V			4.25	mA

[1] Added jitter calculated by de-embedding the clock source jitter.

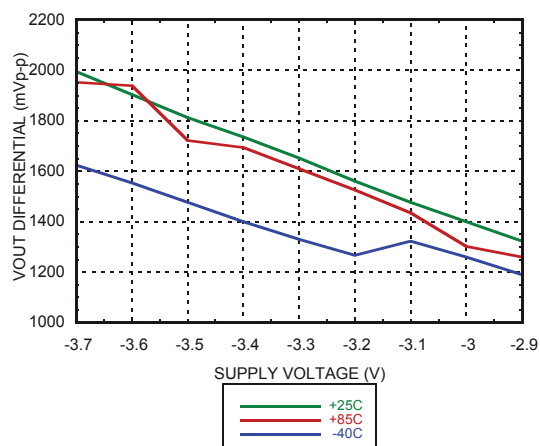
DC Current vs. Supply Voltage ^{[1][2]}



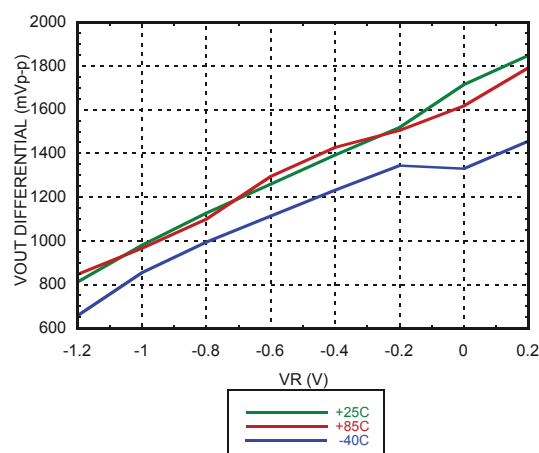
DC Current vs. VR ^{[2][3]}



Output Differential Voltage vs. Supply Voltage ^{[1][2]}



Output Differential Voltage vs. VR ^{[2][3]}



[1] VR = 0.0 V

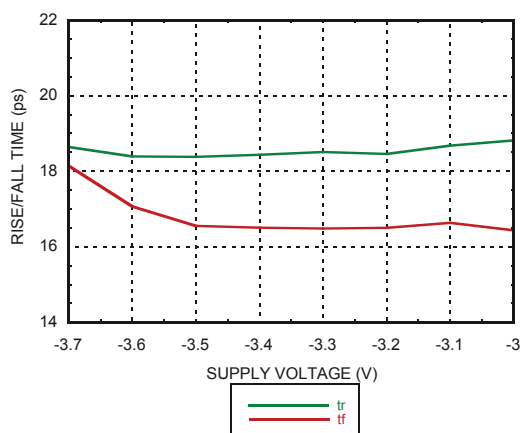
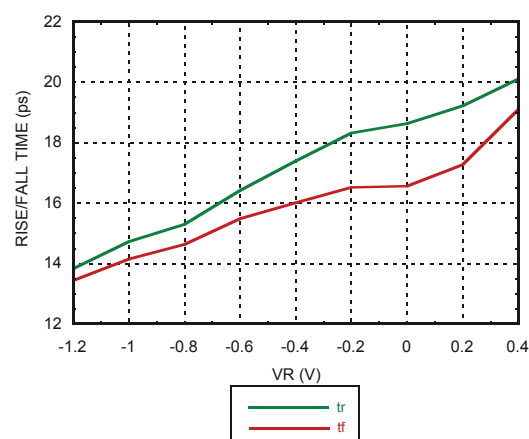
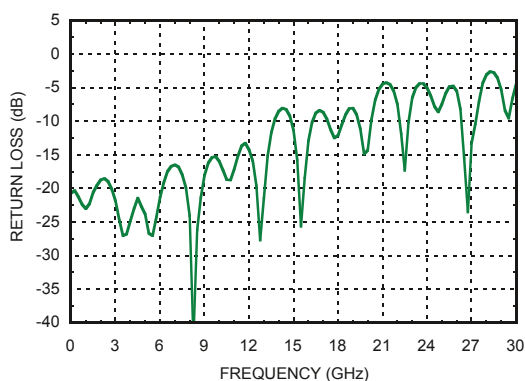
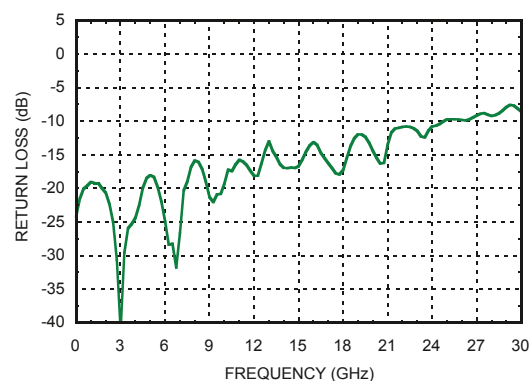
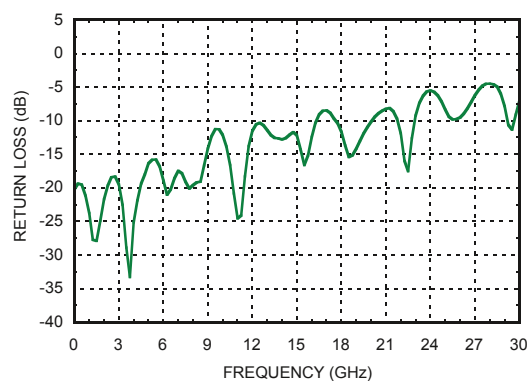
[2] Frequency = 28 GHz

[3] Vee = -3.3 V

For price, delivery and to place orders: Hittite Microwave Corporation, 2 Elizabeth Drive, Chelmsford, MA 01824

Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com

Application Support: Phone: 978-250-3343 or apps@hittite.com


**26 GHz, DIVIDE-BY-8 WITH RESET &
PROGRAMMABLE OUTPUT VOLTAGE**
Rise / Fall Time vs. Supply Voltage [1][2]

Rise / Fall Time vs. VR [2][3]

Clock Output Return Loss [1][2][3][4]

Clock Input Return Loss [1][2][3][4]

Reset Input Return Loss [1][2][3][4]


[1] VR = 0.0 V

[2] Frequency = 28 GHz

[3] Vee = -3.3 V

[4] Device measured on evaluation board with gating

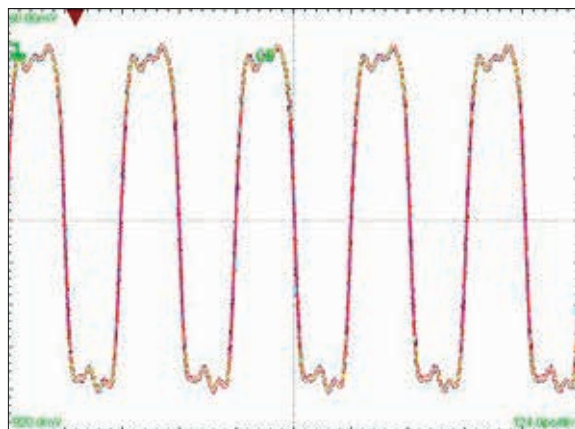
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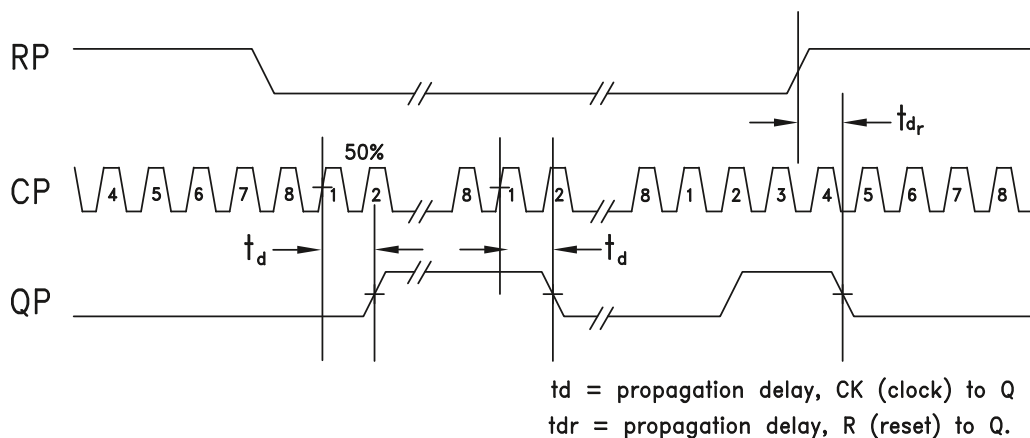
Output Waveform



[1] Test Conditions:

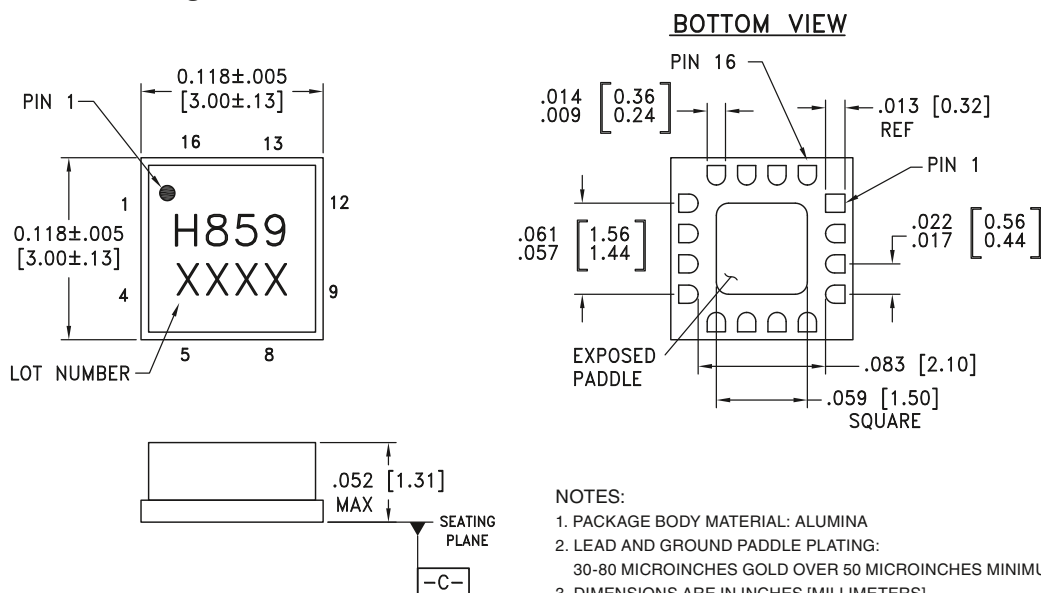
Waveform generated with a CW signal source input at 28 GHz.
 Diagram data presented on a Tektronix CSA 8000.

Timing Diagram




**26 GHz, DIVIDE-BY-8 WITH RESET &
PROGRAMMABLE OUTPUT VOLTAGE**
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance (R _{th-j-p}) Worst Case Junction to Package Paddle	59 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
Maximum Junction Temperature	125 °C
ESD Sensitivity (HBM)	Class 1B


**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**
Outline Drawing

NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[2]
HMC859LC3	Alumina, White	Gold over Nickel	MSL3 ^[1]	H859 XXXX

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX


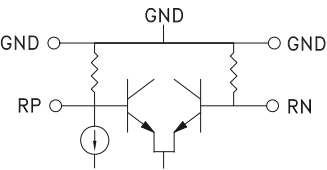
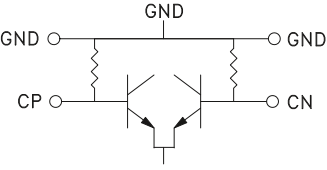
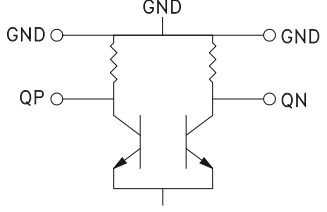

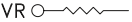
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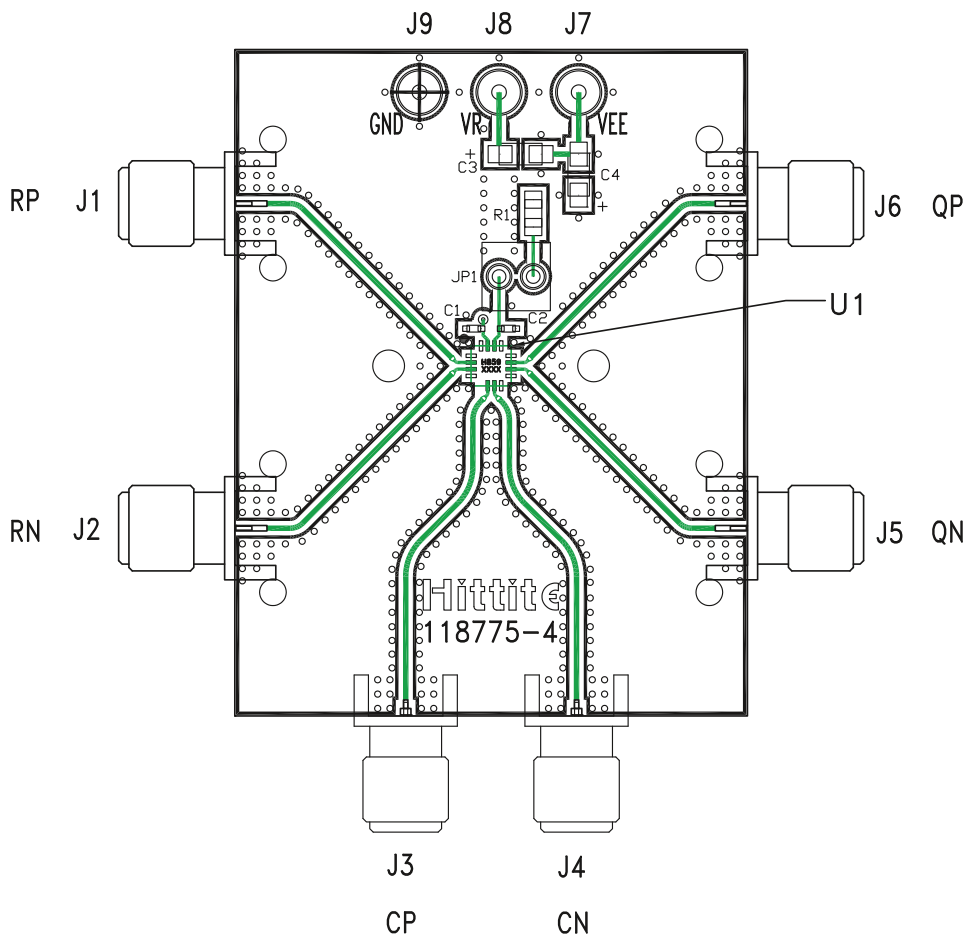
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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	RP, RN	Differential Reset Inputs: Current Mode Logic (CML) referenced to positive supply.	
6, 7	CP, CN	Differential Clock Inputs: Current Mode Logic (CML) referenced to positive supply.	
10, 11	QN, QP	Differential Clock Outputs: Current Mode Logic (CML) referenced to positive supply.	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per "Output Differential vs. VR" plot.	
15, Package Base	Vee	This pin and the exposed paddle must be connected to the negative voltage supply.	

**26 GHz, DIVIDE-BY-8 WITH RESET &
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Evaluation PCB



List of Materials for Evaluation PCB 123585 [1]

Item	Description
J1, J2, J5, J6	PCB Mount SMA RF Connectors
J3, J4	PCB Mount 2.92mm RF Connectors
J7 - J9	DC Pin
JP1	2-Position Header with Shunt
C1 - C2	100 pF Capacitor, 0402 Pkg.
C3 - C4	4.7 μ F Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC859LC3 Clock Divider
PCB [2]	118775 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

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Application Circuit

