IGBT - NPT

600 V

HGTG30N60B3

Description

The HGTG30N60B3 combines the best features of high input impedance of a MOSFET and the low on−state conduction loss of a bipolar transistor. The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: UPS, solar inverter and power supplies.

Features

- 30 A, 600 V, T_C = 110°C
- Low Saturation Voltage: $V_{CE(SAT)}$ = 1.45 V @ I_C = 30 A
- Typical Fall Time . . . . 90 ns at T_J = 150°C
- Short Circuit Rating
- Low Conduction Loss
- This Device is Pb−Free

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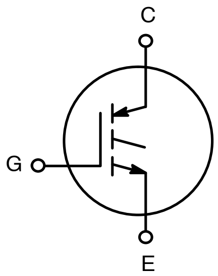
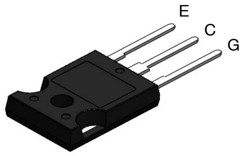
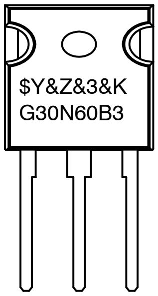
V_{CES}	I_C
1200 V	30 A





TO−247−3LD
CASE 340CK

MARKING DIAGRAM



$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
G30N60B3 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

March, 2020 − Rev. 3

Publication Order Number:
HGTG30N60B3/D

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Description		Ratings	Unit
BV_{CES}	Collector to Emitter Voltage		600	V
I_C	Collector Current Continuous	T_C = 25°C	60	A
		T_C = 110°C	30	A
I_{CM}	Collector Current Pulsed (Note 1)		220	A
V_{GES}	Gate to Emitter Voltage Continuous		±20	V
V_{GEM}	Gate to Emitter Voltage Pulsed		±30	V
SSOA	Switching Safe Operating Area at T_J = 150°C (Figure 2)		60 A at 600 V	
P_D	Power Dissipation Total	T_C = 25°C	208	W
	Power Dissipation Derating	T_C > 25°C	1.67	W/°C
E_{ARV}	Reverse Voltage Avalanche Energy		100	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering		260	°C
T_{SC}	Short Circuit Withstand Time (Note 2)	V_{GE} = 12 V	4	μs
	Short Circuit Withstand Time (Note 2)	V_{GE} = 10 V	10	μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)}$ = 360 V, T_J = 125°C, R_G = 3 Ω

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Shipping
HGTG30N60B3	G30N60B3	TO−247	Tube	450/Tube

ELECTRICAL CHARACTERISTICS OF THE IGBT (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{CES}	Collector to Emitter Breakdown Voltage	I_C = 250 μA, V_{GE} = 0 V	600	–	–	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_C = −10 mA, V_{GE} = 0 V	20	–	–	V
I_{CES}	Collector to Emitter Leakage Current	V_{CE} = BV_{CES}, T_C = 25°C	–	–	250	μA
		V_{GE} = BV_{CES}, T_C = 150°C	–	–	3.0	mA
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = I_{C110}, V_{GE} = 15 V, T_C = 25°C	–	1.45	1.9	V
		I_C = I_{C110}, V_{GE} = 15 V, T_C = 150°C	–	1.7	2.1	V
$V_{GE(th)}$	Gate to Emitter Threshold Voltage	I_C = 250 μA, V_{CE} = V_{GE}	4.2	5.0	6.0	V
I_{GES}	Gate to Emitter Leakage Current	V_{GE} = ±20 V	–	–	±250	nA
SSOA	Switching SOA	T_J = 150°C, R_G = 3 Ω, V_{GE} = 15 V, L = 100 μH, $V_{CE(PK)}$ = 480 V	200		–	A
		T_J = 150°C, R_G = 3 Ω, V_{GE} = 15 V, L = 100 μH, $V_{CE(PK)}$ = 600 V	60		–	A
V_{GEP}	Gate to Emitter Plateau Voltage	I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}	–	7.2	–	V
$Q_{G(ON)}$	On−State Gate Charge	I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}, V_{GE} = 15 V	–	170	190	nC
		I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}, V_{GE} = 20 V	–	230	250	nC

ELECTRICAL CHARACTERISTICS OF THE IGBT (T_C = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$T_{d(on)I}$	Current Turn−On Delay Time	IGBT and Diode at T_J = 25°C $I_{CE} = I_{C110}$ $V_{CE} = 0.8\ BV_{CES}$ V_{GE} = 15 V $R_G = 3\ \Omega$ L = 1 mH Test Circuit (Figure 17)	–	36	–	ns
T_{rI}	Current Rise Time		–	25	–	ns
$T_{d(off)I}$	Current Turn−Off Delay Time		–	137	–	ns
T_{fI}	Current Fall Time		–	58	–	ns
E_{on1}	Turn−On Energy (Note 4)		–	500		μJ
E_{on2}	Turn−On Energy (Note 4)		–	550	800	μJ
E_{off}	Turn−Off Energy (Note 3)		–	680	900	μJ
$T_{d(on)I}$	Current Turn−On Delay Time	IGBT and Diode at T_J = 150°C $I_{CE} = I_{C110}$ $V_{CE} = 0.8\ BV_{CES}$ V_{GE} = 15 V $R_G = 3\ \Omega$ L = 1 mH Test Circuit (Figure 17)	–	32	–	ns
T_{rI}	Current Rise Time		–	24	–	ns
$T_{d(off)I}$	Current Turn−Off Delay Time		–	275	320	ns
T_{fI}	Current Fall Time		–	90	150	ns
E_{on1}	Turn−On Energy (Note 4)		–	500	–	μJ
E_{on2}	Turn−On Energy (Note 4)		–	1300	1550	μJ
E_{off}	Turn−Off Energy (Note 3)		–	1600	1900	μJ
$R_{\theta JC}$	Thermal Resistance Junction To Case		–	–	0.6	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Turn−Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0 A). All devices were tested per JEDEC Standard No. 24−1 Method for Measurement of Power Device Turn−Off Switching Loss. This test method produces the true total Turn−Off Energy Loss.
4. Values for two Turn−On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn−on loss of the IGBT only. E_{ON2} is the turn−on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in Figure 17.

TYPICAL PERFORMANCE CURVES

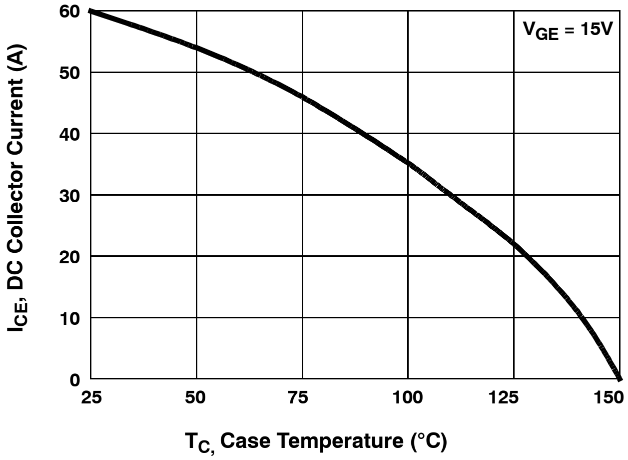


Figure 1. DC Collector Current vs. Case Temperature

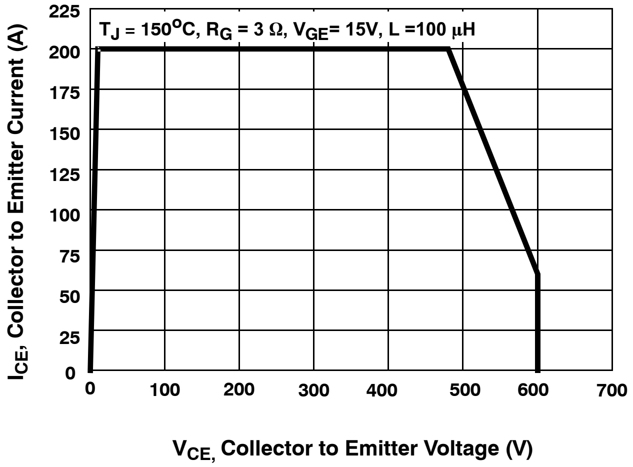


Figure 2. Minimum Switching Safe Operating Area

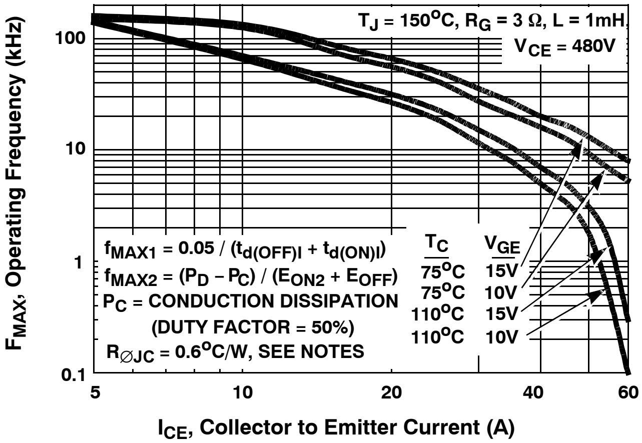


Figure 3. Operating Frequency vs. Collector to Emitter Current

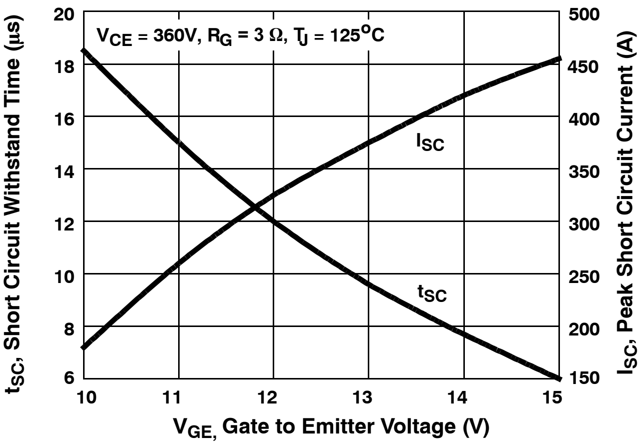


Figure 4. Short Circuit Withstand Time

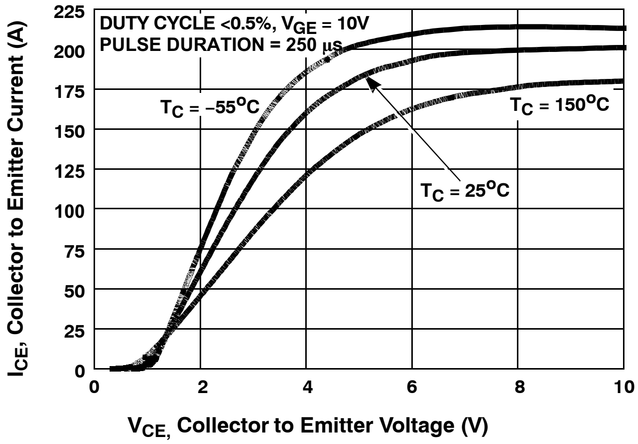


Figure 5. Collector to Emitter On−State Voltage

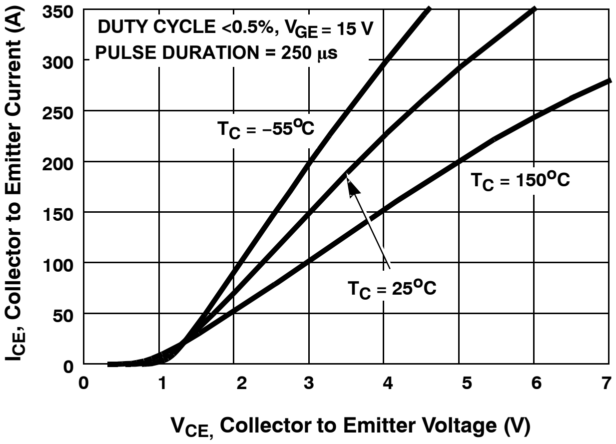


Figure 6. Collector to Emitter On−State Voltage

TYPICAL PERFORMANCE CURVES (Continued)

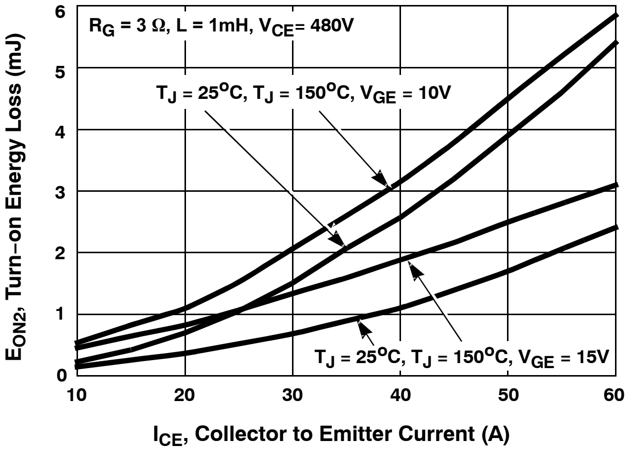


Figure 7. Turn−on Energy Loss vs. Collector to Emitter Current

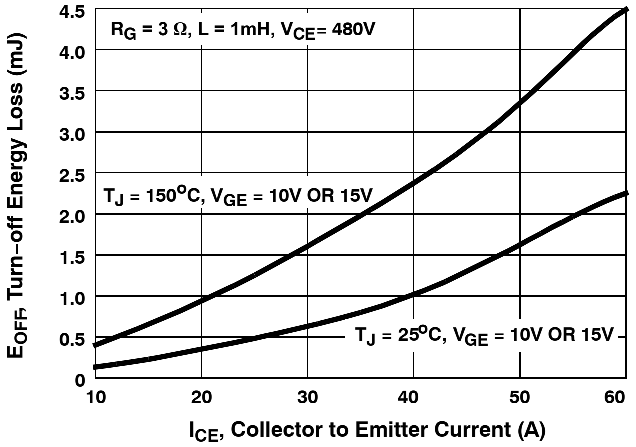


Figure 8. Turn−off Energy Loss vs. Collector to Emitter Current

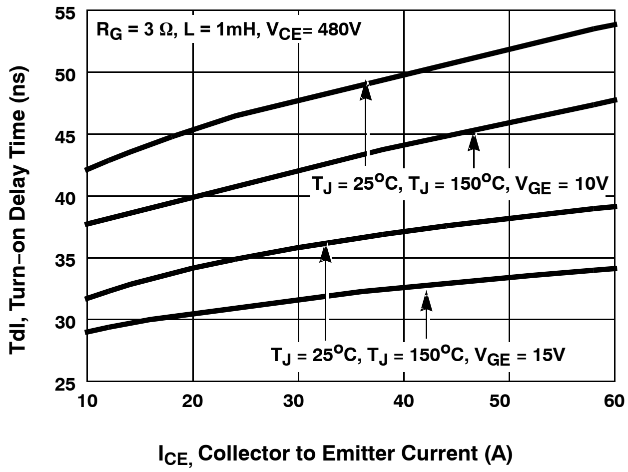


Figure 9. Turn−on Delay Time vs. Collector to Emitter Current

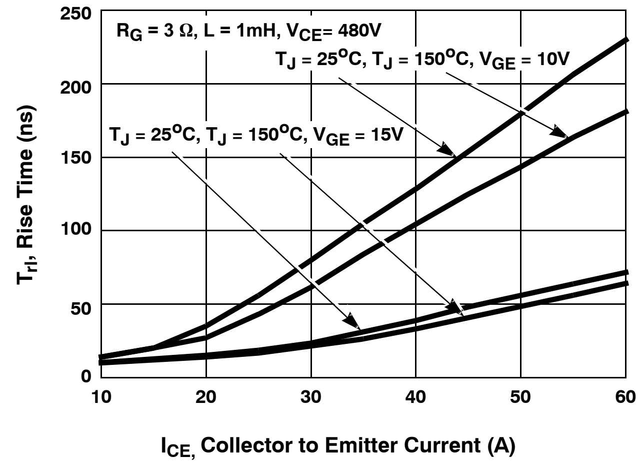


Figure 10. Turn−on Rise Time vs. Collector to Emitter Current

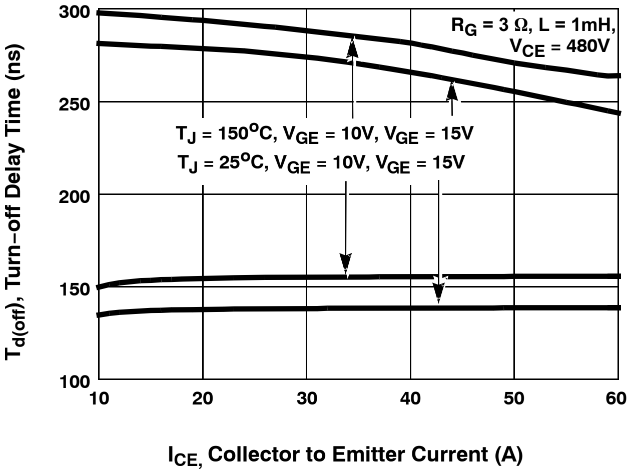


Figure 11. Turn−off Delay Time vs. Collector to Emitter Current

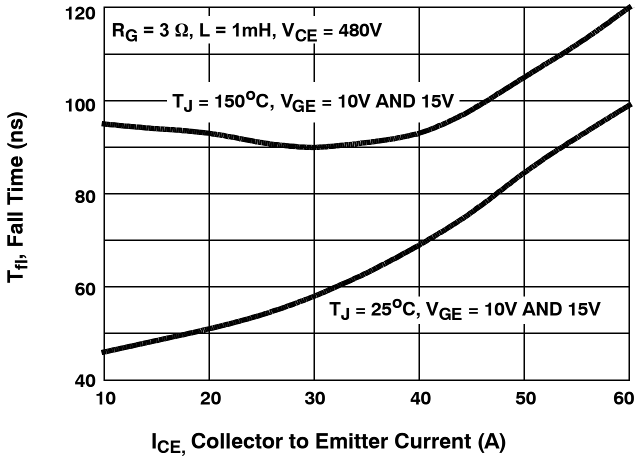


Figure 12. Fall Time vs. Collector to Emitter Current

TYPICAL PERFORMANCE CURVES (Continued)

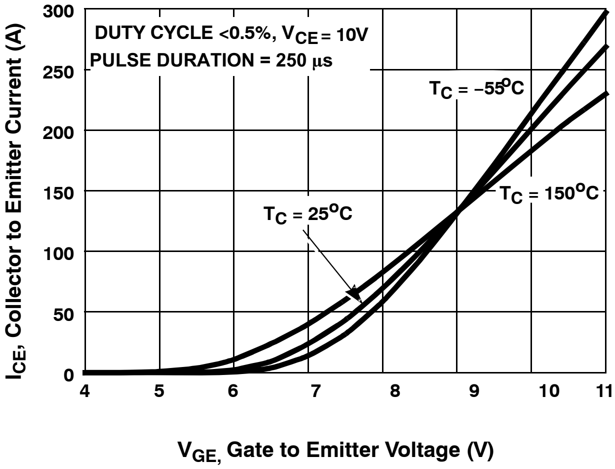


Figure 13. Transfer Characteristics

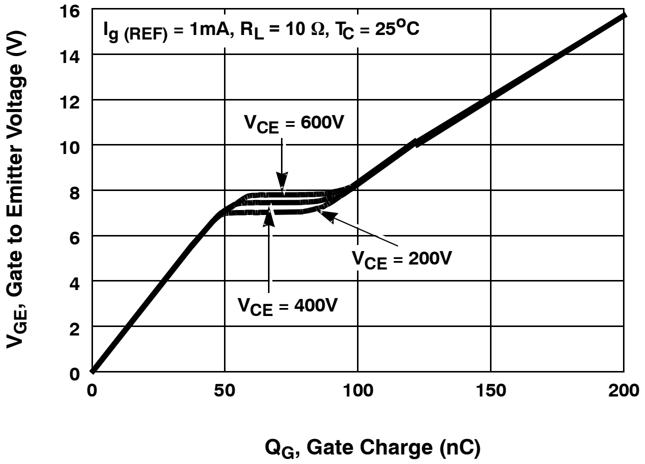


Figure 14. Gate Charge Waveforms

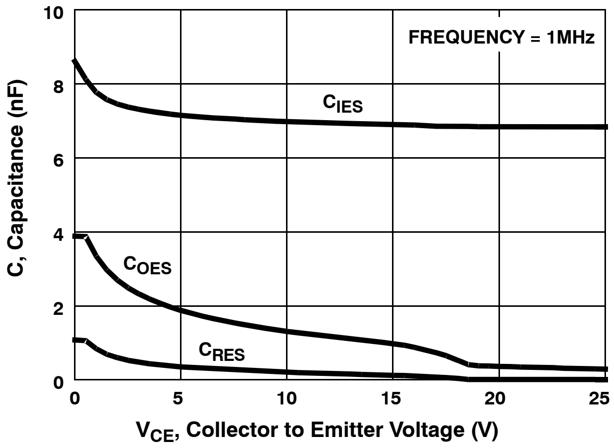


Figure 15. Capacitance vs. Collector to Emitter Voltage

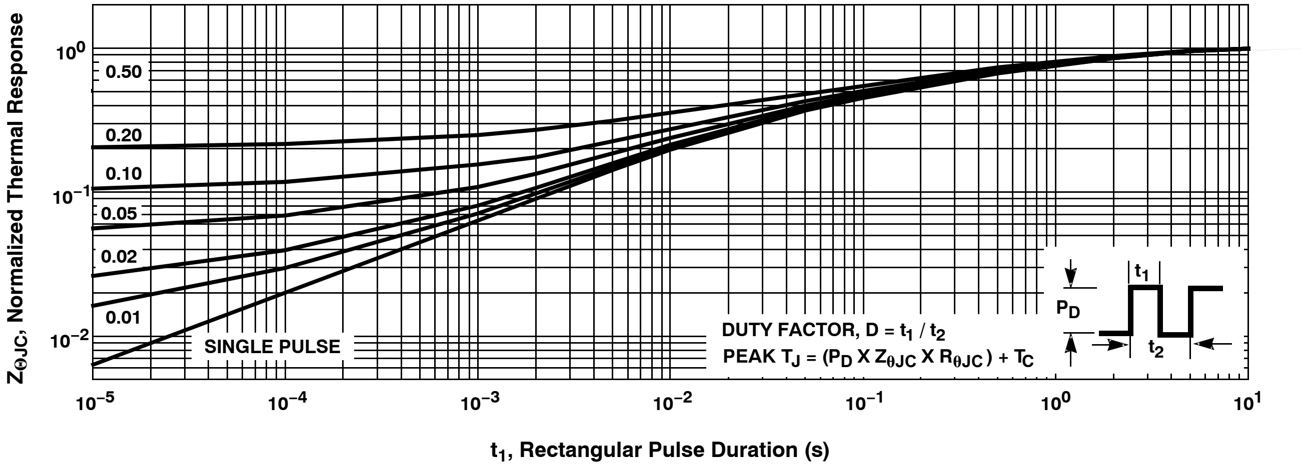


Figure 16. Normalized Transient Thermal Response, Junction to Case

TEST CIRCUITS AND WAVEFORMS

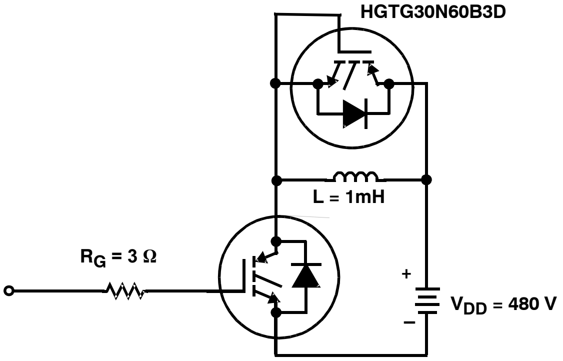


Figure 17. Inductive Switching Test Circuits

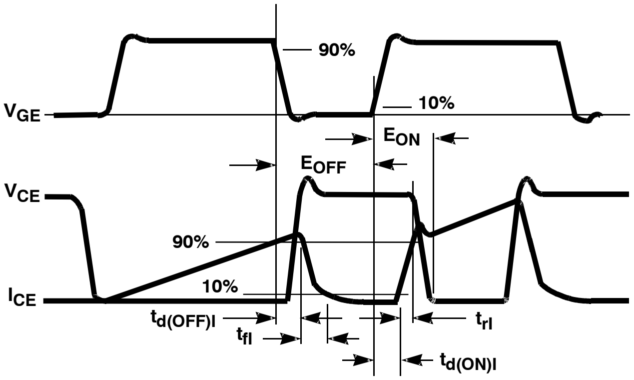


Figure 18. Switching Test Waveforms

HANDLING PRECAUTIONS FOR IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate−insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means − for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating − Never exceed the gate−voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination − The gates of these devices are essentially capacitors. Circuits that leave the gate open−circuited or floating should be avoided. These conditions can result in turn on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. Gate Protection − These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

OPERATING FREQUENCY INFORMATION

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

$f_{MAX}1$ is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on−state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 18. Device turn−off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

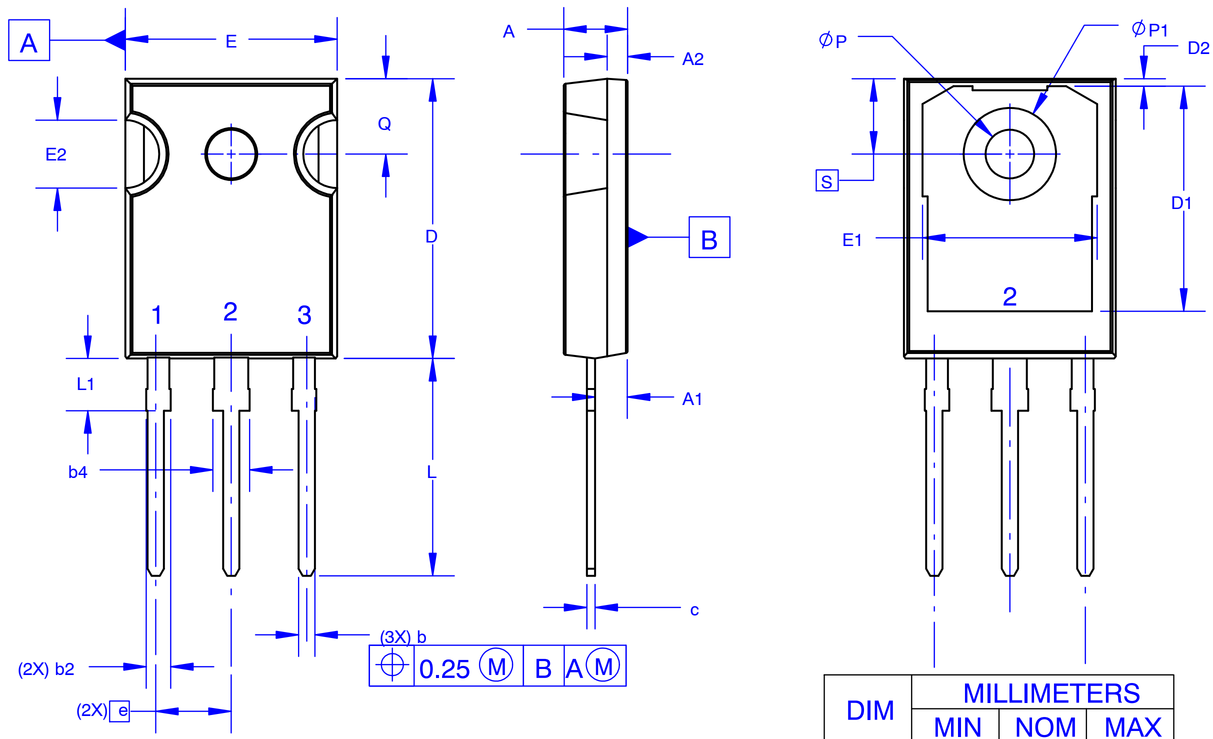
E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 18. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn−on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn−off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

GENERIC MARKING DIAGRAM*

AYWWZZ
XXXXXXX
XXXXXXX
∘

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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