ON Semiconductor®

FQB8N60C / FQI8N60C

N-Channel QFET® MOSFET

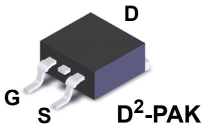
600 V, 7.5 A, 1.2 Ω

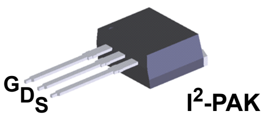
Description

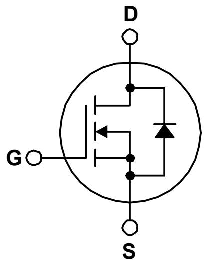
This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 7.5 A, 600 V, $R_{DS(on)}$ = 1.2 Ω (Max.) @ V_{GS} = 10 V, I_D = 3.75 A
- Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 12 pF)
- 100% Avalanche Tested
- RoHS Compliant







Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter	FQB8N60CTM / FQI8N60CTU	Unit
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current - Continuous (T_C = 25°C)	7.5	A
	- Continuous (T_C = 100°C)	4.6	A
I_{DM}	Drain Current - Pulsed (Note 1)	30	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	230	mJ
I_{AR}	Avalanche Current (Note 1)	7.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	14.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)*	3.13	W
	Power Dissipation (T_C = 25°C)	147	W
	- Derate above 25°C	1.18	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	°C

Thermal Characteristics

Symbol	Parameter	FQB8N60CTM / FQI8N60CTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in^2 Pad of 2-oz Copper), Max.	40	

October-2017,Rev.3

Publication Order Number:
FQI8N60C/D

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB8N60CTM	FQB8N60C	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units
FQI8N60CTU	FQI8N60C	I^2-PAK	Tube	N/A	N/A	50 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.7	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 480 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.75 A	--	1.0	1.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 3.75 A	--	8.7	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	965	1255	pF
C_{oss}	Output Capacitance		--	105	135	pF
C_{rss}	Reverse Transfer Capacitance		--	12	16	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 7.5A, R_G = 25 Ω (Note 4)	--	16.5	45	ns
t_r	Turn-On Rise Time		--	60.5	130	ns
$t_{d(off)}$	Turn-Off Delay Time		--	81	170	ns
t_f	Turn-Off Fall Time		--	64.5	140	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 7.5A, V_{GS} = 10 V (Note 4)	--	28	36	nC
Q_{gs}	Gate-Source Charge		--	4.5	--	nC
Q_{gd}	Gate-Drain Charge		--	12	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	30	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.5 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 7.5 A, dI_F / dt = 100 A/μs	--	365	--	ns
Q_{rr}	Reverse Recovery Charge		--	3.4	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 7.3 mH, I_{AS} = 7.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 7.5 A, di/dt $\leq$ 200 A/μs , $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

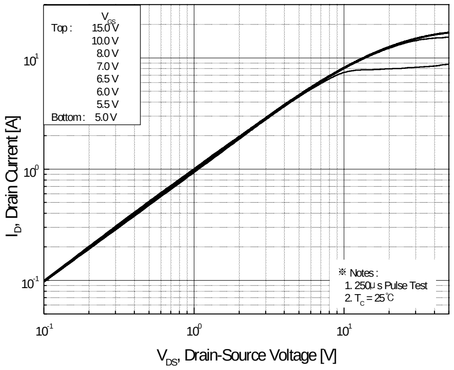


Figure 1. On-Region Characteristics

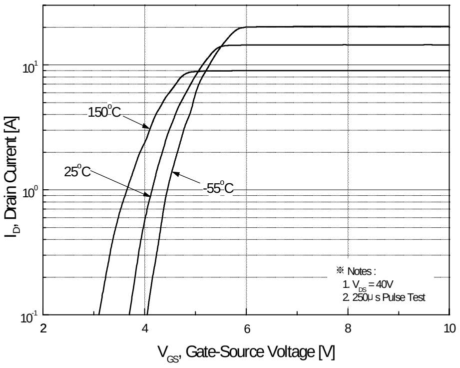


Figure 2. Transfer Characteristics

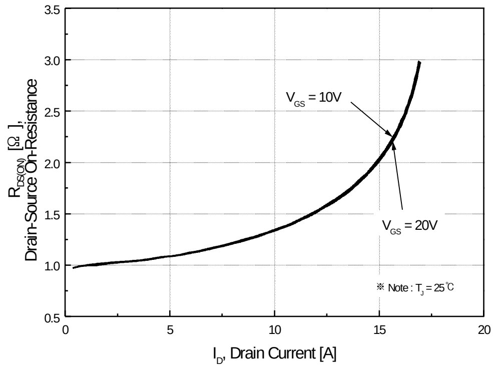


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

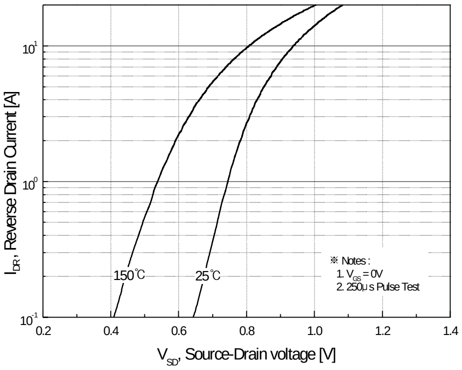


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

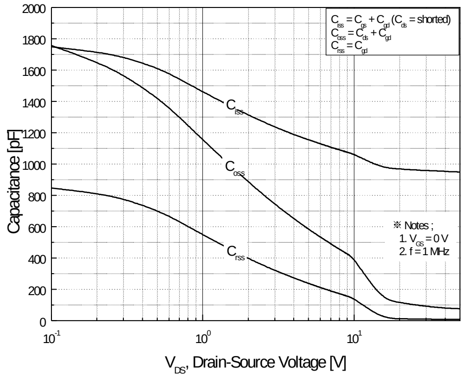


Figure 5. Capacitance Characteristics

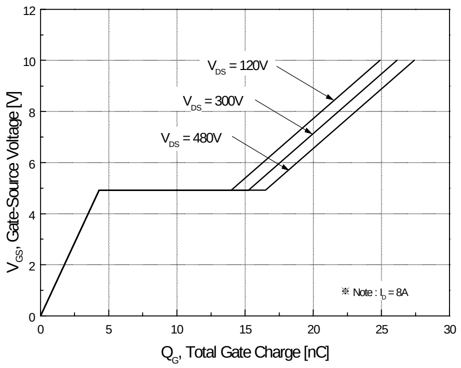


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

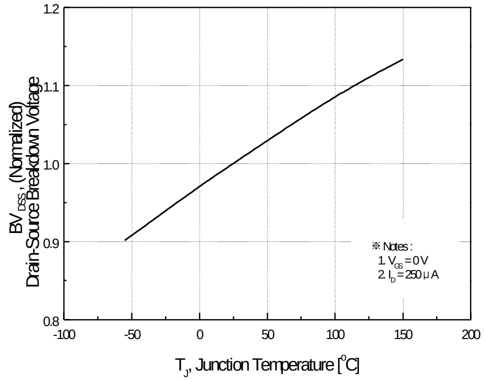


Figure 7. Breakdown Voltage Variation vs Temperature

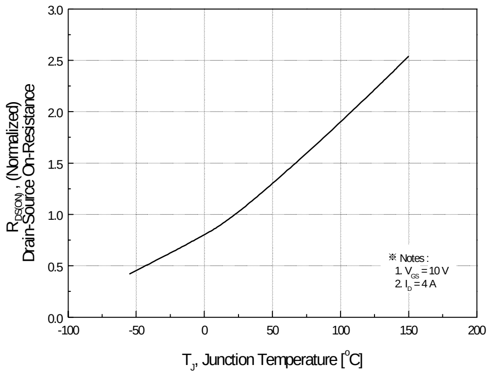


Figure 8. On-Resistance Variation vs Temperature

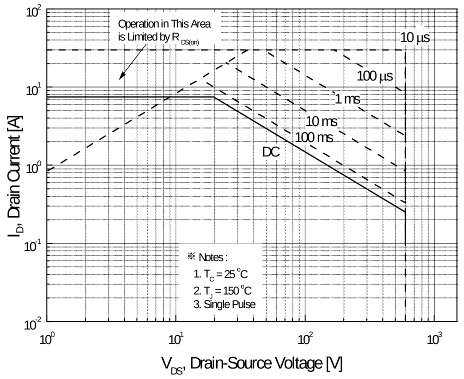


Figure 9. Maximum Safe Operating Area

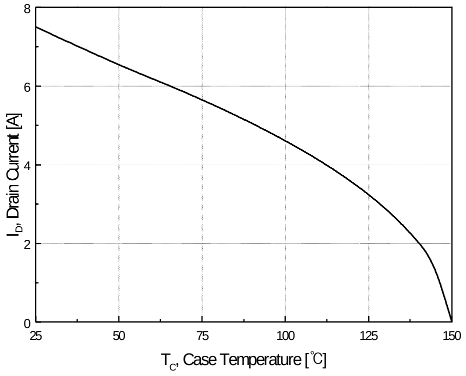


Figure 10. Maximum Drain Current vs Case Temperature

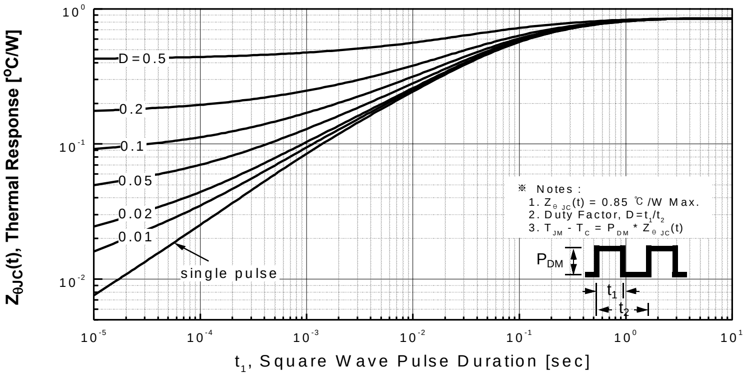


Figure 11. Transient Thermal Response Curve

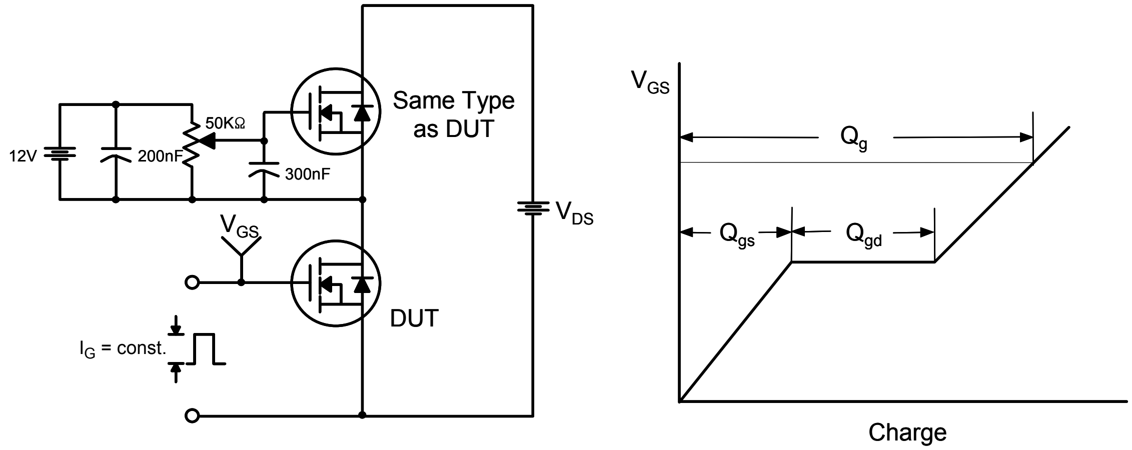


Figure 12. Gate Charge Test Circuit & Waveform

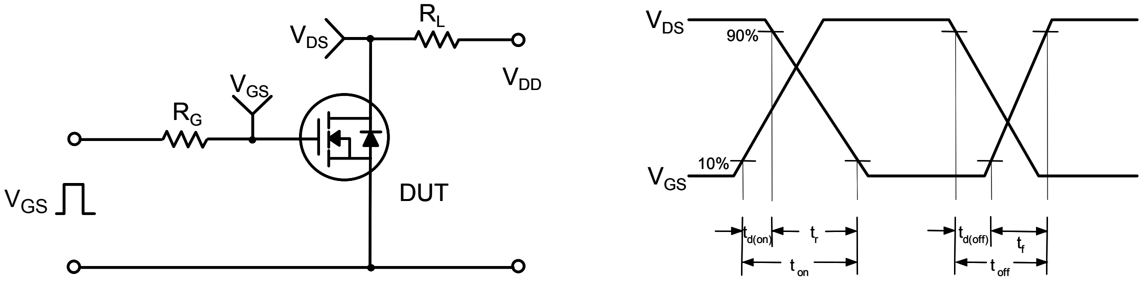


Figure 13. Resistive Switching Test Circuit & Waveforms

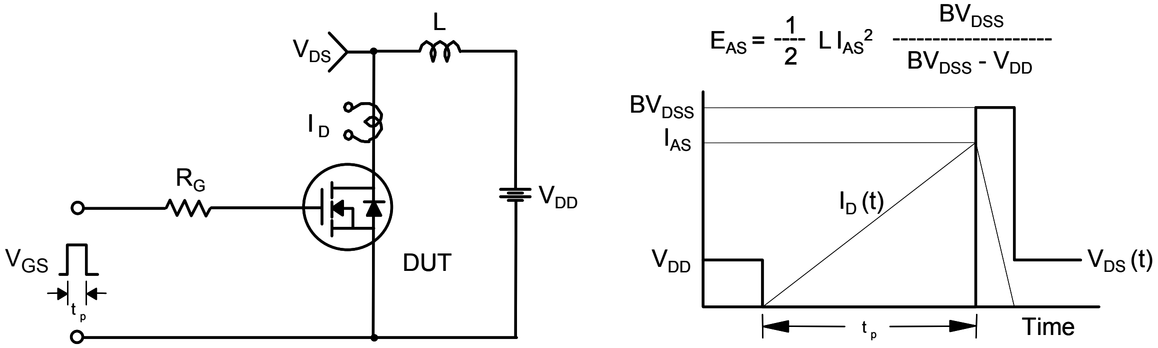


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

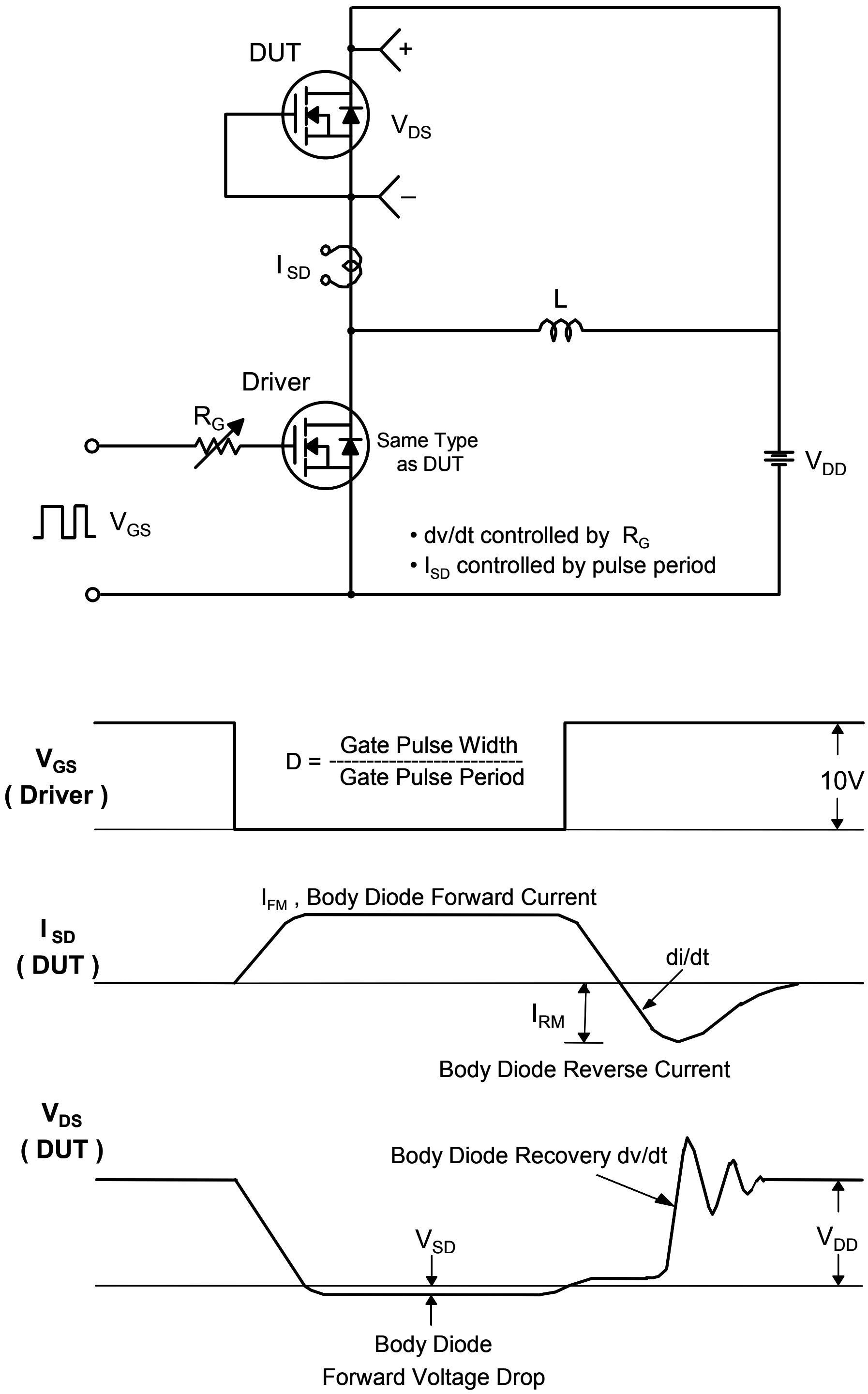
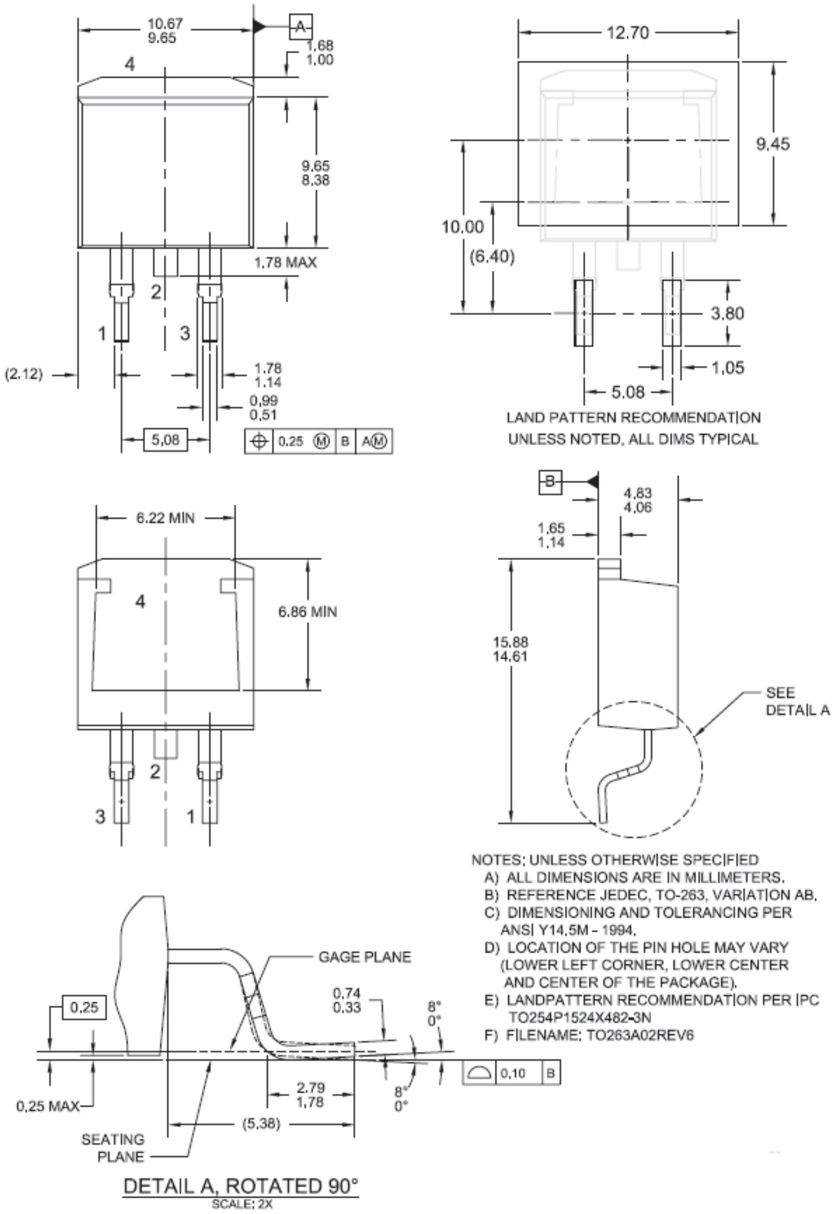


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) REFERENCE JEDEC, TO-263, VARIATION AB.
- C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.
- D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
- E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
- F) FILENAME: TO263A02REV6

Figure 16. TO263 (D^2PAK), Molded, 2-Lead, Surface Mount

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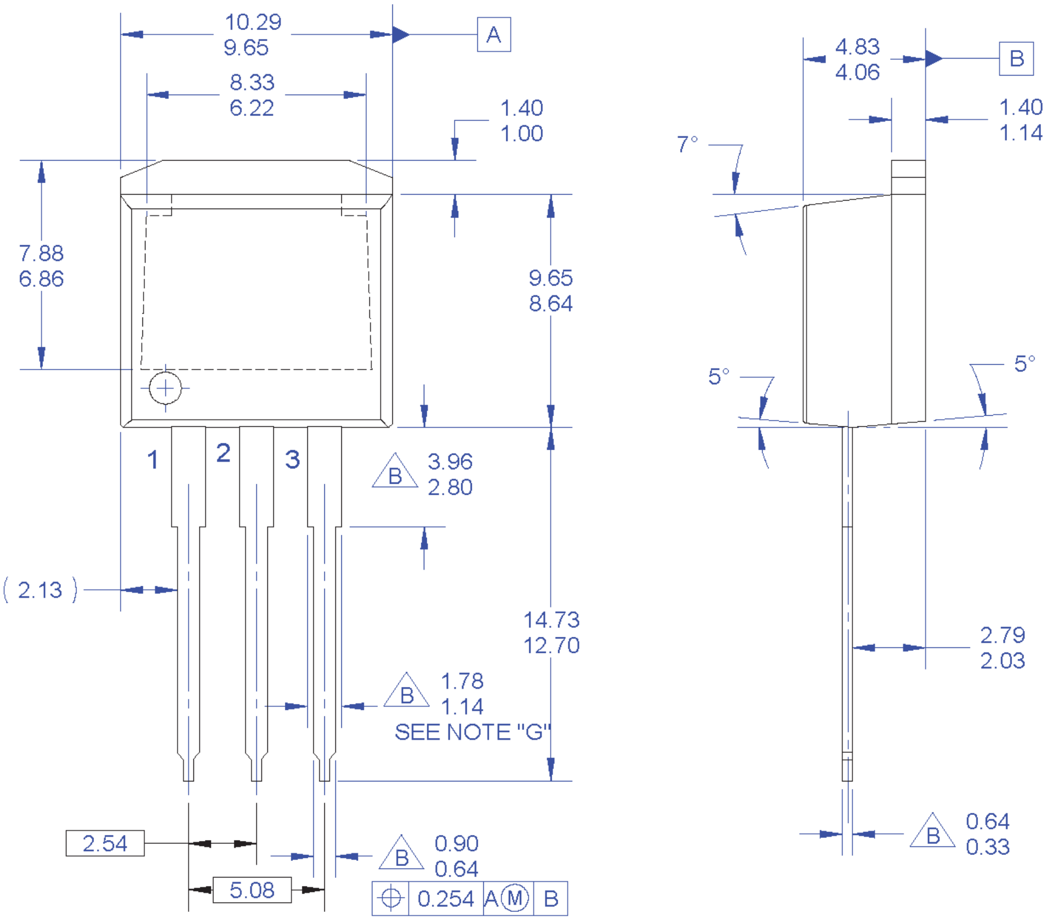
Mechanical Dimensions



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.

△B DOES NOT COMPLY JEDEC STD. VALUE.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.

F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)

G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.

H. DRAWING FILE NAME: TO262A03REV5

Figure 17. TO262 (I^{2}PAK), Molded, 3-Lead, Jedec Variation AA

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