Contents

Pinouts

Figure 1. 8-pin SOIC pinout

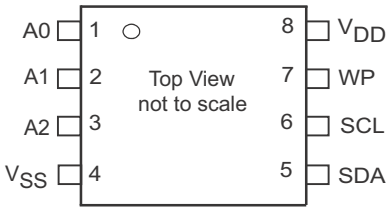
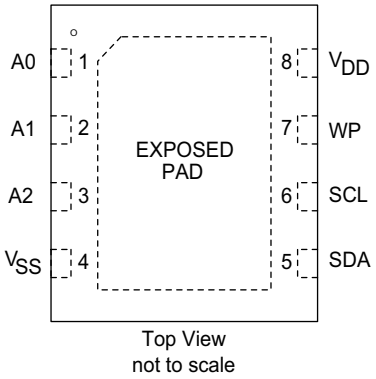


Figure 2. 8-pin DFN pinout



Pin Definitions

Pin Name	I/O Type	Description
A2–A0	Input	**Device Select Address 2–0**. These pins are used to select one of up to 8 devices of the same type on the same I^2C bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	**Serial Data/Address**. This is a bi-directional pin for the I^2C interface. It is open-drain and is intended to be wire-AND'd with other devices on the I^2C bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	**Serial Clock**. The serial clock pin for the I^2C interface. Data is clocked out of the device on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
WP	Input	**Write Protect**. When tied to V_{DD}, addresses in the entire memory map will be write-protected. When WP is connected to ground, all addresses are write enabled. This pin is pulled down internally.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.
EXPOSED PAD	No connect	The EXPOSED PAD on the bottom of 8-pin DFN package is not connected to the die. The EXPOSED PAD should not be soldered on the PCB.

Functional Overview

The FM24CL64B is a serial F-RAM memory. The memory array is logically organized as 8,192 × 8 bits and is accessed using an industry-standard I^2C interface. The functional operation of the F-RAM is similar to serial (I^2C) EEPROM. The major difference between the FM24CL64B and a serial (I^2C) EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing the FM24CL64B, the user addresses 8K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the I^2C protocol, which includes a slave address (to distinguish other non-memory devices) and a two-byte address. The upper 3 bits of the address range are 'don't care' values. The complete address of 13 bits specifies each byte address uniquely.

The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the I^2C bus. Unlike a serial (I^2C) EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in the interface section.

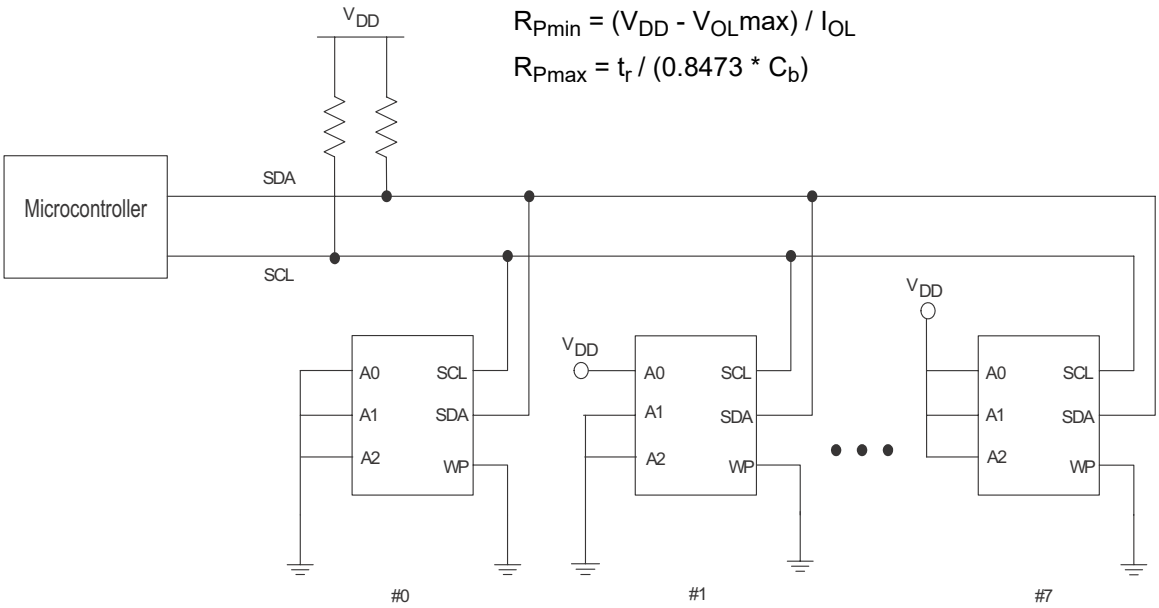
I^2C Interface

The FM24CL64B employs a bi-directional I^2C bus protocol using few pins or board space. Figure 3 illustrates a typical system configuration using the FM24CL64B in a microcontroller-based system. The industry standard I^2C bus is familiar to many users but is described in this section.

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24CL64B is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. Figure 4 on page 5 and Figure 5 on page 5 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

Figure 3. System Configuration using Serial (I^2C) nvSRAM



STOP Condition (P)

A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM24CL64B should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of SDA in order to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM24CL64B for a new operation.

If during operation the power supply drops below the specified V_{DD} minimum, the system should issue a START condition prior to performing another operation.

Figure 4. START and STOP Conditions

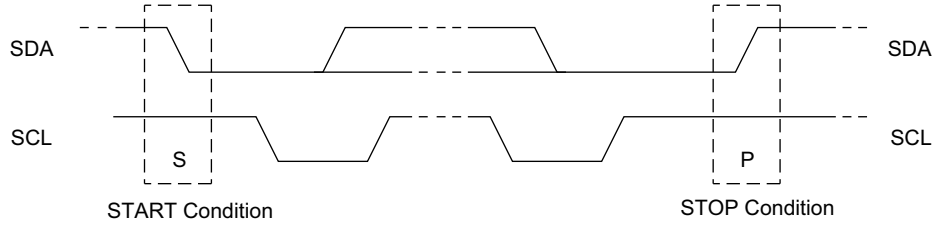
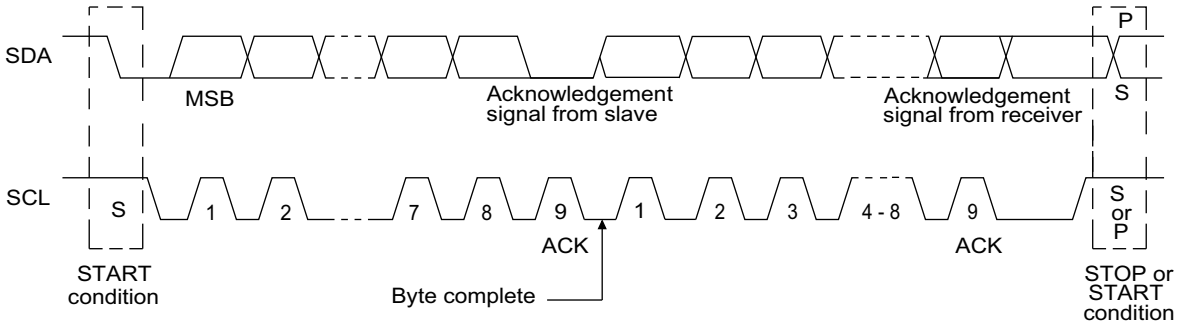


Figure 5. Data Transfer on the I²C Bus



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

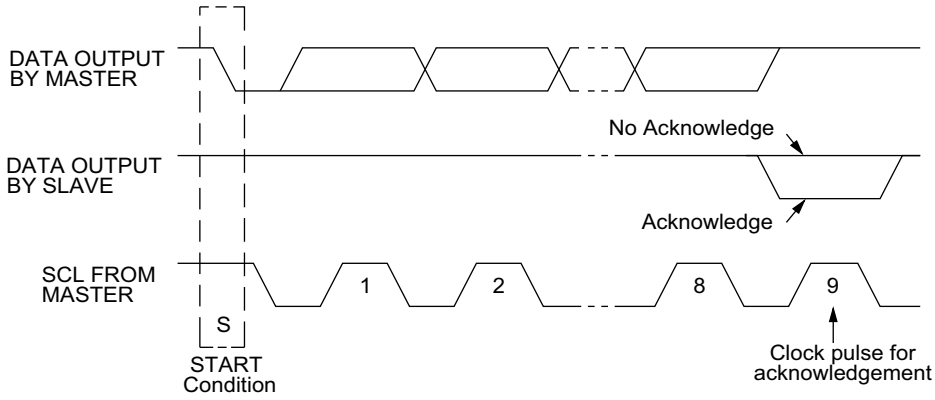
Acknowledge/No-acknowledge

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the device can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24CL64B will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM24CL64B to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Figure 6. Acknowledge on the I²C Bus

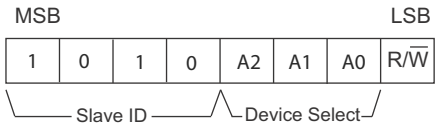


Slave Device Address

The first byte that the FM24CL64B expects after a START condition is the slave address. As shown in Figure 7, the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

Bits 7-4 are the device type (slave ID) and should be set to 1010b for the FM24CL64B. These bits allow other function types to reside on the I^2C bus within an identical address range. Bits 3-1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to eight FM24CL64B devices can reside on the same I^2C bus by assigning a different address to each. Bit 0 is the read/write bit (R/W). R/W = '1' indicates a read operation and R/W = '0' indicates a write operation.

Figure 7. Memory Slave Device Address



Addressing Overview

After the FM24CL64B (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 13-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24CL64B increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (1FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM24CL64B can begin. For a read operation the FM24CL64B will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM24CL64B will transfer the next sequential byte. If the acknowledge is not sent, the FM24CL64B will end the read operation. For a write operation, the FM24CL64B will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24CL64B is designed to operate in a manner very similar to other I^2C interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM24CL64B and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/W bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 1FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM24CL64B uses no page buffering.

The memory array can be write-protected using the WP pin. Setting the WP pin to a HIGH condition (V_{DD}) will write-protect all addresses. The FM24CL64B will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a LOW state (V_{SS}) will disable the write protect. WP is pulled down internally.

Figure 8 and Figure 9 on page 7 below illustrate a single-byte and multiple-byte write cycles.

Figure 8. Single-Byte Write

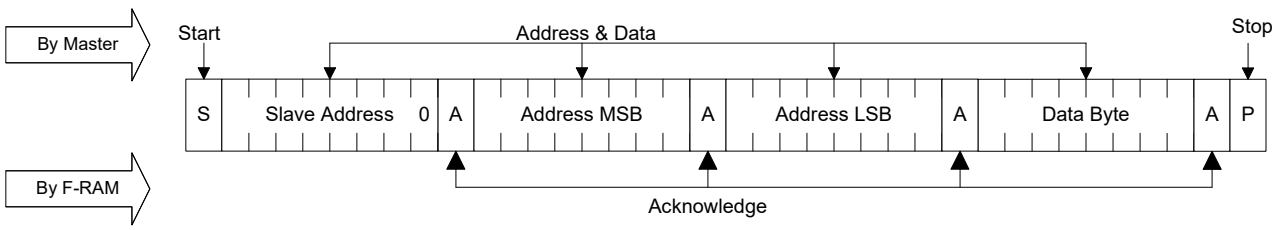
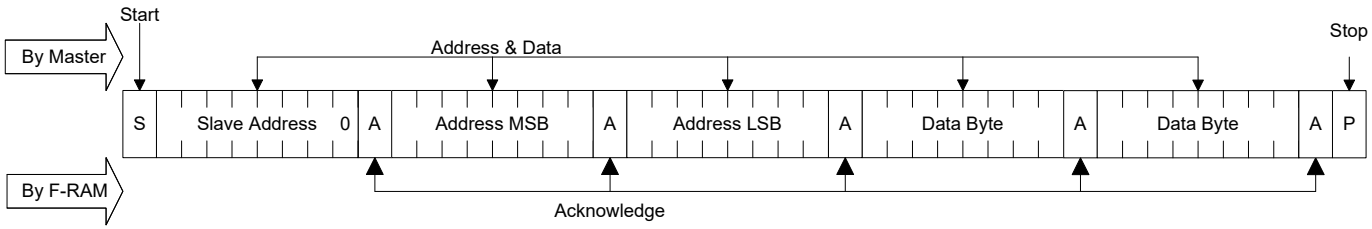


Figure 9. Multi-Byte Write



Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM24CL64B uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM24CL64B uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM24CL64B will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM24CL64B should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24CL64B attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 1FFFh, it will wrap around to 0000h on the next read cycle. Figure 10 and Figure 11 below show the proper operation for current address reads.

Figure 10. Current Address Read

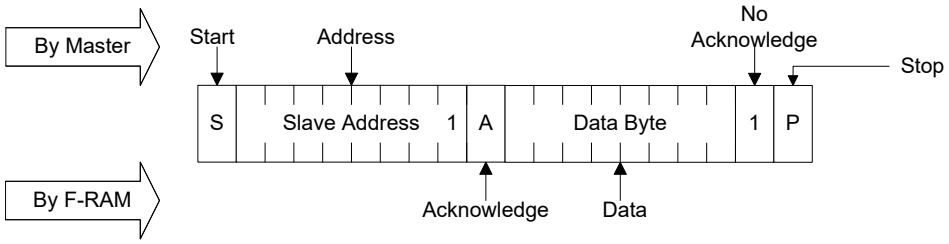
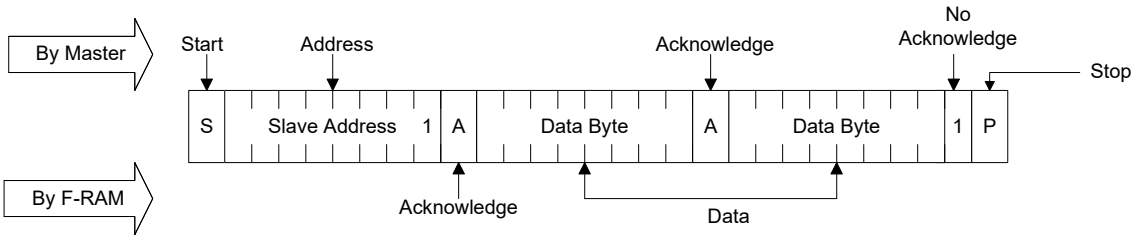


Figure 11. Sequential Read

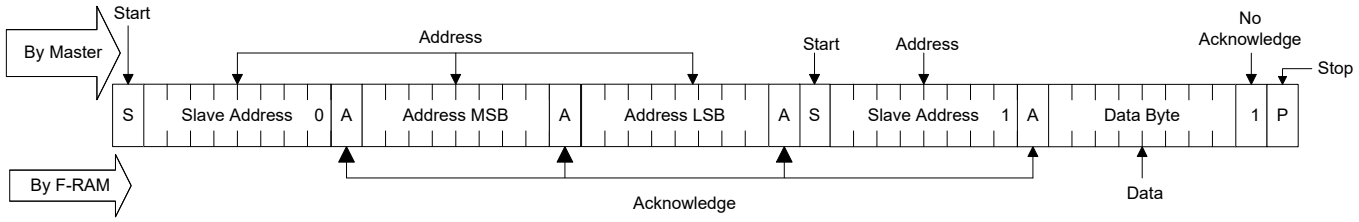


Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB (R/W) set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM24CL64B acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 12. Selective (Random) Read



Endurance

The FM24C64B internally operates with a read and restore mechanism. Therefore, endurance cycles are applied for each read or write cycle. The memory architecture is based on an array of rows and columns. Each read or write access causes an endurance cycle for an entire row. In the FM24C64B, a row is 64 bits wide. Every 8-byte boundary marks the beginning of a new row. Endurance can be optimized by ensuring frequently accessed data is located in different rows. Regardless, FRAM read and write endurance is effectively unlimited at the 1MHz I^2C speed. Even at 3000 accesses per second to the same segment, 10 years time will elapse before 1 trillion endurance cycles occur.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 10 Years

Ambient temperature
with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +5.0 V

Input voltage ..... –1.0 V to + 5.0 V and $V_{IN} < V_{DD} + 1.0$ V

DC voltage applied to outputs
in High-Z state ..... –0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns)
on any pin to ground potential ..... –2.0 V to V_{DD} + 2.0 V

Package power dissipation capability
(T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature
(10 seconds) ..... +260 °C

Electrostatic Discharge Voltage [1]
Human Body Model (AEC-Q100-002 Rev. E) ..... 2 kV
Charged Device Model (AEC-Q100-011 Rev. B) ..... 500 V

Latch-up current ..... > 140 mA

* Exception: The "$V_{IN} < V_{DD} + 1.0$ V" restriction does not apply to the SCL and SDA inputs.

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.7 V to 3.65 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [2]	Max	Unit
V_{DD}	Power supply			2.7	3.3	3.65	V
I_{DD}	Average V_{DD} current	SCL toggling between V_{DD} – 0.3 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.3 V.	f_{SCL} = 100 kHz	–	–	100	µA
			f_{SCL} = 400 kHz	–	–	170	µA
			f_{SCL} = 1 MHz	–	–	300	µA
I_{SB}	Standby current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	3	6	µA
I_{LI}	Input leakage current (Except WP and A2–A0)	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+1	µA
	Input leakage current (for WP and A2–A0)	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+100	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+1	µA
V_{IH}	Input HIGH voltage			0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage			–0.3	–	0.3 × V_{DD}	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA		–	–	0.4	V
R_{in} [3]	Input resistance (WP, A2–A0)	For $V_{IN} = V_{IL\ (Max)}$		40	–	–	kΩ
		For $V_{IN} = V_{IH\ (Min)}$		1	–	–	MΩ
V_{HYS} [4]	Input hysteresis			0.05 × V_{DD}	–	–	V

Notes
1. Electrostatic Discharge voltages specified in the datasheet are the JEDEC standard limits used for qualifying the device. To know the maximum value device passes for, please refer to the device qualification report available on the website.
2. Typical values are at 25 °C, $V_{DD} = V_{DD}$ (typ). Not 100% tested.
3. The input pull-down circuit is strong (40 kΩ) when the input voltage is below V_{IL} and weak (1 MΩ) when the input voltage is above V_{IH}.
4. This parameter is guaranteed by design and is not tested.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

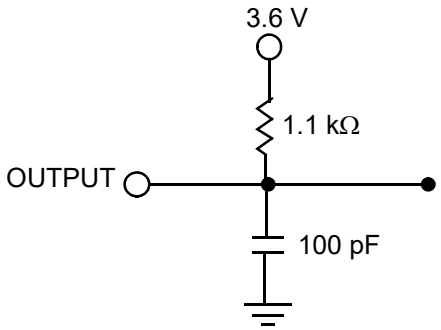
Parameter [5]	Description	Test Conditions	Max	Unit
C_O	Output pin capacitance (SDA)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	8	pF
C_I	Input pin capacitance		6	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	8-pin SOIC	8-pin DFN	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	147	28	°C/W
Θ_{JC}	Thermal resistance (junction to case)		47	30	°C/W

AC Test Loads and Waveforms

Figure 13. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels .....10% and 90% of V_{DD}
Input rise and fall times .....10 ns
Input and output timing reference levels .....0.5 × V_{DD}
Output load capacitance ..... 100 pF

Note
5. This parameter is periodically sampled and not 100% tested.

AC Switching Characteristics

Over the Operating Range

Parameter [6]		Description	Min	Max	Min	Max	Min	Max	Unit
Cypress Parameter	Alt. Parameter								
f_{SCL}[7]		SCL clock frequency	–	0.1	–	0.4	–	1.0	MHz
$t_{SU;\ STA}$		Start condition setup for repeated Start	4.7	–	0.6	–	0.25	–	µs
$t_{HD;STA}$		Start condition hold time	4.0	–	0.6	–	0.25	–	µs
t_{LOW}		Clock LOW period	4.7	–	1.3	–	0.6	–	µs
t_{HIGH}		Clock HIGH period	4.0	–	0.6	–	0.4	–	µs
$t_{SU;DAT}$	$t_{SU;DATA}$	Data in setup	250	–	100	–	100	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	–	0	–	ns
t_{DH}		Data output hold (from SCL @ V_{IL})	0	–	0	–	0	–	ns
t_R[8]	t_r	Input rise time	–	1000	–	300	–	300	ns
t_F[8]	t_f	Input fall time	–	300	–	300	–	100	ns
$t_{SU;STO}$		STOP condition setup	4.0	–	0.6	–	0.25	–	µs
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	3	–	0.9	–	0.55	µs
t_{BUF}		Bus free before new transmission	4.7	–	1.3	–	0.5	–	µs
t_{SP}		Noise suppression time constant on SCL, SDA	–	50	–	50	–	50	ns

Figure 14. Read Bus Timing Diagram

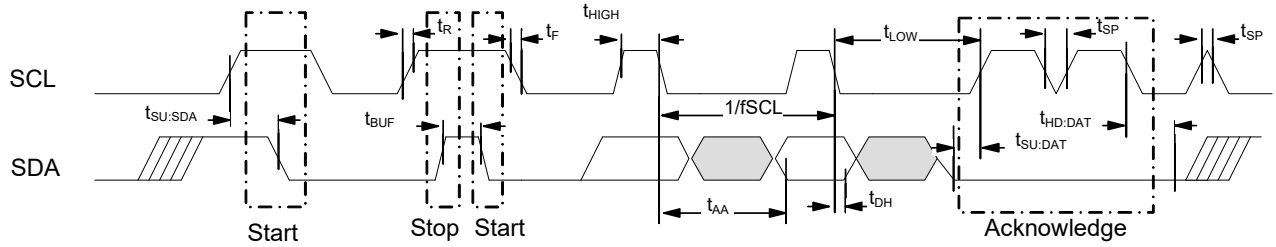
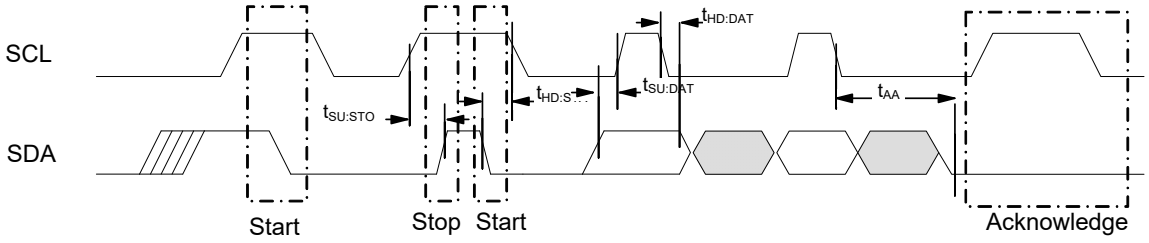


Figure 15. Write Bus Timing Diagram



Notes

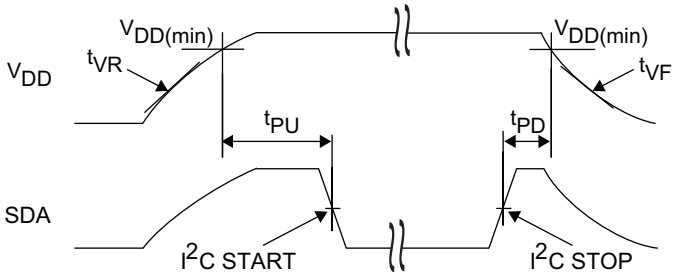
6. Test conditions assume signal transition time of 10 ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0 to V_{DD}(typ), and output loading of the specified I_{OL} and load capacitance shown in Figure 13.
7. The speed-related specifications are guaranteed characteristic points along a continuous curve of operation from DC to f_{SCL} (max).
8. These parameters are guaranteed by design and are not tested.

Power Cycle Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up V_{DD}(min) to first access (START condition)	1	–	ms
t_{PD}	Last access (STOP condition) to power-down (V_{DD}(min))	0	–	µs
t_{VR} [9, 10]	V_{DD} power-up ramp rate	30	–	µs/V
t_{VF} [9, 10]	V_{DD} power-down ramp rate	30	–	µs/V

Figure 16. Power Cycle Timing



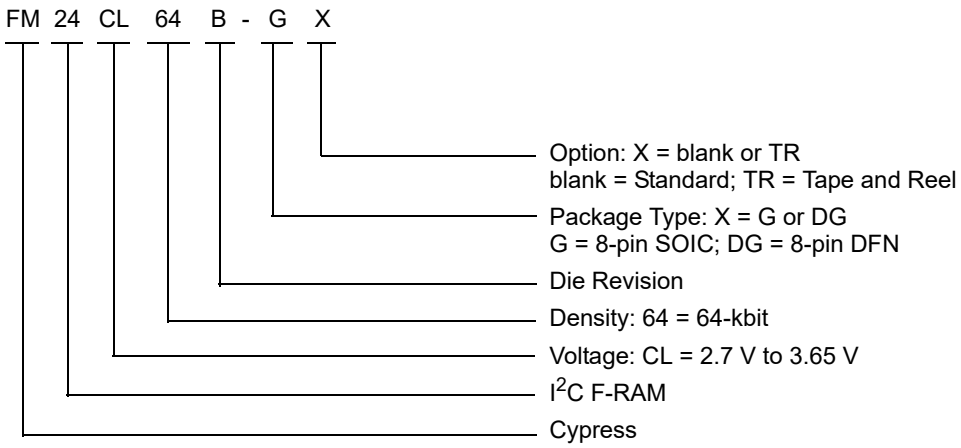
Note
9. Slope measured at any point on the V_{DD} waveform.
10. Guaranteed by design.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM24CL64B-G	51-85066	8-pin SOIC	Industrial
FM24CL64B-GTR			
FM24CL64B-DG	001-85260	8-pin DFN	
FM24CL64B-DGTR			

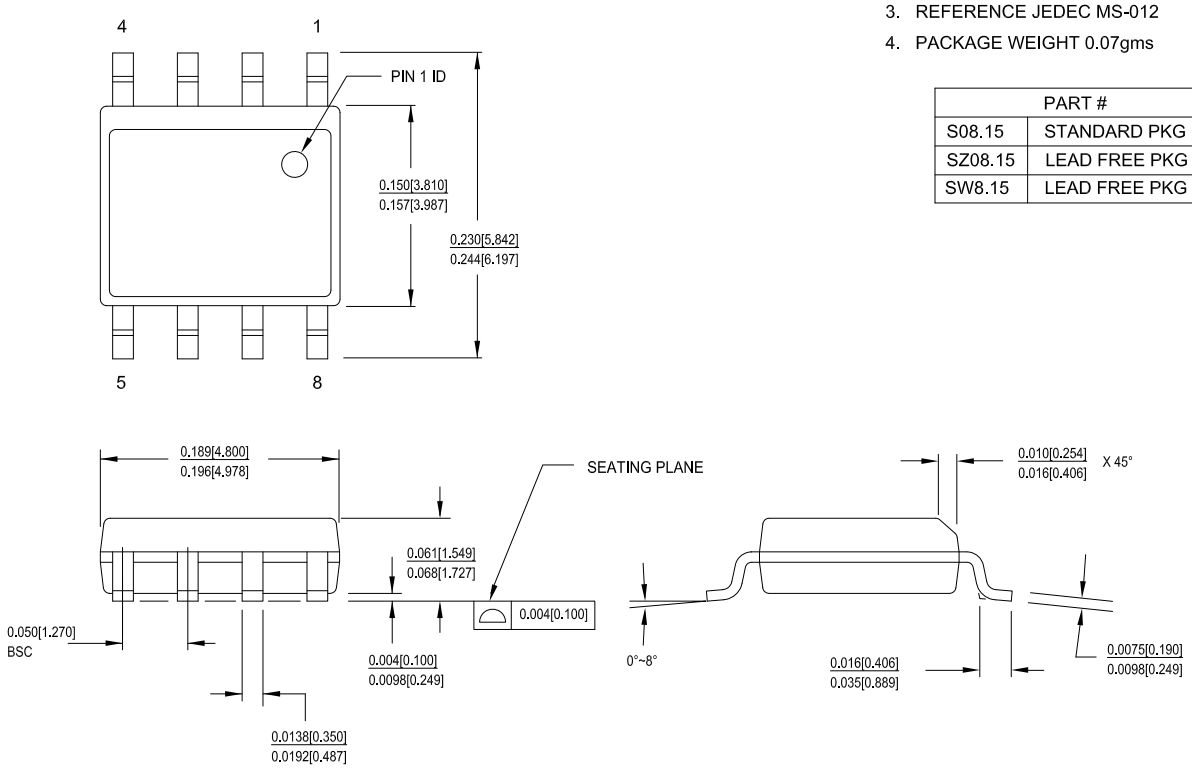
All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



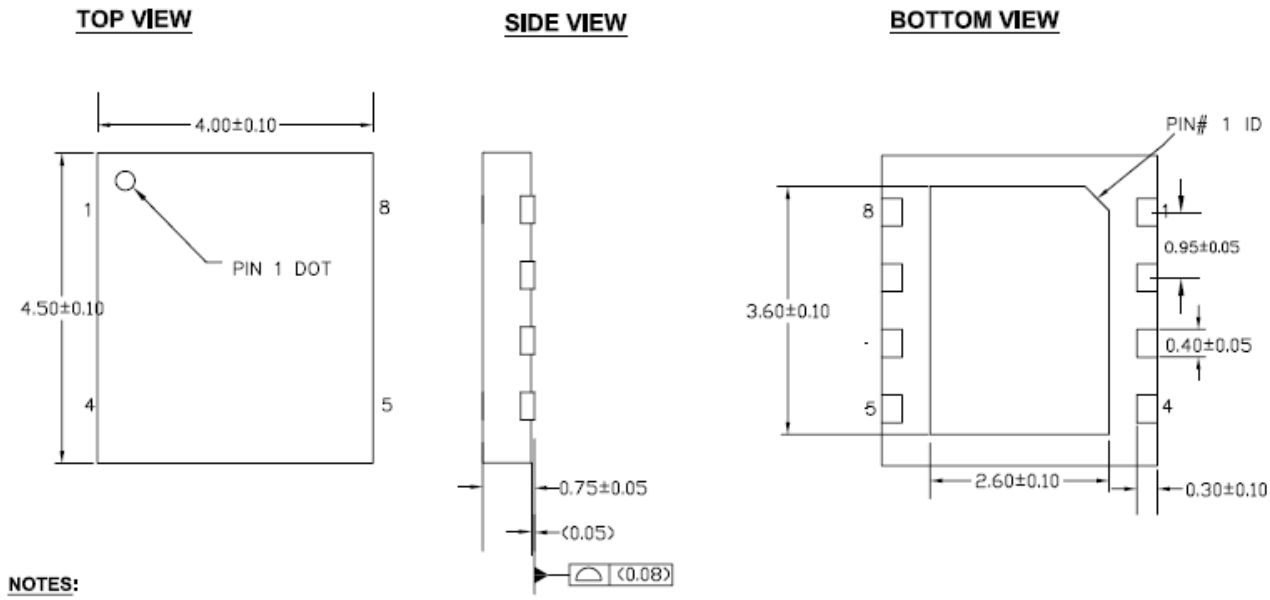
Package Diagrams

Figure 17. 8-pin SOIC (150 Mils) Package Outline, 51-85066



Package Diagrams (continued)

Figure 18. 8-pin DFN (4.0 × 4.5 × 0.8 mm) Package Outline, 001-85260



NOTES:

1. REFERENCE JEDEC # MO-229F
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-85260 *B

Acronyms

Acronym	Description
ACK	Acknowledge
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	No Acknowledge
RoHS	Restriction of Hazardous Substances
R/$\overline{W}$	Read/Write
SCL	Serial Clock Line
SDA	Serial Data Access
SOIC	Small Outline Integrated Circuit
WP	Write Protect
DFN	Dual Flat No-lead

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
Kb	1024 bit
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM24CL64B, 64-Kbit (8K × 8) Serial (I^2C) F-RAM Document Number: 001-84458				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3902082	GVCH	02/25/2013	New spec.
*A	3924523	GVCH	03/07/2013	Updated Power Cycle Timing: Changed minimum value of t_{PU} parameter from 10 ms to 1 ms.
*B	3996669	GVCH	05/13/2013	Added Appendix A - Errata for FM24CL64B.
*C	4045469	GVCH	06/30/2013	Removed Errata (All errata items are fixed).
*D	4283420	GVCH	02/19/2014	Updated Pinouts: Updated Figure 2 (Added EXPOSED PAD details). Updated Pin Definitions: Added EXPOSED PAD pin and its corresponding details. Updated Maximum Ratings: Added “Maximum Junction Temperature” and its corresponding details. Added “DC voltage applied to outputs in High-Z state” and its corresponding details. Added “Transient voltage (< 20 ns) on any pin to ground potential” and its corresponding details. Added “Package power dissipation capability (T_A = 25 °C)” and its corresponding details. Added “Latch-up Current” and its corresponding details. Removed “Package Moisture Sensitivity Level” and its corresponding details. Updated DC Electrical Characteristics: Removed existing details of I_{LI} parameter and splitted I_{LI} parameter into two rows namely “Input leakage current (Except WP and A2–A0)” and “Input leakage current (for WP and A2–A0)” and added corresponding values. Updated Data Retention and Endurance: Removed details of T_{DR} parameter corresponding to “T_A = +80 °C”. Added details of T_{DR} parameter corresponding to “T_A = 65 °C”. Added NV_C parameter and its details. Added Thermal Resistance. Updated Package Diagrams: Removed SOIC Package Marking Scheme. Removed “Ramtron Revision History”. Updated to Cypress template. Completing Sunset Review.
*E	4564960	GVCH	11/10/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*F	4771539	GVCH	05/20/2015	Replaced “TDFN” with “DFN” in all instances across the document. Updated Pin Definitions: Updated details in “Description” column corresponding to “EXPOSED PAD”. Updated Ordering Information: Fixed Typo (Replaced “001-85066” with “51-85066” in “Package Diagram” column). Updated part numbers (Added part numbers namely FM24CL64B-DG, and FM24CL64B-DGTR). Updated Package Diagrams: spec 51-85066 – Changed revision from *F to *G. spec 001-85260 – Changed revision from *A to *B. Updated to new template.

Document History Page (continued)

Document Title: FM24CL64B, 64-Kbit (8K × 8) Serial (I^2C) F-RAM Document Number: 001-84458				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	4874624	ZSK / PSR	08/06/2015	Updated Maximum Ratings: Removed “Maximum junction temperature” and its corresponding details. Added “Maximum accumulated storage time” and its corresponding details. Added “Ambient temperature with power applied” and its corresponding details.
*H	5606521	GVCH	01/27/2017	Updated Maximum Ratings: Updated Electrostatic Discharge Voltage (in compliance with AEC-Q100 standard): Changed value of “Human Body Model” from 4 kV to 2 kV. Changed value of “Charged Device Model” from 1.25 kV to 500 V. Removed “Machine Model” related information. Updated Package Diagrams: spec 51-85066 – Changed revision from *G to *H. Updated to new template. Completing Sunset Review.
*I	5703890	GVCH	04/20/2017	Updated Maximum Ratings: Added Note 1 and referred the same note in “Electrostatic Discharge Voltage”. Updated to new template.
*J	6105573	GVCH	03/21/2018	Updated Package Diagrams: spec 51-85066 – Changed revision from *H to *I. Updated to new template.
*K	6306327	GVCH	12/05/2018	Updated Maximum Ratings: Replaced “–55 °C to +125 °C” with “–65 °C to +125 °C” in ratings corresponding to “Storage temperature”. Updated to new template.

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