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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	$I_{PP\_I/O}$	±6	A	I/O to V_{SS}, 8/20µs
Peak Pulse Power, per IEC 61000-4-5	$P_{PP\_I/O}$	55	W	I/O to V_{SS}, 8/20µs
Operating Voltage (DC)	V_{DC}	5.5	V	I/O to V_{SS}
ESD Protection – Contact Discharge, per IEC 61000-4-2	$V_{ESD\_I/O}$	±16	kV	I/O to V_{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	$V_{ESD\_I/O}$	+27/-19	kV	I/O to V_{SS}
Operating Temperature	T_{OP}	-55 to +85	°C	–
Storage Temperature	T_{STG}	-55 to +150	°C	–

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	300	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	417	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	–	–	5.0	V	V_{CC} to V_{SS}
Reverse Current (Note 6)	$I_{R(V_{cc}\ to\ V_{ss})}$	–	–	1.0	µA	$V_R = V_{RWM}$ = 5V, V_{CC} to V_{SS}
Reverse Current (Note 6)	$I_{R(IO\ to\ V_{ss})}$	–	–	0.5	µA	$V_R = V_{RWM}$ = 5V, any I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	6.2	–	–	V	I_R = 1mA, V_{CC} to V_{SS}
Forward Clamping Voltage	V_F	-1.0	-0.8	–	V	I_F = -15mA, V_{CC} to V_{SS}
Reverse Clamping Voltage(Note 7)	V_{C_Vcc}	–	6.3	–	V	I_{PP} = 9A, V_{CC} to V_{SS}, 8/20 µs
	$V_{C\_I/O}$	–	7.7	9	V	I_{PP} = 6A, I/O to V_{SS}, 8/20 µs
ESD Clamping Voltage	V_{ESD_Vcc}	–	6.8	–	V	TLP, 10A, tp = 100 ns, V_{CC} to V_{SS}, per Fig. 8
	$V_{ESD\_I/O}$	–	9	–	V	TLP, 10A, tp = 100 ns, I/O to V_{SS}, per Fig. 8
Dynamic Resistance	R_{DIF_Vcc}	–	0.1	–	Ω	TLP, 10A, tp = 100 ns, V_{CC} to V_{SS}
	$R_{DIF\_I/O}$	–	0.25	–	Ω	TLP, 10A, tp = 100 ns, I/O to V_{SS}
Channel Input Capacitance	$C_{I/O\ to\ V_{SS}}$	–	0.65	0.8	pF	V_R = 2.5V, V_{CC} = 5V, f = 1MHz
Variation of Channel Input Capacitance	$\Delta C_{I/O}$	–	0.02	–	pF	V_{CC} = 5V, V_{SS} = 0V, I/O = 2.5V, f = 1MHz, T = +25°C , I/O_x to V_{SS} – I/O_y to V_{SS}

Notes:
5. Device mounted on Polymide PCB pad layout (2oz copper) as shown on Diodes Inc. suggested pad layout AP02001, which can be found on our website at http://www.diodes.com.
6. Short duration pulse test used to minimize self-heating effect.
7. Clamping voltage value is based on an 8x20µs peak pulse current (I_{pp}) waveform.

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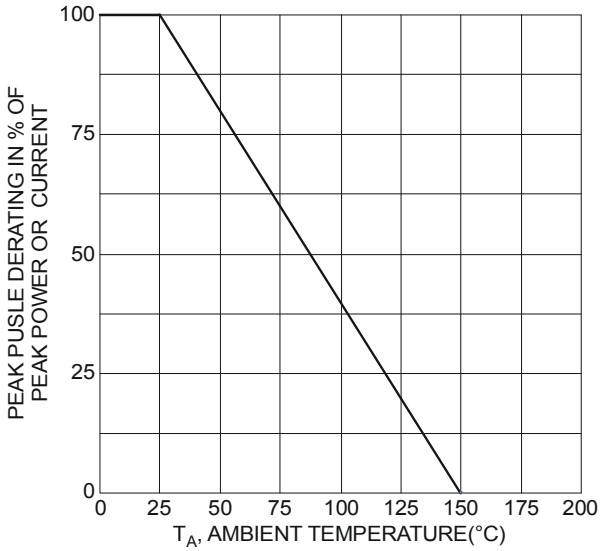

Figure 1 Pulse Derating Curve

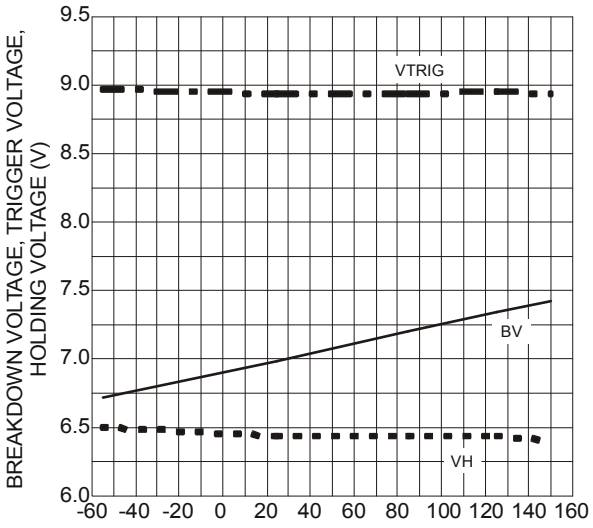

Figure 2 Breakdown Voltage, Trigger Voltage, Holding Voltage vs. Ambient Temperature

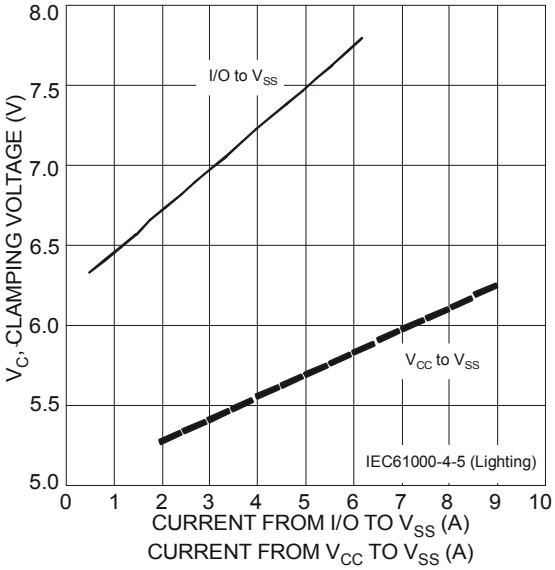

Figure 3 Clamping Voltage Characteristics

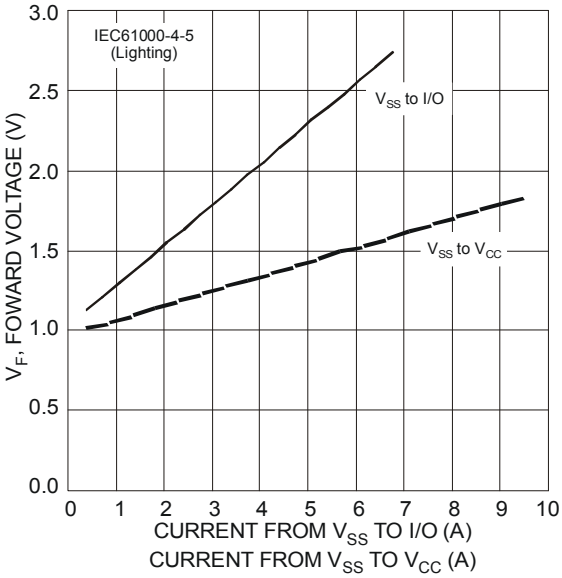

Figure 4 Forward Voltage Characteristics

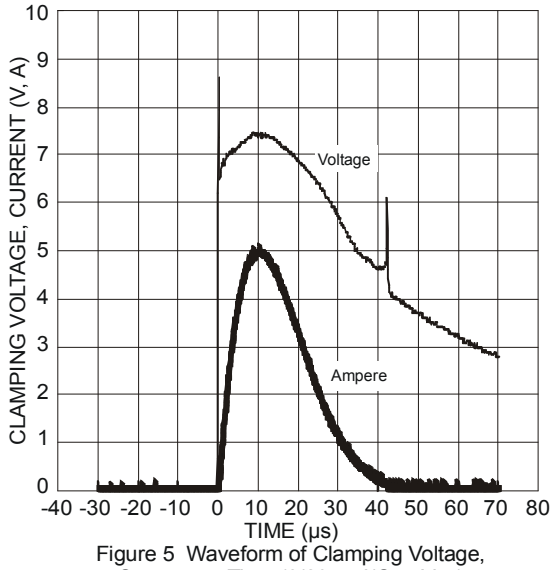

Figure 5 Waveform of Clamping Voltage, Current vs. Time (8/20µs, I/O to V_{SS})

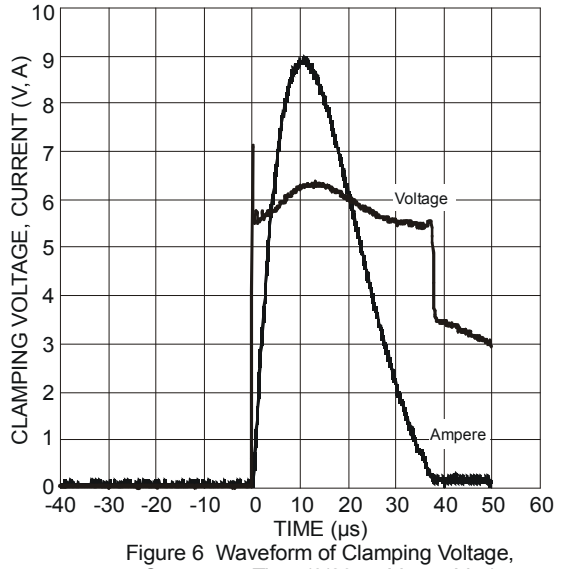

Figure 6 Waveform of Clamping Voltage, Current vs. Time (8/20µs, V_{CC} to V_{SS})

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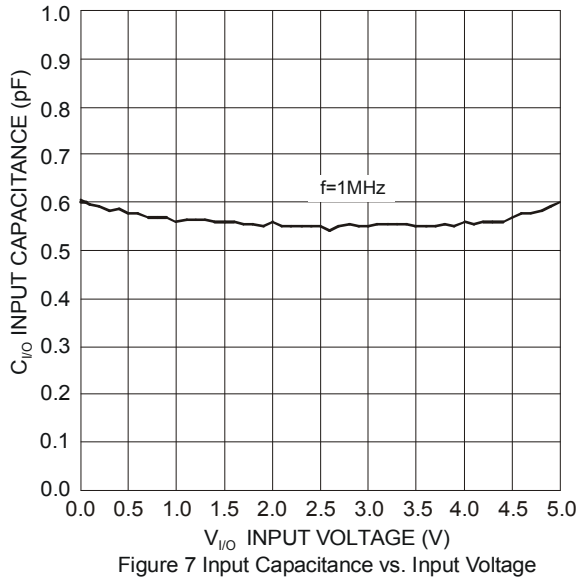


Figure 7 Input Capacitance vs. Input Voltage

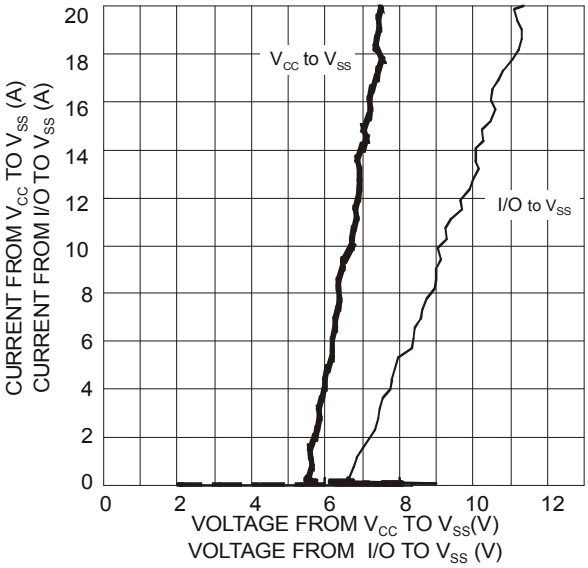
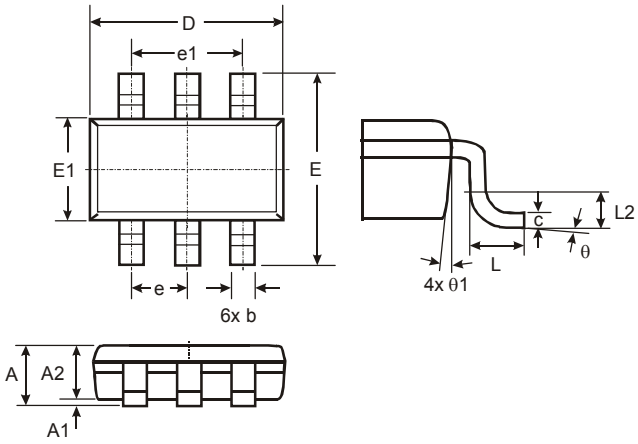


Figure 8. Current vs. Voltage

Package Outline Dimensions

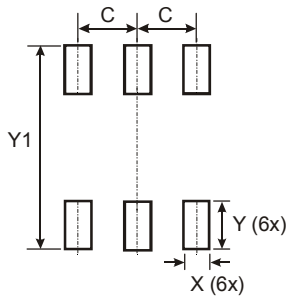
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



TSOT26			
Dim	**Min**	**Max**	**Typ**
A	–	1.00	–
A1	0.01	0.10	–
A2	0.84	0.90	–
D	–	–	2.90
E	–	–	2.80
E1	–	–	1.60
b	0.30	0.45	–
c	0.12	0.20	–
e	–	–	0.95
e1	–	–	1.90
L	0.30	0.50	
L2	–	–	0.25
θ	0°	8°	4°
θ1	4°	12°	–
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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